WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first gate stack structure and a second gate stack structure, including a first conductive pattern and a second conductive pattern, the first conductive pattern spaced apart from the second conductive pattern, the first gate stack structure adjacent to the second gate stack structure;

a vertical conductive line disposed adjacent to the first gate stack structure and the second gate stack structure; and

a semiconductor substrate extending to overlap with the first gate stack structure, the second gate stack structure, and the vertical conductive line,

wherein the semiconductor substrate includes a plurality of pass transistors connected to the first and second conductive patterns of at least one of the first gate stack structure and the second gate stack structure, and

wherein the vertical conductive line is connected to a plurality of gate electrodes of the plurality of pass transistors.

2. The semiconductor memory device of claim 1, wherein, on a plane parallel to the semiconductor substrate, the vertical conductive line extends in a first direction, and the first gate stack structure and the second gate stack structure are adjacent to each other in a second direction intersecting the vertical conductive line,

wherein the first gate stack structure includes a first end portion

and a second end portion spaced apart from the first end portion in the first direction, and

wherein the plurality of pass transistors include a first pass transistor overlapping with the first end portion of the first gate stack structure and a second pass transistor overlapping with the second end portion of the first gate stack structure.

3. The semiconductor memory device of claim 2, wherein the semiconductor substrate includes:

a first contact region in which the first pass transistor is disposed;

a second contact region in which the second pass transistor is disposed;

a cell array region between the first contact region and the second contact region;

a third contact region overlapping with the vertical conductive line; and

a row decoder region facing the second contact region with the first contact region and the cell array region interposed between the row decoder region and the second contact region, the row decoder region extending to be adjacent to the third contact region.

4. The semiconductor memory device of claim 3, further comprising:

a first lower conductive line disposed between the first pass

transistor and the first gate stack structure, the first lower conductive line connecting the first conductive pattern and the first pass transistor to each other;

a second lower conductive line disposed between the second pass transistor and the first gate stack structure, the second lower conductive line connecting the second conductive pattern and the second pass transistor to each other;

a row decoder disposed in the row decoder region of the semiconductor substrate; and

a third lower conductive line disposed at a level between the first pass transistor and the first gate stack structure, the third lower conductive line being connected to the row decoder.

5. The semiconductor memory device of claim 4, wherein each of the first lower conductive line, the second lower conductive line, and the third lower conductive line extends to overlap with the vertical conductive line.

6. The semiconductor memory device of claim 5, further comprising a plurality of conductive contact structures disposed between a level at which the vertical conductive line is disposed and a level at which the first to third lower conductive lines are disposed,

wherein the vertical conductive line is connected to the first lower conductive line, the second lower conductive line, and the third lower

conductive line via the plurality of conductive contact structures.

7. The semiconductor memory device of claim 3, further comprising:

a channel layer overlapping with the cell array region of the semiconductor substrate, the channel layer penetrating the first gate stack structure;

a memory layer between the channel layer and the first gate stack structure;

a bit line disposed between the channel layer and the semiconductor substrate, the bit line being connected to the channel layer; and

a source layer extending to overlap with the first gate stack structure and the second gate stack structure, the source layer being in contact with the channel layer.

8. The semiconductor memory device of claim 7, further comprising a vertical insulating layer extending along surfaces of the vertical conductive line, which face the first gate stack structure, the second gate stack structure, and the source layer,

wherein the vertical insulating layer is thicker than the memory layer.

9. A semiconductor memory device, comprising:

a semiconductor substrate including a peripheral circuit structure;

a vertical conductive line disposed over the semiconductor substrate, the vertical conductive line extending in a first direction on a plane parallel to the semiconductor substrate, the vertical conductive line being connected to the peripheral circuit structure;

a vertical insulating layer extending on a sidewall of the vertical conductive line; and

a first gate stack structure and a second gate stack structure, adjacent to each other in a second direction intersecting the vertical conductive line,

wherein the vertical conductive line and the vertical insulating layer are disposed between the first gate stack structure and the second gate stack structure, and

wherein each of the first gate stack structure and the second gate stack structure includes a plurality of interlayer insulating layers and a plurality of conductive patterns, which are alternately stacked over the semiconductor substrate, and

wherein the vertical conductive line protrudes farther in the first direction than each of the first and second gate stack structures.

10. A semiconductor memory device, comprising:

a semiconductor substrate including a peripheral circuit structure;

a vertical conductive line disposed over the semiconductor substrate, the vertical conductive line extending in a first direction on a plane

parallel to the semiconductor substrate, the vertical conductive line being connected to the peripheral circuit structure;

a vertical insulating layer extending on a sidewall of the vertical conductive line; and

a first gate stack structure and a second gate stack structure, adjacent to each other in a second direction intersecting the vertical conductive line,

wherein the vertical conductive line and the vertical insulating layer are disposed between the first gate stack structure and the second gate stack structure, and

wherein each of the first gate stack structure and the second gate stack structure includes a plurality of interlayer insulating layers and a plurality of conductive patterns, which are alternately stacked over the semiconductor substrate,

wherein the peripheral circuit structure includes a first circuit group, a second circuit group, and a third circuit group, which are connected to the vertical conductive line and are spaced apart from each other, and

wherein the vertical conductive line is configured to transmit a signal output from the third circuit group to the first circuit group and the second circuit group.

11. The semiconductor memory device of claim 10, wherein the third circuit group is configured to output the signal corresponding to a block select signal, and

wherein the first circuit group and the second circuit group are configured to transmit operating voltages to the plurality of conductive patterns of one of the first gate stack structure and the second gate stack structure in response to the block select signal.

12. The semiconductor memory device of claim 11, wherein the plurality of conductive patterns include a first local line and a second local line, which are spaced apart from each other in a direction intersecting a top surface of the semiconductor substrate,

wherein the first circuit group includes a first pass transistor connected to the first local line, and

the second circuit group includes a second pass transistor connected to the second local line, and

wherein the vertical conductive line is commonly connected to a first gate electrode of the first pass transistor and a second gate electrode of the second pass transistor.

13. The semiconductor memory device of claim 10, further comprising:

a channel layer penetrating the first gate stack structure and the second gate stack structure;

a memory layer surrounding a sidewall of the channel layer;

a bit line disposed between the peripheral circuit structure and the channel layer, the bit line being connected to the channel layer; and

a source layer extending to overlap with the first gate stack structure and the second gate stack structure, the source layer being in contact with the channel layer.

14. The semiconductor memory device of claim 13, wherein each of the channel layer and the vertical conductive line protrudes farther toward the source layer than the memory layer.

15. The semiconductor memory device of claim 13, wherein the vertical insulating layer extends between the source layer and the vertical conductive line.

16. The semiconductor memory device of claim 13, wherein the vertical insulating layer is thicker than the memory layer.

17. A semiconductor memory device comprising:

a semiconductor substrate including a first circuit group and a second circuit group, which are spaced apart from each other;

a memory cell array overlapping with the semiconductor substrate;

a vertical conductive line crossing the memory cell array, the vertical conductive line overlapping with the semiconductor substrate;

a plurality of first conductive bonding patterns disposed at a level between the semiconductor substrate and the memory cell array, the

plurality of first conductive bonding patterns being respectively connected to the first circuit group and the second circuit group; and

a plurality of second conductive bonding patterns disposed at a level between the plurality of first conductive bonding patterns and the memory cell array, the plurality of second conductive bonding patterns being connected to the vertical conductive line and the memory cell array, the plurality of second conductive bonding patterns being bonded to the plurality of first conductive bonding patterns,

wherein the vertical conductive line is commonly connected to the first circuit group and the second circuit group via parts of the plurality of first conductive bonding patterns and parts of the plurality of second conductive bonding patterns.

18. The semiconductor memory device of claim 17, wherein the memory cell array includes:

a plurality of interlayer insulating layers and a plurality of conductive patterns, alternately stacked over the semiconductor substrate;

a channel layer penetrating the plurality of interlayer insulating layers and the plurality of conductive patterns; and

a memory layer surrounding a sidewall of the channel layer.

19. The semiconductor memory device of claim 18, further comprising:

a source layer in contact with the channel layer, the source layer extending to overlap with the vertical conductive line; and

a vertical insulating layer extending along surfaces of the vertical conductive line, which face the plurality of interlayer insulating layers, the plurality of conductive patterns, and the source layer.

20. The semiconductor memory device of claim 19, wherein the vertical insulating layer is thicker than the memory layer.