FIG. 1

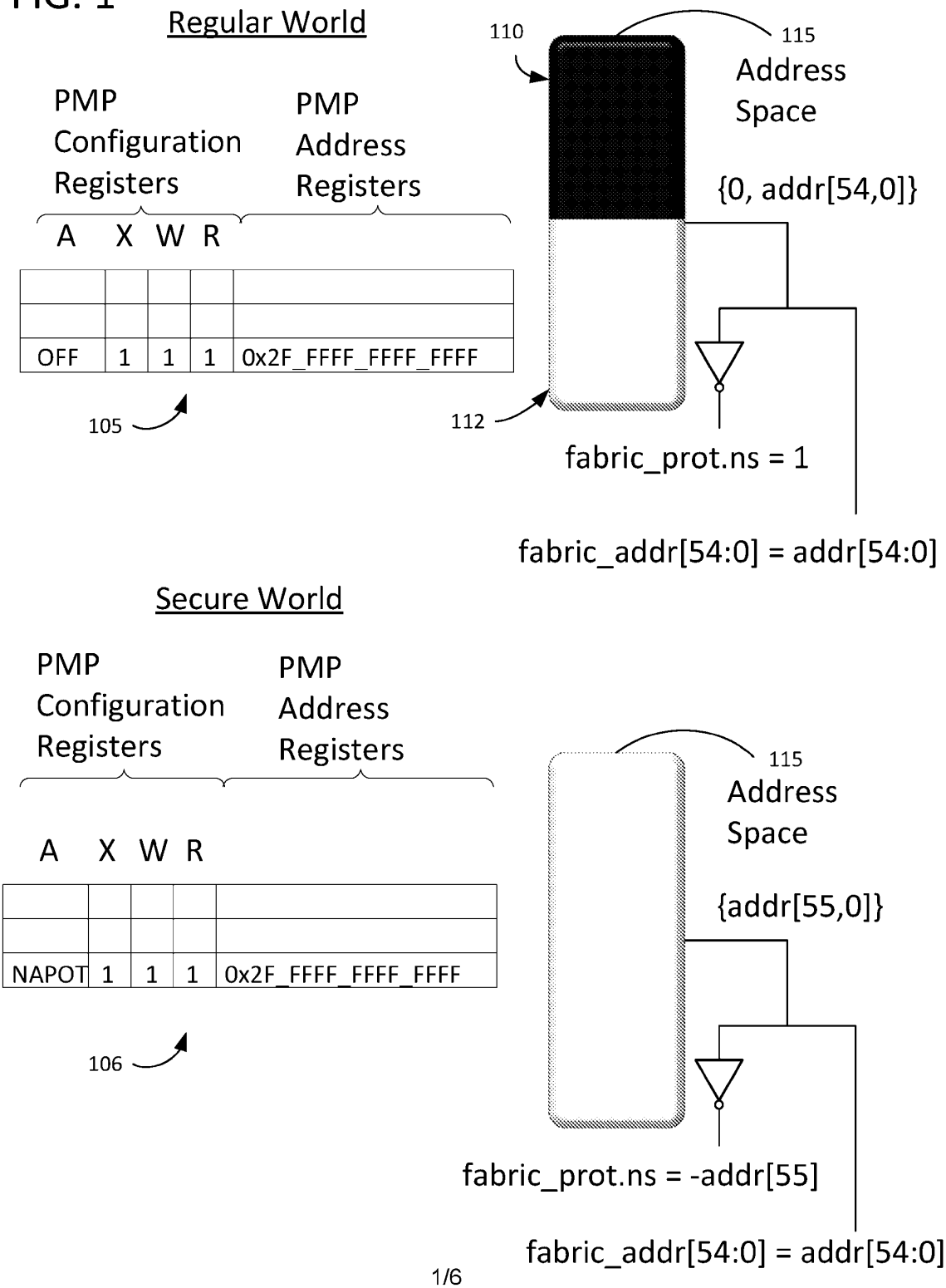
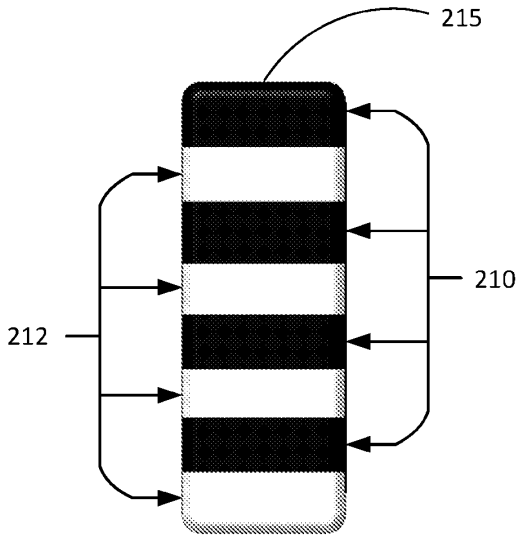

Regular World
PMP Configuration Registers
PMP Address Registers
A X W R
OFF 1 1 1 0x2F_FFFF_FFFF_FFFF
105
110
115
Address Space
{0, addr[54,0]}
112
fabric_prot.ns = 1
fabric_addr[54:0] = addr[54:0]
Secure World
PMP Configuration Registers
PMP Address Registers
A X W R
NAPOT 1 1 1 0x2F_FFFF_FFFF_FFFF
106
115
Address Space
{addr[55,0]}
fabric_prot.ns = -addr[55]
fabric_addr[54:0] = addr[54:0]

FIG. 2

Regular World



Secure World

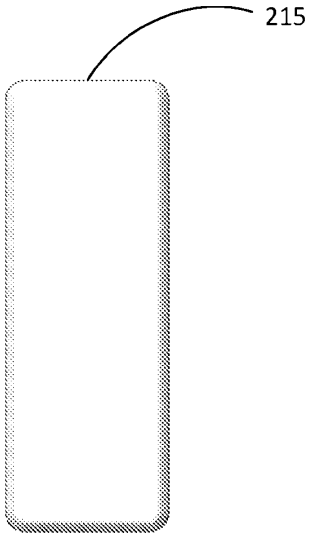


FIG. 3

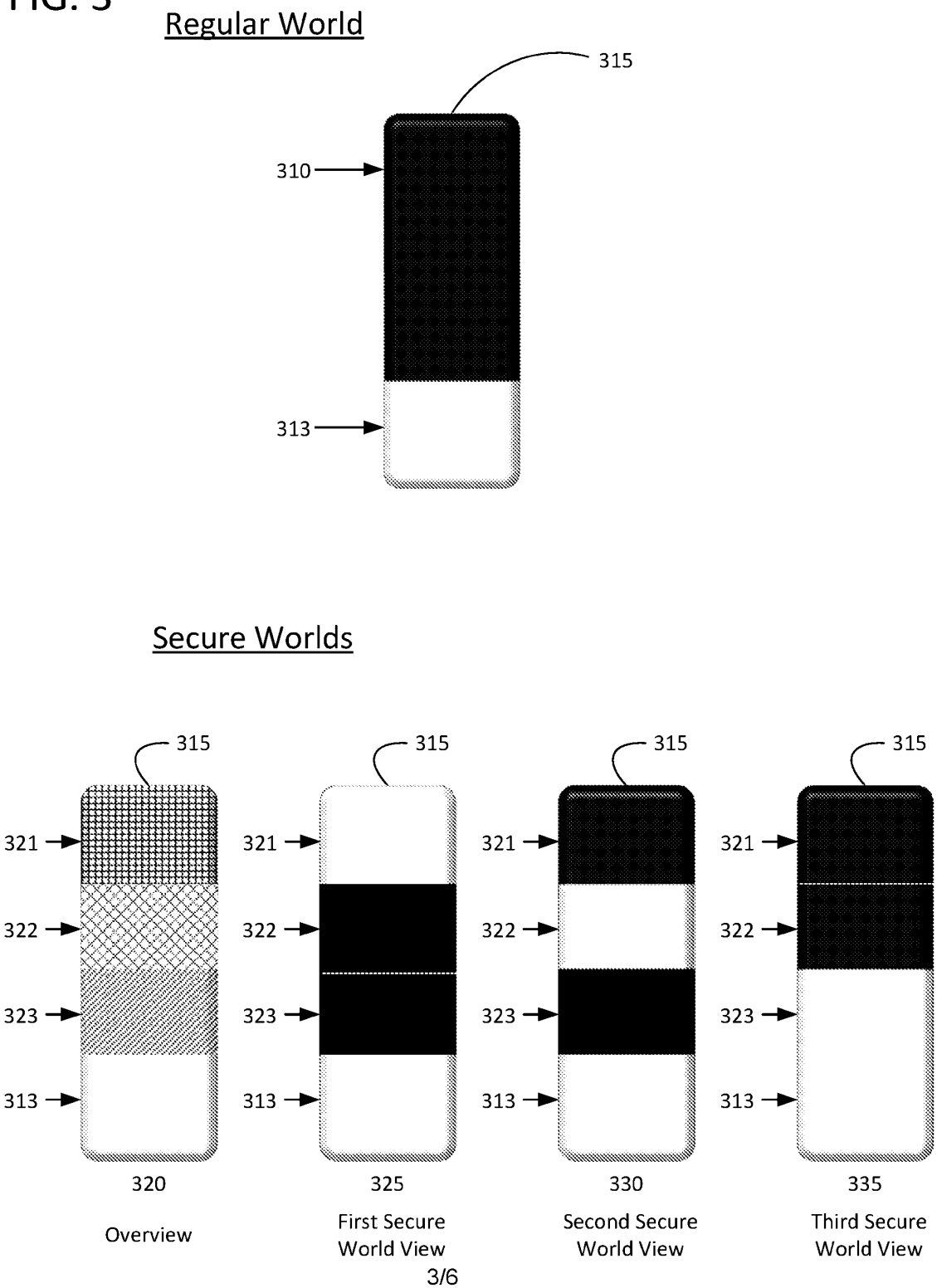

Regular World
315
310
313
Secure Worlds
315
321
322
323
313
320
Overview
315
321
322
323
313
325
First Secure World View
315
321
322
323
313
330
Second Secure World View
315
321
322
323
313
335
Third Secure World View

FIG. 4

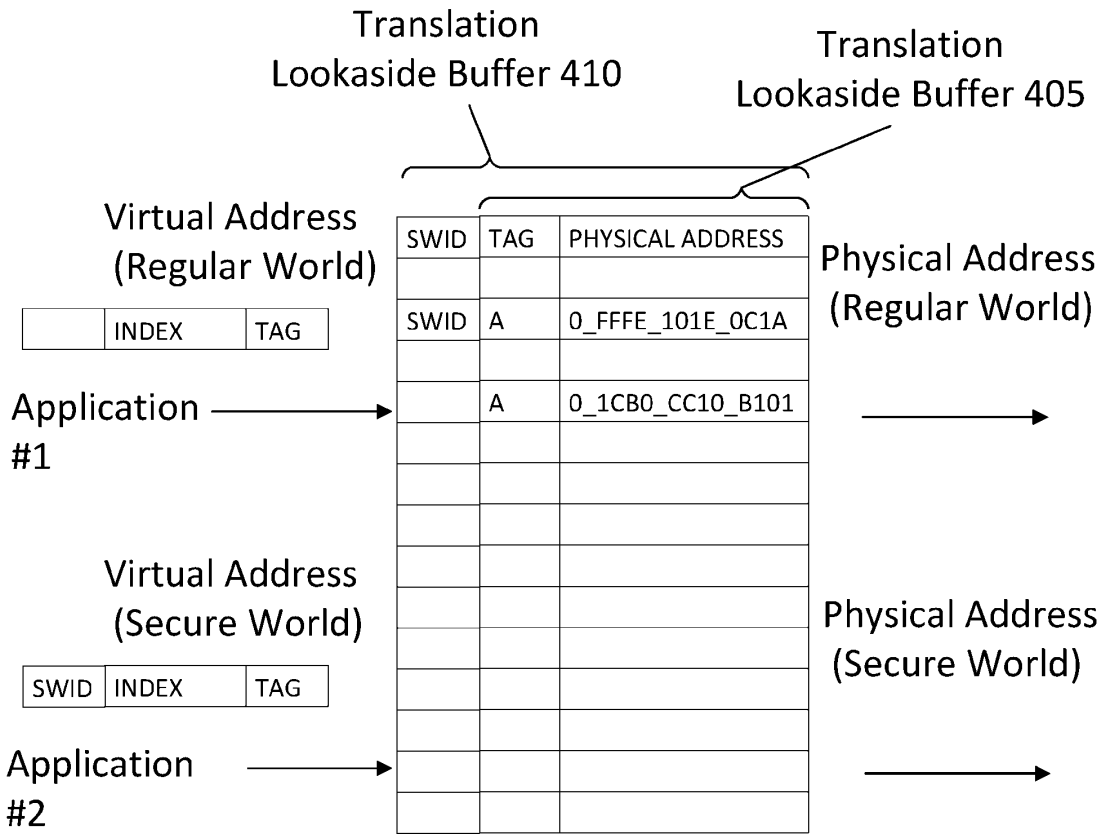

Translation
Lookaside Buffer 410
Translation
Lookaside Buffer 405
Virtual Address
(Regular World)
INDEX
TAG
Application
#1
Virtual Address
(Secure World)
SWID
INDEX
TAG
Application
#2
SWID
TAG
PHYSICAL ADDRESS
SWID
A
0_FFFE_101E_0C1A
A
0_1CB0_CC10_B101
Physical Address
(Regular World)
Physical Address
(Secure World)

FIG. 5

Custom Machine Address Translation and Protection CSR (matp)

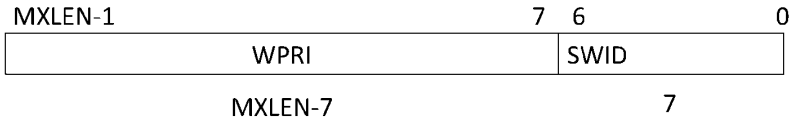
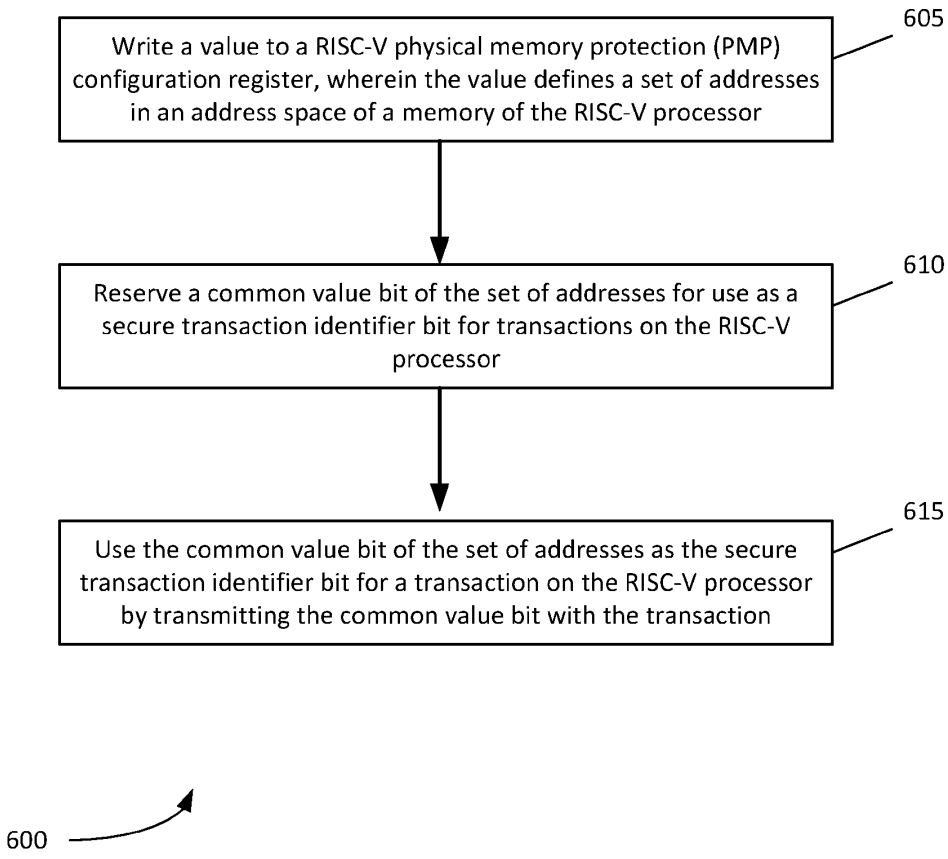


FIG. 6


Write a value to a RISC-V physical memory protection (PMP) configuration register, wherein the value defines a set of addresses in an address space of a memory of the RISC-V processor
605
Reserve a common value bit of the set of addresses for use as a secure transaction identifier bit for transactions on the RISC-V processor
610
Use the common value bit of the set of addresses as the secure transaction identifier bit for a transaction on the RISC-V processor by transmitting the common value bit with the transaction
615
600