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PIECEWISE LINEARIZED FOCUS VOLTAGE CIRCUIT FOR TELEVISION APPARATUS

This invention relates to modulated focus voltage circuits for television apparatus.

5 The need for focus control is well understood in the art. It was experienced early in television apparatus as an incident to the scanning of cathode-ray tubes because the distance from the center of deflection to the scanned raster is not uniform. Actually, that distance varies markedly as the beam is deflected
10 horizontally and vertically from the central portion of the screen and, consequently, defocusing is most severe at the corners of the raster. The adaption of picture tubes of increased size and wider deflection angles in recent years has emphasized the defocusing effect at the corners of the scanning pattern.

15 Efforts have been made to control focus in electrostatically focused tubes by changing the magnitude of the focus potential with displacement of the beam from the center of the raster. This technique is referred to as dynamic focusing. It comprises the application of a unidirectional potential to the focus
20 electrode of the electrostatically focused cathode-ray tube to establish the proper focus condition at the center of the raster and the concurrent application of a suitable varying potential to preserve that condition throughout the scanning raster. Since, in the usual case, the beam focus changes approximately in
25 accordance with a parabolic function along either scanning direction, the varying components of focus potential may have a parabolic waveform in both axes.

Typically, a vertical rate parabolic waveform is produced by integrating a sawtooth waveform that is
30 synchronized to, for example, a vertical deflection current. Also, multiplication can be used. Disadvantageously, both techniques may require complex circuitry.

In accordance with an aspect of the invention, a vertical rate trapezoidal waveform is produced from a vertical
35 sawtooth signal using a piecewise linearization technique. The trapezoidal waveform is applied to the focus electrode and approximates the aforementioned parabolic waveform. Because

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no signal integration is required, the circuitry may be less expensive and better controlled.

5 A focus voltage generating apparatus, embodying an aspect of the invention, with deflection frequency modulation of the focus voltage, includes a source of a first signal at a frequency that is related to a deflection frequency. A switching arrangement is responsive to the first signal for producing piecewise linearized portions of a modulation signal, during corresponding portions of a trace interval of a deflection cycle. The focus voltage is modulated
10 in accordance with the modulation signal.

The sole FIGURE illustrates a dynamic focus voltage generating circuit 100, embodying an aspect of the invention. A conventional vertical deflection circuit 101, not shown in detail, generates in a sampling resistor R01 that is coupled in series with
15 a vertical deflection winding LV a vertical rate sawtooth VSAW. During a trace interval TRACE, signal VSAW is substantially a linear upramping voltage. During a retrace interval RT, signal VSAW is a downramping voltage.

Signal VSAW is AC coupled to a non-inverting input
20 terminal of an amplifier 102 operating as a non-inverting amplifier. An inverting input terminal of amplifier 102 is AC coupled via a capacitor C20a to a DC blocking capacitor C01 that is coupled in series with resistor R01. A voltage V6.8 at 6.8V is coupled via a resistor R13 to the non-inverting input terminal and
25 via a resistor R14 to the inverting input terminal of amplifier 102. Such an arrangement requires only a positive supply voltage of 12V and no negative supply voltage for energizing amplifier 102.

Amplifier 102 produces an output signal V102 that varies in a ramping manner, during vertical trace interval TRACE.
30 Similarly, signal VSAW is AC coupled to an amplifier 103 operating as an inverting amplifier. Amplifier 103 produces an output signal V103 that varies in a ramping manner but at opposite direction or phase with respect to signal V102, during interval TRACE. Signals V102 and V103 are selectively coupled
35 via diodes CR20 and CR21, respectively, operating as switches to an emitter of a clamp transistor Q01. A clamping reference voltage that is equal to 5.6V is developed at a base of transistor Q01.



In accordance with an aspect of the invention, during approximately the beginning third of the length of interval TRACE, upramping signal V102 is smaller than 5.6V. Therefore, diode CR20 conducts and clamp transistor Q01 is nonconductive. An
5 upramping portion TR1 of a trapezoidal signal VT is developed at the emitter of transistor Q01. Following interval TR1, when signal V102 exceeds 5.6V, diode CR20 becomes nonconductive and signal VT is clamped by transistor Q01 to a voltage that is equal to a clamp level VCLAMP. Level VCLAMP is equal to 6.2V or the sum
10 of 5.6V and the forward emitter-base voltage of transistor Q01. Transistor Q01 maintains signal VT at level CLAMP for approximately one third of the length of interval TRACE to form a portion TR2. Thereafter, during the last third of interval TRACE, downramping signal V103 is smaller than the difference between
15 level VCLAMP and the forward voltage of diode CR21. Consequently, diode CR21 conducts and transistor Q01 is nonconductive. As a result, a downramping portion TR3 of signal VT is produced. During vertical retrace interval RT, the waveform of signal VT has no significance because of vertical blanking.
20 Trapezoidal signal VT is coupled via an emitter follower transistor Q02 to a resistor R23 that is coupled to an inverting input terminal 104a of an amplifier 104.

In accordance with an inventive feature, during ramping portions TR1 and TR3, temperature related variation of
25 the forward voltage of diode CR20 or CR21 is compensated and prevented from affecting the emitter voltage of transistor Q02 by the corresponding variation of the base-emitter forward voltage of transistor Q02. Similarly, during portion TR2, temperature related variation of the forward voltage of transistor Q01 is
30 compensated by that of transistor Q02.

Amplifier 104 that is responsive to the temperature compensated emitter voltage of transistor Q02 is formed by a pair of transistors Q03 and Q06, each operating in an emitter follower configuration, having emitters that are coupled to the bases of a
35 pair of transistors Q04 and Q06, respectively. Transistors Q04 and Q06 are coupled to each other as a transistor pair forming a differential amplifier. A collector of transistor Q04 is coupled to a conventional boot-strap pull-up arrangement 105. Arrangement



105 includes a collector load resistor R30 of transistor Q04 that is coupled to a supply voltage of +250V. An active pull-up transistor Q07 operating as an emitter follower when the collector voltage of transistor Q04 increases has a base that is coupled to the collector of transistor Q04. A diode CR03, coupled between the emitter of transistor Q07 and the collector of transistor Q04, provides an active pull-down current path when the collector voltage of transistor Q04 decreases. A negative feedback path forming resistor R24 is coupled between inverting input terminal 104a and the collector of transistor Q04.

A voltage reference, developed at a non-inverting input terminal 104b of amplifier 104, is equal to the emitter voltage of transistor Q02 when transistor Q01 performs clamping operation. Resistor R24 causes the collector voltage and, hence, a voltage VT2 at an output terminal 104c of amplifier 104 to be approximately 0V when the emitter voltage of transistor Q02 is nominally equal to 5.6V, during portion TR2 of signal VT. During portion TR3 of signal VT, voltage VT2 at terminal 104c is downramping, whereas, during portion TR1, it is upramping. The gain of amplifier 104 is such that the peak level of trapezoidal voltage VT2 at terminal 104c is 200V.

Advantageously, because of common mode cancellation, the waveform of voltage VT2 is not degraded or changed when supply voltages change within a wide tolerance range. Furthermore, the same circuit can be used without modification with different vertical deflection frequencies because it is insensitive to frequency variations.

Trapezoidal voltage VT2 at the vertical rate V developed at terminal 104c is coupled to an end terminal W2a of a secondary winding W2 of a transformer T. A horizontal rate signal produced in a conventional manner in a horizontal output stage 99 is applied to a winding W1 of transformer T. An output signal VOUT, developed at a terminal W2b of winding W2 is equal to the sum of the vertical rate waveform at terminal W2a and a horizontal rate signal developed in winding W2. Signal VOUT is AC-coupled to a focus electrode F for providing dynamic focus voltage. Signal VOUT is superimposed on a high level DC voltage produced in a voltage divider 110 from an ultor voltage U in a



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conventional manner.

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WHAT IS CLAIMED IS:

1. A focus voltage generating apparatus with deflection frequency modulation of the focus voltage (F), comprising:
 - 5 a source (101) of a first signal (VSAW) at a frequency that is related to a deflection frequency (V); characterized by switching means (CR20, CR21) responsive to said first signal for producing piecewise linearized portions of a modulation signal (VT), during corresponding portions (TR1, TR3) of a trace
 - 10 interval of a deflection cycle;
a source of a high voltage (U); and
means (110, 105) coupled to said high voltage source and to said switching means for generating said focus voltage that is modulated in accordance with said modulation signal.
 - 15
2. An apparatus according to Claim 1, characterized in that said first signal (VSAW) is a sawtooth signal, and wherein a ratio between a rate of change of a portion (TR1) of said modulation signal (VT) and a rate of change of said sawtooth
- 20 signal (VSAW) is substantially constant, during a corresponding portion (1/3 of trace) of said trace interval.
3. An apparatus according to Claim 1 further characterized by, means (102) responsive to said first signal
- 25 (VSAW) for generating a first sawtooth signal (V102), wherein said switching means (CR20) is responsive to said first sawtooth signal for coupling said first sawtooth signal to said focus voltage generating means (110) during a first portion (TR1) of said trace interval, and for decoupling said first sawtooth signal from said
- 30 focus voltage generating means, during a second portion (TR3) of said trace interval, in accordance with a magnitude of said first sawtooth signal.
4. An apparatus according to Claim 3 further
- 35 characterized by, a source (103) of a second sawtooth signal (V103) that varies in an opposite direction with respect to said first sawtooth signal (V102), wherein said switching means (CR20, CR21) couples said first and second sawtooth signals to said





focus voltage generating means (110) during said first (TR1) and second (TR2) portions of said trace interval, respectively.

5 5. An apparatus according to Claim 1, characterized in that said modulation signal (VT1, VT2) varies in a trapezoidal manner during said trace interval.

6. An apparatus for generating a focus voltage (F), comprising:

10 a source (101) of a sawtooth signal (V102) at a frequency that is related to a deflection frequency (VERTICAL); means (CR20) responsive to said sawtooth signal for generating a first portion (TR1) of a modulation signal (VT), during a first portion of a trace interval, having a rate of change
15 that is determined in accordance with said sawtooth signal; characterized by

clamping means (Q01) coupled to said modulation signal generating means for generating a second portion (TR2) of said modulation signal that is clamped to a predetermined
20 clamping level (6.2V), during a second portion of said trace interval;

a source of a high voltage (U); and
means (110, 105) responsive to said modulation signal and coupled to said source of high voltage for generating
25 therefrom said focus voltage.

7. An apparatus according to Claim 6, further characterized by, means (103) for generating a second sawtooth signal (V103) at a frequency that is related to said deflection
30 frequency that varies in opposite directions with respect to said first sawtooth signal (V102), wherein said modulation signal generating means comprises switching means (CR21) responsive to said second sawtooth signal for generating a third ramping portion (TR2) of said modulation signal (VT) that varies in
35 opposite direction with respect to said first portion of said modulation signal such that said clamped, second portion (TR2) of said modulation signal occurs between said first and third portions of said modulation signal.



8. An apparatus according to Claim 7, characterized in that said switching means (CR21, CR20) comprises first (CR20) and second (CR21) diodes for coupling said first (V102) and second (V103) sawtooth signals, respectively, to said clamping means (Q01).

9. An apparatus according to Claim 6, characterized in that said clamping means (Q01) comprises a bipolar transistor (Q01) and wherein said modulation signal (VT) is developed at an emitter electrode of said transistor.

10. An apparatus according to Claim 9, further characterized by, an emitter follower (Q02) responsive to said modulation signal (VT) and coupled to said focus voltage generating means (110) for providing temperature compensation for temperature related variations in each of said diodes (CR20, CR21) and said bipolar transistor (Q01) of said clamping means.

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