METHOD FOR FABRICATING A SELF ALIGNED S/D CMOS DEVICE ON INSULATED LAYER BY FORMING A TRENCH ALONG THE STI AND FILL WITH OXIDE

Abstract

A method for a self aligned TX with elevated source/drain (S/D) regions on an insulated layer (oxide) by forming a trench along side the STI and filling the trench with oxide. STI regions are formed in a substrate. A gate structure is formed. LDD regions are formed adjacent to the gate structure in the substrate. Spacers are formed on the sidewall of the gate structure. We etch S/D trenches between the STI regions and the first spacers. The S/D trenches are filled with a S/D insulating layer. Elevated S/D regions are formed over the S/D insulating layer and the LDD regions. A top isolation layer is formed over the STI regions. The invention builds the raised source/drain (S/D) regions on an insulating layer and reduces junction leakage and hot carrier degradation to gate oxide.

Fig. 3B