METHOD FOR PASSIVATION OF PLASMA ETCH DEFECTS IN DRAM DEVICES

ABSTRACT

A process for fabricating an MOS device specifically a DRAM device, featuring passivation of defects in regions of a semiconductor substrate wherein defects left unpassivated can deleteriously influence data retention time, has been developed. A high density plasma dry etching procedure used to define the DRAM conductive gate electrode can create unwanted defects in a region near the surface of uncovered portions of the semiconductor substrate during the high density plasma procedure over etch cycle. Implantation of a group V element such as arsenic can be used to passivate the unwanted plasma etch defects, thus reducing the risk of defect related device leakage phenomena. However to insure the group V implanted species remain at or near the semiconductor surface for optimum defect passivation, the group V element implantation procedure is performed after all high temperature DRAM fabrication steps, such as selective oxidation for creation of oxide spacers on the sides of the conductive gate electrode, have been completed. A slow diffusing implanted arsenic ion is the optimum candidate for passivation while faster diffusing group V elements such as phosphorous are not as attractive for defect passivation.

Fig. 8