

ABSTRACTSEMICONDUCTOR MEMORY DEVICE

5           According to one embodiment, a semiconductor memory device includes a memory cell array, a first sense amplifier circuit, and a second sense amplifier circuit. The memory cell array includes a plurality of first memory cell units, a plurality of second memory cell units, a plurality of first interconnects, and a plurality of second interconnects. The first sense amplifier circuit is connected to the plurality of first interconnects. The second sense amplifier circuit is connected to the plurality of second interconnects. Heights of upper surfaces of interconnects are equal. At least one of a width of each of the plurality of second interconnects along a second direction perpendicular to the first direction and a thickness of each of the plurality of second interconnects along a third direction perpendicular to the first direction and the second direction is set smaller than each of the plurality of first interconnects, and the first sense amplifier circuit and the second sense amplifier circuit are disposed to face each other across the memory cell array.

FIG. 1

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