

SEMICONDUCTOR DEVICE

ABSTRACT OF THE DISCLOSURE

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A semiconductor device capable of reducing a cell area without affecting the accuracy, capable of reducing the number of interconnection layers, and capable of realizing a hybrid circuit of a memory cell and peripheral
10 circuit easily and at a low cost, including a bit line, a word line, control gate line, a capacitor with a first electrode connected to the word line, a read transistor comprising an NMOS connected between the bit line and a predetermined potential point and with a gate electrode
15 connected to a second electrode of a capacitor, and a write transistor comprising an NMOS connected between the bit line and the second electrode of the capacitor and with a gate electrode connected to the control gate line.

Fig. 1