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**ELECTRONIC DEVICES FORMED OF TWO OR MORE SUBSTRATES
BONDED TOGETHER, ELECTRONIC SYSTEMS COMPRISING
ELECTRONIC DEVICES AND METHODS OF MAKING
ELECTRONIC DEVICES**

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PRIORITY CLAIM

This application claims the benefit of the filing date of United States Patent Application Serial No. 12/401,387, filed March 10, 2009, for "Electronic Devices Formed of Two or More Substrates Bonded Together, Electronic Systems Comprising
10 Electronic Devices and Methods of Making Electronic Devices."

TECHNICAL FIELD

Embodiments of the present disclosure relate to electronic devices comprising at least two substrates bonded together.

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BACKGROUND

Electronic devices, and specifically semiconductor devices and memory devices, are becoming increasingly more complex. Accordingly, circuitry area or space, also termed "real estate," in electronic devices is becoming more and more
20 limited. In an effort to provide more circuitry on a single semiconductor chip without increasing the size, as well as in an effort to reduce the size of other semiconductor chip, the circuitry has become increasingly smaller and a greater number of circuits are formed on a single chip. For example, memory devices have reduced from microscale devices and circuits to nanoscale devices and circuits. Nanoscale is conventionally
25 defined as referring to circuits and pitches less than 100 nanometers.

An example of a memory device having memory cells formed on the nanoscale includes magnetic shift registers, conventionally referred to as "racetrack memory." An example of racetrack memory is described in U.S. Patent No. 6,834,005 to Parkin, assigned to International Business Machines Corporation (IBM). FIG. 10 of the
30 drawings of the present application is a schematic diagram illustrating a prior art embodiment of an array of racetrack memory. Racetrack memory may include an array of nanoscale wires or tracks 1010 made of a ferromagnetic material. Each track 1010 may include a plurality of magnetic shift registers 1020 connected to each

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other in series. Each magnetic shift register 1020 includes a writing device 1030 and a reading device 1040 associated therewith. Because of the small size of the tracks 1010, the array of tracks 1010 may be arranged very close together in a memory device.

While nanoscale memory cells are desirable for providing increased storage capacity in a limited real estate, conventional supporting circuitry (e.g., charge pumps, decode and addressing circuits, sense amplifiers, I/O circuits, etc. (not shown)) of a memory device may not need to be formed on such a small scale and, indeed, may be more efficiently and economically formed on a microscale as opposed to a nanoscale.

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BRIEF SUMMARY

Various embodiments of the present disclosure are directed toward embodiments of an electronic device and method for forming an electronic device comprising both nanoscale circuitry and microscale circuitry. In at least one embodiment, an electronic device may comprise a first substrate comprising circuitry.

15 The circuitry of the first substrate may include a plurality of conductive traces extending at least substantially parallel to each other through a portion of the first substrate. A plurality of bond pads may be positioned on a surface of the first substrate and may comprise a width extending over at least two of the plurality of conductive traces. A plurality of vias may extend from adjacent at least some conductive traces of

20 the plurality of conductive traces to bond pads of the plurality of bond pads. A second substrate comprising circuitry coupled to the plurality of bond pads on the first substrate with a plurality of conductive bumps may be bonded to the first substrate.

Further embodiments are directed to memory devices. Various embodiments of such memory devices may comprise a first substrate including a plurality of

25 magnetic tracks comprising a plurality of domains having domain walls. A plurality of magnetic tunneling junctions may be positioned proximate to the plurality of magnetic tracks and may extend to a location adjacent a surface of the first substrate. A plurality of bond pads may be positioned on the surface of the first substrate. Each bond pad of the plurality of bond pads may be electrically coupled to a magnetic tunneling junction

30 of the plurality of magnetic tunneling junctions.

Additional embodiments comprise methods of forming an electronic device. One or more embodiments of such methods may comprise forming a first substrate and

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a second substrate. The first substrate may comprise a plurality of conductive traces extending through a portion thereof, a plurality of vias extending from adjacent at least some conductive traces of the plurality of conductive traces to a surface of the first substrate, and a plurality of bond pads on the surface of the first substrate and adjacent
5 to a via of the plurality of vias. Each bond pad of the plurality of bond pads may comprise a width extending over at least two conductive traces of the plurality of conductive traces. The second substrate may comprise circuitry, and the second substrate may be attached to the first substrate with a plurality of conductive bumps coupled to the plurality of bond pads of the first substrate and to the circuitry of the
10 second substrate.

In yet further embodiments, the disclosure includes methods of forming a memory device. According to various embodiments, such methods may comprise forming a plurality of conductive traces in a first substrate. The plurality of conductive traces may be configured as magnetic shift registers comprising a plurality of domains
15 having domain walls. A plurality of vias may be formed comprising magnetic tunneling junctions extending from a surface of the first substrate to proximate the plurality of magnetic shift registers. A plurality of bond pads may also be formed, each bond pad of the plurality of bond pads being coupled to a via of the plurality of vias.

Still other embodiments of the disclosure include electronic systems. One or
20 more embodiments of such systems may comprise at least one processor and at least one memory device coupled to the processor. The at least one memory device may comprise a first substrate and a second substrate. The first substrate may comprise a plurality of magnetic tracks including a plurality of domains having domain walls, a plurality of magnetic tunneling junctions proximate to the plurality of magnetic tracks
25 and extending to a location adjacent a surface of the first substrate, and a plurality of bond pads on the surface of the first substrate. Each bond pad of the plurality of bond pads is electrically coupled to a magnetic tunneling junction of the plurality of magnetic tunneling junctions. The second substrate may comprise support circuitry and may be bonded to the plurality of bond pads with a plurality of conductive bumps.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectioned elevation view of a portion of an electronic device according to one or more embodiments.

FIG. 2 illustrates a top view of a portion of a first substrate depicting a plurality of bond pads disposed in a predefined pattern according to some embodiments.

FIG. 3 illustrates a top view of a portion of a first substrate depicting a plurality of bond pads disposed according to a predefined pattern of vias according to some embodiments.

FIG. 4 is a top view of a portion of a first substrate depicting the bond pads configured in a honeycomb pattern on the surface of the first substrate according to at least one embodiment.

FIG. 5 illustrates a top view of a portion of a first substrate comprising bond pads configured in a honeycomb pattern on the surface thereof according to at least one embodiment.

FIG. 6 illustrates a top view of an embodiment of the first substrate comprising bond pads having a triangular configuration.

FIG. 7A is a cross-sectioned elevation view of a portion of an electronic device according to at least one embodiment.

FIG. 7B is an enlarged view of a bond pad of the electronic device of FIG. 7A.

FIG. 8 illustrates a top view of the first substrate comprising bond pads structures including diodes formed thereon patterned according to at least one embodiment.

FIG. 9 is a schematic of a computing system diagram showing at least one semiconductor memory device containing at least one memory device according to at least one embodiment of the present invention.

FIG. 10 is a schematic diagram illustrating a prior art embodiment of a racetrack memory array.

MODE(S) FOR CARRYING OUT THE INVENTION

The illustrations presented herein are, in some instances, not actual views of any particular substrates, electronic devices, or memory devices, but are merely idealized representations which are employed to describe the present invention.

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Additionally, elements common between figures may retain the same numerical designation.

Various embodiments of the present disclosure comprise electronic devices configured to couple nanoscale electronic components, nanoscale pitches, or both to
5 microscale electronic components, microscale pitches, or both. FIG. 1 is a cross-sectioned elevation view of a portion of an electronic device 100 according to at least one embodiment. The electronic device 100 comprises a first substrate 110 and a second substrate 120 coupled together. The first substrate 110 and second substrate 120 may comprise semiconductor wafers or other bulk semiconductor
10 substrates in some embodiments, or singulated semiconductor dies in other embodiments.

The first substrate 110 comprises circuitry 140 disposed in a portion thereof. At least a portion of the circuitry 140 may comprise a small footprint that is densely configured. By way of example and not limitation, components of circuitry 140 may
15 be configured and disposed comprising a pitch P of less than 100 nanometers. In at least some embodiments, at least a portion of the components of circuitry 140 may comprise a plurality of conductive traces extending at least substantially parallel to each other through a portion of the first substrate 110.

Bond pads 150 may be disposed on a surface 160 of the first substrate 110 and
20 a plurality of vias 170 may extend from adjacent at least a portion of the circuitry 140 to the bond pads 150. By way of example and not limitation, the bond pads 150 may be sized and configured to comprise an area of about $2,000\ \mu\text{m}^2$ or greater. By way of example and not limitation, in at least some embodiments, the bond pads 150 may be configured substantially square and may be sized about $50\ \mu\text{m} \times 50\ \mu\text{m}$.

25 The bond pads 150 may be disposed in a pattern on the surface 160 of the first substrate 110 to provide a connection to each of the vias 170. Because the bond pads 150 comprise a substantially larger size (microscale) than the components of circuitry 140 (nanoscale), each bond pad 150 may comprise a width W extending over an area that crosses a portion of circuitry 140 comprising a plurality of components
30 (e.g., conductive traces). For example, each bond pad 150 may comprise a width W extending over two or more conductive traces of circuitry 140. Although the figures illustrate circuitry 140 comprising approximately 10 or 11 conductive traces below the

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width W of each bond pad 150, the differences in scales between the circuitry 140 and the bond pads 150 may facilitate hundreds or even thousands of such conductive traces below the width W of each bond pad 150 according to various embodiments.

FIG. 2 illustrates a top view of a portion of the first substrate 110 depicting a plurality of bond pads 150 disposed in a predefined pattern according to some embodiments. Such embodiments, in which the bond pads 150 are disposed according to a predefined pattern, may be referred to herein as a “bond raster” pattern. The bond pads 150 are depicted as partially transparent in order to illustrate the relationship between the circuitry 140, vias 170 and bond pads 150. According to various embodiments, a plurality of bond pads 150 may be disposed on the surface 160 in a fixed pattern to facilitate coupling the circuitry 140 to the bond pads 150 through vias 170. In the embodiments shown, the bond pads 150 are fixed in a pattern akin to bricks laid in a wall, in which each bond pad 150 is offset with respect to the bond pads 150 directly above and below (as oriented in FIG. 2), although those of ordinary skill in the art will recognize that any fixed pattern is contemplated as within the scope of embodiments of the invention. In some embodiments, the fixed offset may be approximately half the length of a side 210 of the bond pads 150. In such embodiments, the vias 170 may not be oriented in a fixed pattern. In other words, the vias 170 may not be coupled to the circuitry 140 in any apparent pattern.

FIG. 3 is a top view of a portion of a first substrate 110 depicting the bond pads 150 disposed according to other embodiments. According to at least some of such embodiments, the vias 170 may be coupled to the center, or at least substantially the center, of the respective bond pad 150, and the vias 170 may be configured according to a predefined pattern. In the embodiment of FIG. 3, the vias 170 are positioned in a pattern wherein each via is coupled to a conductive trace immediately adjacent to the conductive trace to which the via above and below (as oriented in FIG. 3) are coupled. The bond pads 150 are, therefore, shifted in accordance with the pattern of the vias 170. Such a configuration, of shifting the bond pads 150 in accordance with the predefined pattern of the vias 170, may be referred to herein as a “bond shift” pattern.

FIGS. 2 and 3 illustrate bond pads 150 having a substantially square or rectangular shape. However, those of ordinary skill in the art will recognize that a plurality of potential shapes and patterns have utility in implementation of various

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embodiments. By way of example and not limitation, FIGS. 4-6 illustrate various suitable configurations for the bond pads 150 according to embodiments of the first substrate 110.

FIG. 4 is a top view of a portion of a first substrate 110 depicting the bond pads 150 configured with a hexagonal shape and disposed in a honeycomb pattern on the surface 160. The vias 170 are shown as coupled to respective conductive traces of the circuitry 140 in accordance with the pattern of the bond pads 150. Such a honeycomb pattern may be formed to comprise a bond raster pattern in which the bond pads 150 are disposed according to a predefined pattern.

FIG. 5 illustrates another embodiment of the first substrate 110 comprising bond pads 150 configured with a hexagonal shape and disposed in a honeycomb pattern, comprising a bond raster pattern on the surface 160. In the embodiment of FIG. 5, the bond pads 150 are rotated slightly, in a few degrees about their centerpoints, resulting in a pattern that provides an improved coverage of the circuitry 140. The improved coverage is provided by disposing the bond pads 150 in a configuration that is angularly misaligned with the underlying circuitry 140 comprising conductive traces. In other words, according to the embodiments illustrated in FIG. 5, the bond pads 150 are not disposed in columns that run straight up and down in alignment with the underlying circuitry 140 that is configured to run substantially straight up and down (as oriented in FIG. 4). Such misalignment may improve the coverage of the circuitry 140 by providing at least one bond pad 150 that is positioned over each component of the circuitry 140 to enable coupling a via 170 for each component of the circuitry 140 to a substantially centralized portion of a bond pad 150. In other words, because the bond pads 150 are angularly misaligned with the underlying circuitry 140, each component of the circuitry 140, such as the conductive traces of FIG. 5, may have at least one bond pad 150 that is positioned substantially centrally thereover, enabling a via 170 to be positioned, and extend between each component of the circuitry 140 and a substantially central portion of a bond pad 150. Thus, vias 170 do not need to be coupled to a bond pad 150 along a peripheral edge thereof.

FIG. 6 illustrates another embodiment of the first substrate 110 comprising bond pads 150 having a triangular configuration and comprising a bond raster pattern. The bond pads 150 are ordered in pairs configured with bases of the triangles

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positioned facing each other and aligned together on the surface 160. The triangular-shaped bond pads 150 are also angularly misaligned with the underlying circuitry. In the embodiment shown, the bond pads 150 are disposed according to a pattern, while there is no apparent pattern by which the vias 170 are coupled to the circuitry 140.

Conductive bumps 130 may be formed on the bond pads 150 to electrically couple the bond pads 150 of the first substrate 110 to the second substrate 120 and any circuitry 125 thereon. The conductive bumps 130 may comprise any bump configuration known to those of ordinary skill in the art. By way of example, the conductive bumps 130 may be configured as bumps, pillars, studs, balls, columns, posts, or any other suitable physical structure, as well as combinations thereof. The conductive bumps 130 may comprise any conductive metal or alloy thereof, such as copper, gold, silver, aluminum, and alloys of any of the foregoing, conventional silver or tin/lead solder, a conductive or conductor-filled polymer, or conductive composites.

In additional embodiments, the electronic device may be configured to reduce the number of bond pads necessary to couple the circuitry 140 to a respective bond pad. FIG. 7A is a cross-sectioned elevation view of a portion of an electronic device 700 according to at least one embodiment. The electronic device 700 comprises a first substrate 110 and a second substrate 120 coupled together. The first substrate 110 and second substrate 120 may comprise semiconductor wafers or other bulk semiconductor substrates in some embodiments, or singulated semiconductor dies in other embodiments.

In FIG. 7A, the first substrate 110 again comprises circuitry 140 disposed in a portion thereof. In at least some embodiments, at least a portion of the circuitry 140 may comprise a plurality of conductive traces extending at least substantially parallel to each other through a portion of the first substrate 110. Bond pads 750 are disposed on the surface 160 of the first substrate 110 and a plurality of vias 170 extend from adjacent at least a portion of the circuitry 140 to the bond pads 750. The bond pads 750 comprise a selection device 705 formed in a portion thereof configured to enable access to a plurality of discrete vias 170. In at least some embodiments, the selection device 705 may comprise a plurality of diodes or similar rectifying devices. FIG. 7B is an enlarged view of a bond pad 750 of the electronic device of FIG. 7A, indicated by

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the designation 7B in FIG. 7A and appropriate broken lead line and oval. Each bond pad 750 of the electronic device 700 may comprise a first diode 710 and a second diode 720, positioned in side by side relationship. The first diode 710 and the second diode 720 may both be coupled to a common upper conductive pad 730 disposed over a portion of each diode 710, 720. The first diode 710 is coupled to a first lower conductive pad 760, and the second diode 720 is coupled to a second lower conductive pad 770, the first lower conductive pad 760 and second lower conductive pad 770 being electrically isolated from each other by gap 780. The conductive bump 130 (FIG. 7A) is coupled to the upper conductive pad 730 in some embodiments, or the upper conductive pad 730 may be omitted and the conductive bump 130 may be coupled directly to the first diode 710 and second diode 720. A via 170 (FIG. 7A) is coupled to each of the first lower conductive pad 760 and the second lower conductive pad 770.

The first diode 710 and second diode 720 are oriented to comprise opposing biasing schemes, such that the first diode 710 may be biased in a first direction and the second diode 720 may be biased in a second, opposing direction. For example, the first diode 710 may be forward biased (i.e., allows a positive current to pass through and blocks a current of the opposite polarity) while the second diode 720 may be reverse biased (i.e., blocks a positive current and allows a current of the opposite polarity to pass). In this configuration, a positive current through the conductive bump 130 will pass through the first diode 710 and the first lower conductive pad 760, enabling access to the circuitry 140 coupled with first lower conductive pad 760 and the associated via 170. The positive current is blocked by the second diode 720. Likewise, a current in the opposite polarity through the conductive bump 130 will pass through the second diode 720 and the second lower conductive pad 770, enabling access to the circuitry 140 coupled with the second lower conductive pad 770 and the associated via 170. The current in the opposite polarity is blocked by the first diode 710.

The first and second diodes 710, 720, respectively, may comprise any suitable structure or stack which is known to those of ordinary skill in the art. By way of example and not limitation, the diodes may comprise crystalline silicon NP, or PN, structures, metal/double-insulator/metal diodes, filamentary structures that exhibit

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rectifying abilities, such as silver/amorphous silicon/p-type silicon stacks, as well as any other stack or structure having rectification features.

The bond pads 750 may be disposed on the surface 160 of the first substrate 110 comprising any one of a variety of patterns, such as those described
5 above with relation to FIGS. 2-6. FIG. 8 illustrates a top view the first substrate 110 comprising bond pads 750 patterned according to at least one embodiment. According to at least some of such embodiments, the vias 170 may be coupled to the center, or at least substantially the center, of the respective lower conductive pads 760, 770 (FIG. 7B) associated with each bond pad 750, and the vias 170 may be coupled to the
10 circuitry 140 according to a predefined pattern. In the embodiment of FIG. 8, the vias 170 of each bond pad 750 are positioned in a pattern wherein each via is coupled to a conductive trace immediately adjacent to the conductive trace to which the via 170 above and below (as oriented in FIG. 8) are coupled. The bond pads 150 are, therefore, shifted in accordance with the pattern of the vias 170.

15 In at least some embodiments, the electronic device 100, 700 may comprise a memory device. In such embodiments, at least a portion of the circuitry 140 of the first substrate 110 may comprise a plurality of memory cells and at least a portion of the circuitry 125 of the second substrate 120 may comprise support circuitry (e.g., charge pumps, decode and addressing, sense amplifiers, I/O circuits, etc.). By way of example
20 and not limitation, in some embodiments, at least a portion of the circuitry 140 may comprise one or more magnetic shift registers 180, such as those disclosed in each of U.S. Patent Nos. 7,236,386, 6,920,062, 6,898,132 and 6,834,005. Such a magnetic shift register 180 comprises a fine track of ferromagnetic or ferrimagnetic material which can be magnetized in small sections or regions, which may also be characterized
25 as domains 185, in one direction or another. Thus, information is stored in the domains 185 in the track. An electrical current may be applied to the magnetic shift register track to move the magnetic moments within the domains 185 along the track, and past magnetic tunneling junctions or the writing elements 190. The direction of the current controls the direction of the movement along the track of the magnetic
30 moments within the domains 185.

This magnetic shift register track may be disposed in the first substrate 110 comprising a nanoscale pitch. The magnetic shift register 180 may have any of a

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variety of shapes, including but not limited to, serpentine, straight, U-shaped, or otherwise, as well as combinations thereof. The vias 170 positioned to extend from adjacent a portion of the magnetic shift register 180 to the bond pads 150 may be configured as magnetic tunneling junctions 190 (as depicted in the leftmost via in
5 FIG. 1), writing elements, or similar devices, as well as combinations thereof.

A conventional magnetic tunneling junction (MTJ) generally comprises two layers of magnetic material separated by a thin layer of insulating material which comprises a tunneling barrier. The tunneling barrier is typically formed from an ultra thin layer of aluminum oxide, although it can also be formed from other insulating or
10 semiconducting materials. One magnetic layer in the MTJ is typically a hard magnetic material that requires a large magnetic field to change its magnetization. The other magnetic material is typically a soft magnetic material, allowing a weak magnetic field to change its magnetization. When a small magnetic field is applied to the soft magnetic material, its direction of magnetization changes so that the direction of the
15 magnetization of the soft magnetic layer can be varied relative to that of the hard magnetic material.

The magnitude of the current passed through the tunneling barrier depends on the relative magnetic orientation of the two magnetic materials in the tunneling junction. Consequently, the value of the current in the tunneling junction indicates the
20 direction of the magnetic moment in the soft magnetic material if the moment of the hard layer is known or the current in the tunneling junction indicates the direction of the moment of the hard magnetic material if the direction of the moment of the soft magnetic material is known.

The two magnetic materials in the magnetic tunneling junction can also be
25 formed from hard magnetic materials if means for independently switching the magnetic moments in the MTJ are provided. The tunneling current passing through the MTJ allows the direction of the magnetic moment of either one of the two magnetic materials in the MTJ, i.e., the storage or sensing layer, to be determined if the direction of the magnetic moment of the other material, i.e., the reference layer, is known.

30 Embodiments of electronic devices of the present disclosure may be formed by separately forming the first substrate 110 and the second substrate 120. In at least some embodiments, first substrate 110 and the second substrate 120 may be processed

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at different temperatures. The circuitry 140 may be disposed in the first substrate 110. As set forth herein above, the circuitry 140 of the first substrate 110 may comprise conductive traces, including memory cells comprising one or more magnetic shift registers 180 in the form of tracks disposed into the first substrate 110. Such
5 circuitry 140, such as magnetic shift registers 180, may be formed comprising nanoscale electronic components, nanoscale pitch, or both. The support circuitry 125 of the second substrate 120 may comprise conventional CMOS circuitry and may comprise substantially larger (e.g., microscale) electronic components, pitch, or both. The conventional CMOS circuitry may be formed according to conventional
10 fabrication techniques and processes known to those of ordinary skill in the art.

In at least some embodiments, the circuitry 140 of the first substrate 110 may experience performance degradation at lower temperatures than the temperatures employed to process the second substrate 120. Therefore, the circuitry 140 of the first substrate 110 may be formed at temperatures substantially lower than the temperatures
15 employed for forming circuitry disposed in the second substrate 120. For example, in embodiments in which the circuitry 140 of the first substrate 110 comprises magnetic shift registers 180, the circuitry 140 of the first substrate 110 may experience performance degradation when exposed to temperatures of about 450° C or more. The support circuitry 125 of the second substrate 120 may comprise conventional CMOS
20 circuitry formed with conventional Front-End-Of-Line (FEOL) or Back-End-Of-Line (BEOL) CMOS processing. Conventional FEOL processes may employ temperatures as high as about 1,000° C to 1,100° C, or higher, while conventional BEOL processes may employ temperatures as high as about 450° C.

A plurality of vias 170 may be formed in a portion of the first substrate 110, the
25 vias 170 extending from the surface 160 to adjacent the circuitry 140. The vias 170 may be formed using conventional techniques, such as laser ablation, wet or dry etching, or other suitable methods. As set forth herein above, in at least some embodiments, the vias 170 may be formed to comprise a magnetic tunneling junction, as is known to those of ordinary skill in the art.

30 The bond pads 150, 750 may be disposed on the surface 160 of the first substrate 110 by blanket deposition followed by selective etching using lithography, or other suitable methods, and the first substrate 110 may be bonded to the second

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substrate 120 using a plurality of conductive bumps 130 coupled to the second substrate 120 and the bond pads 150, 750 of the first substrate 110. The bond pads 150, 750 may be patterned on the surface 160 according to any suitable pattern, including without limitation any of the patterns described herein above with relation to
5 FIGS. 2-6, and 8.

In at least some embodiments, as illustrated in FIGS. 7A-7B, the bond pads 150 may be formed comprising a selection device formed therein. Such embodiments may include forming a first lower conductive pad 760 coupled to a first via 170 and a second lower conductive pad 770 coupled to a second via 170. The first and second
10 lower conductive pads 760, 770 may be formed by comprising a gap 780 therebetween by blanket deposition followed by etching using lithography, or other suitable methods known to those of ordinary skill in the art. A first diode 710 may be formed on the first lower conductive pad 760 biased in a first direction and a second diode 720 may be formed on the second lower conductive pad 770 and biased in a second, opposing
15 direction. The first and second diodes 710, 720 may be formed by conventional processing techniques known to those of ordinary skill in the art. By way of example and not limitation, the first diode 710 may be formed by depositing a diode stack in a first polarity, and then etching the diode stack so the stack only occupies the area of the first lower conductive pad 760. The first diode 710 may then be covered with a
20 conventional etch stop according to the stack materials and a second diode stack may be deposited in the second, opposite polarity to form the second diode 720. In at least some embodiments, an upper conductive pad 730 may be formed over both the first diode 710 and the second diode 720.

The first substrate 110 and related nanoscale circuitry 140 may, therefore, be
25 formed separate from the second substrate 120 and any related microscale circuitry 125 thereon, and the circuitry 140 of the first substrate 110 may be coupled to the circuitry of the second substrate 120 with the plurality of conductive bumps 130, which may be formed on the bond pads 150. Because the circuitry 125 on the second substrate 120 may be formed on a larger scale, such circuitry 125 may be formed more efficiently
30 and at a significantly lower cost, while the circuitry 140 of the first substrate 110 may be formed on a smaller scale to increase performance (e.g., increased storage capacity, etc.). The second substrate 120 may then be bonded to the first substrate 110, and the

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circuitry 125 of the second substrate 120 coupled to the circuitry 140 of the first substrate 110 to combine the circuitry of both substrates into a single device. In such embodiments, the first substrate 110 and circuitry 140 may be formed at lower temperatures than the temperatures employed in forming the second substrate 120 and any related circuitry 125, such as the support circuitry.

Additional embodiments of the present disclosure are directed to electronic systems. As shown in FIG. 9, an electronic system 900, such as a computer system, in accordance with an embodiment of the present invention, comprises at least one input device 910, at least one output device 920, at least one processor 930, and at least one memory device 940. As used herein, the term "computer system" includes not only computers such as personal computers and servers, but also wireless communications devices (e.g., cell phones, personal digital assistants configured for text messaging and email, etc.), cameras, chip sets, set top boxes, controllers, vehicle and engine control and sensor systems, digital music players, and other combinations of the above-referenced input, output, processor and memory devices. The at least one memory device 940 may comprise at least one memory device (e.g., devices 100, 700 in FIGS. 1 and 7A) comprising a first substrate coupled to a second substrate.

The first substrate may include circuitry comprising, by way of non-limiting example, a plurality of magnetic tracks comprising a plurality of domains, a plurality of magnetic tunneling junctions proximate to the plurality of magnetic tracks and extending to a location adjacent a surface of the first substrate, and a plurality of bond pads on the surface of the first substrate, each bond pad of the plurality of bond pads electrically coupled to a magnetic tunneling junction of the plurality of magnetic tunneling junctions.

The second substrate comprises support circuitry and is coupled to the plurality of bond pads on the surface of the first substrate with a plurality of conductive bumps. The support circuitry may comprise one or more of a charge pump, a decode and addressing circuit, a sense amplifier and an I/O circuit.

While certain embodiments have been described and shown in the accompanying drawings, such embodiments are merely illustrative and not restrictive of the scope of the invention, and this invention is not limited to the specific constructions and arrangements shown and described, since various other additions and

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modifications to, and deletions from, the described embodiments will be apparent to one of ordinary skill in the art. Thus, the scope of the invention is only limited by the literal language, and legal equivalents, of the claims which follow.

CLAIMS:

1. An electronic device, comprising:
a first substrate comprising circuitry including a plurality of conductive traces extending at least
5 substantially parallel to each other through a portion of the first substrate, a plurality of
bond pads positioned on a surface of the first substrate and comprising a width
extending over at least two of the plurality of conductive traces, and a plurality of vias
extending from adjacent at least some conductive traces of the plurality of conductive
traces to bond pads of the plurality of bond pads; and
10 a second substrate bonded to the first substrate, the second substrate comprising circuitry
coupled to the plurality of bond pads on the first substrate with a plurality of conductive
bumps.
2. The electronic device of claim 1, wherein the plurality of conductive traces
15 comprises a plurality of magnetic shift registers comprising a plurality of domains, and the
plurality of vias comprises a plurality of magnetic tunneling junctions.
3. The electronic device of claim 1, wherein the circuitry of the second substrate
comprises at least one of a charge pump, a decode and addressing circuit, a sense amplifier
20 and an I/O circuit.
4. The electronic device of claim 1, wherein the plurality of conductive traces is
disposed at a pitch of less than 100 nanometers, and wherein each bond pad of the plurality of
bond pads comprises an area of $2,000\text{ }\mu\text{m}^2$ or greater.
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5. The electronic device of claim 1, wherein at least one bond pad of the plurality
of bond pads comprises:
a first diode biased in a first direction and adjacent to an upper conductive pad and a first lower
conductive pad, the first lower conductive pad coupled to a via of the plurality of vias;
30 and
a second diode biased in a second, opposing direction and adjacent to the upper conductive
pad and a second lower conductive pad, the second lower conductive pad coupled to
another via of the plurality of vias.
6. The electronic device of claim 1, wherein:
the plurality of bond pads is positioned in a pattern on the surface of the first substrate
comprising one of a bond raster pattern and a bond shift pattern; and
the bond pads comprise at least one shape selected from the group consisting of square,
35 rectangular, hexagonal and triangular.

7. A memory device comprising a first substrate, the first substrate comprising:
a plurality of magnetic tracks comprising a plurality of domains;
a plurality of magnetic tunneling junctions proximate to the plurality of magnetic tracks and
5 extending to a location adjacent a surface of the first substrate; and
a plurality of bond pads on the surface of the first substrate, each bond pad of the plurality of
bond pads electrically coupled to a magnetic tunneling junction of the plurality of
magnetic tunneling junctions.
- 10 8. The memory device of claim 7, further comprising a second substrate
comprising support circuitry, the second substrate being bonded to the plurality of bond pads
with a plurality of conductive bumps.
- 15 9. The memory device of claim 8, wherein the support circuitry of the second
substrate comprises at least one of a charge pump, a decode and addressing circuit, a sense
amplifier and an I/O circuit.
- 20 10. The memory device of claim 7, wherein at least one bond pad of the plurality
of bond pads comprises:
an upper conductive pad coupled to a first diode and a second diode, the first diode being
biased in a direction opposite to the bias of the second diode;
a first lower conductive pad coupled to the first diode and to a via of a plurality of vias; and
a second lower conductive pad coupled to the second diode and to another via of the plurality
of vias.
- 25 11. The memory device of claim 7, wherein bond pads of the plurality of bond
pads comprise a width extending over at least two magnetic tracks of the plurality of magnetic
tracks.
- 30 12. The memory device of claim 7, wherein the bond pads are configured to
comprise a shape consisting of at least one of square, rectangular, hexagonal, and triangular.
- 35 13. A method of forming an electronic device, comprising:
forming a first substrate comprising a plurality of conductive traces extending through a portion
thereof, a plurality of vias extending from adjacent at least some conductive traces of
the plurality of conductive traces to a surface of the first substrate, and a plurality of
bond pads on the surface of the first substrate and adjacent to a via of the plurality of
vias, each bond pad of the plurality of bond pads comprising a width extending over at
least two conductive traces of the plurality of conductive traces;

forming a second substrate comprising circuitry; and
 attaching a second substrate to the first substrate with a plurality of conductive bumps coupled
 to the plurality of bond pads on the first surface of the first substrate and to the circuitry
 of the second substrate.

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14. The method of claim 13, wherein forming the first substrate further comprises:
 forming the plurality of conductive traces as a plurality of magnetic shift registers, each
 magnetic shift register comprising a plurality of domains; and
 forming the plurality of vias configured as magnetic tunneling junctions.

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15. The method of claim 14, wherein forming the first substrate comprises forming
 the first substrate at a temperature below about 450° C, and wherein forming the second
 substrate comprises forming the second substrate at a temperature above about 450° C.

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16. The method of claim 13, wherein forming the first substrate comprising the
 plurality of bond pads on the surface of the first substrate comprises forming the plurality of
 bond pads comprising at least one shape selected from the group of shapes consisting of
 square, rectangular, hexagonal and triangular.

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17. The method of claim 13, wherein forming the first substrate comprising the
 plurality of bond pads on the surface of the first substrate comprises positioning the plurality of
 bond pads on the surface of the first substrate in a pattern comprising one of a bond raster
 pattern and a bond shift pattern.

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18. The method of claim 13, wherein forming the first substrate comprising the
 plurality of bond pads on the surface of the first substrate comprises:

disposing a first lower conductive pad coupled to a via of the plurality of vias;

disposing a second lower conductive pad coupled to another via of the plurality of vias;

disposing a first diode biased in a first direction on the first lower conductive pad;

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disposing a second diode biased in a second, opposite direction on the second lower
 conductive pad; and

disposing an upper conductive pad over the first diode and the second diode.

19. A method of forming a memory device, comprising:
forming a plurality of conductive traces in a first substrate, the plurality of conductive traces
configured as magnetic shift registers comprising a plurality of domains;
forming a plurality of vias comprising magnetic tunneling junctions extending from a surface of
5 the first substrate to proximate the plurality of magnetic shift registers; and
forming a plurality of bond pads, each bond pad of the plurality of bond pads coupled to a via of
the plurality of vias.

20. The method of claim 19, further comprising:
10 forming support circuitry in a second substrate; and
coupling the support circuitry in the second substrate to the plurality of bond pads of the first
substrate with a plurality of conductive bumps.

21. The method of claim 20, wherein forming the support circuitry in the second
15 substrate comprises forming at least one of a charge pump, a decode and addressing circuit, a
sense amplifier, and an I/O circuit.

22. The method of claim 19, wherein forming the plurality of bond pads comprises
patterning the plurality of bond pads to comprise one of a bond raster pattern and a bond shift
20 pattern.

23. The method of claim 19, wherein forming the plurality of bond pads comprises
configuring the plurality of bond pads with at least one shape selected from the list consisting of
square, rectangular, hexagonal and triangular.

24. The method of claim 19, wherein forming the plurality of bond pads comprises
forming a plurality of bond pads, each comprising:
a first diode biased in a first direction coupled to a first lower conductive pad in electrical contact
with a via of the plurality of vias;
25 a second diode biased in a second, opposite direction coupled to a second lower conductive
30 pad in electrical contact with another via of the plurality of vias; and
an upper conductive pad coupled to the first diode and to the second diode.

25. A system, comprising:
at least one processor; and
at least one memory device coupled to the processor, the at least one memory device comprising:
- 5 a first substrate comprising a plurality of magnetic tracks including a plurality of domains, a plurality of magnetic tunneling junctions proximate to the plurality of magnetic tracks and extending to a location adjacent a surface of the first substrate, and a plurality of bond pads on the surface of the first substrate, each bond pad of the plurality of bond pads electrically coupled to a magnetic
- 10 tunneling junction of the plurality of magnetic tunneling junctions; and
a second substrate comprising support circuitry, the second substrate bonded to the plurality of bond pads with a plurality of conductive bumps.