# SPLIT GATE MEMORY CELL

## Related Applications

This Application claims the benefit of U.S. Provisional Application No. 06/115,602, filed 01/12/99.

## Field Of The Invention.

The present invention relates to a memory cell and more particularly a split gate memory cell useful for low voltage operation.

## Description Of The Prior Art.

As device technology scales down, doping concentrations in devices keep increasing. The resultant decrease in oxide/junction breakdown voltage makes it difficult to utilize high voltages required for the operation of non-volatile (NV) memory cells. Further, in the select gate of a split-gate memory cell itself, one needs relatively thicker gate oxides to prevent oxide breakdown. This makes it difficult to scale the $V_t$'s of the select gate device and thus leads to poorer low voltage operation.

Scientists at Samsung Corp. have proposed the idea of a built-in charge pump for use in stacked gate cells (termed Boosted wordline cell) in an effort to address the aforementioned problems. The cells proposed by Samsung require the use of a triple poly structure. The present invention addresses the aforementioned problems through the use of a novel cell have a two-poly structure.

## Summary Of The Invention

The present invention comprises a novel split gate memory cell and its method of operation.

The novel split gate cell comprises a silicon substrate having a tunnel oxide layer on a portion of its surface and a first control gate and a floating gate electrode spaced from each other and preferably formed from the same material over the tunnel oxide. A dielectric layer overlies the first control gate and the floating gate electrodes, including the surface of the electrodes in the area between them. A second control gate, which is physically separated from the first control gate is provide over the dielectric layer and in the space between the first

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control gate and the floating gate. A highly doped region may be provided in the silicon substrate in the region under the separation of the first control gate and the floating gate. Source and drain regions are also provided in the substrate with optional halo-implants adjacent thereto.

The novel memory cell is fabricated by providing a tunnel oxide layer on the surface of a silicon substrate; forming a conductive layer over the tunnel oxide; forming a space in the conductive layer so as to provide a control gate and a floating gate electrode separated from each other but made from the same deposited or grown layer; forming a highly doped region in the substrate below the space between the aforementioned electrodes; forming a dielectric layer over the surfaces of the aforementioned electrodes; and forming a second control gate over the dielectric layer.

In operation, the novel device can operate at lower voltages than conventional split gate memory cells. The device is programmed by first applying a voltage to the second control gate, electrically floating the node second control gate and the applying a voltage to the first control gate. Due to a coupling between control gates, the voltage on the second control gate is automatically increased upon application of a voltage to the first control gate. The drain may then be pulsed to initiate hot carrier injection into the floating gate or a small charge pump may be provided to generate higher voltages. In the erase mode, erasure can be accomplished with the first control gate open and and the second control gate held at a negative voltage with a positive drain voltage. Alternatively, one can erase utilizing a low voltage charge pump from the coupling between the control gates but using a negative voltage. Further, erase can be accomplished by a channel erase process. During the Read operation, both of the control gates are brought to the wordline voltage.

**Brief Description Of The Drawings**

Figure 1 is a sectional view of a conventional prior art split gate cell.

Figure 2 is a sectional view of an embodiment of the cell of the present invention.

Figures 3-5 are sectional views illustrating the steps for fabricating the novel cell.

Figures 6-8 are sectional views directed to the fabrication of a small space between the floating gate poly storage node and the floating gate poly of control gate 1.

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## Detailed Description Of The Invention

Definitions: As used herein, including the drawings, FG is a storage node made of floating gate polysilicon or other conductor; CG-1 is a control gate also made from polysilicon or other appropriate conductor; and CG-2 is a control gate made of polysilicon, which may be silicided, or other conductor. The FG and CG-1 layers are sometimes referred to as poly-1 since they are formed from the same deposited or grown layer (poly-1). The CG-2 gate is sometimes referred to as poly-2 as it is formed from a deposited layer designated as poly-2. Polysilicon is preferred over other conductors for both the poly-1 and poly-2 layers.

As can be seen with reference to Figs. 3-5, the process for making the novel device 10 includes the growth of a tunnel oxide 12 on a silicon substrate 14 after conventional IC isolation and active area definition steps have been finished. Typically, the thickness of the tunnel oxide is from 50-150A and preferably between about 80-100A. An in-situ doped polysilicon layer, poly-1, (or other conductor) 16 is then deposited. The poly-1 is then patterned by means of a thick gate photoresist (PR-1), as shown in Fig 3A and the device is etched to form the individual, separated FG and CG-1 structures as shown in Fig. 3B. Although not necessary for the operation of the device, one can, using oxide or other dielectric spacers, easily define a very small space (~0.1 μm) between the FG and CG-1 poly-1.

An optional $N^+$ ion implant 18 in the silicon wafer substrate 14 in the region of the separation between CG-1 and FG (see Fig. 3B) is preferably performed. The resist, PR-1, used for implantation is removed, the tunnel oxide etched, and an interpoly dielectric layer 20 is deposited on the wafers to isolate the poly-1 CG-1 and FG structures from the subsequently deposited poly-2 layer 22. The interpoly dielectric layer 20 can be made of silicon dioxide , an ONO (oxide/nitride/oxide) composite or a known high K dielectric to achieve the necessary coupling. Typically, the interpoly layer 20 is from 50-300A thick and and generally about 180A thick for a silicon oxide layer. It should be noted that the thickness of the interpoly layer 20 depends upon the material employed for that layer. Optionally, using a photoresist, the dielectric may be removed from selected areas where a gate-dielectric thinner than the high voltage dielectric may be needed, e.g. for embedded applications, analogous to the thick gate operation. As can be seen with reference to Figs. 4A and 4B, a disposable hard mask 24 is deposited over the poly-2 layer 22. A gate photoresist, PR-2, is then deposited over the hard mask 24 so as to define the width of the split gate cell and the device is etched, stopping after the poly-2 layer 22. The core CMOS area is protected with a photoresist (not shown), and the

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memory cell area is opened for a gate stack etch. First the interpoly dielectric layer 20 and then the FG and CG-1 poly-1 layers 16 are etched, stopping at the tunnel oxide 12 (Fig. 5A).

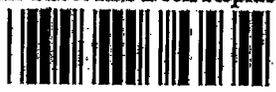
A source/drain halo ion implant 26 is then implanted, followed by a heavy dose source/drain arsenic ion implant 28 resulting in the structure shown in Fig. 5B. Boron, boron fluoride or any other P-type dopant, implanted preferably with a large tilt angle can be used for the drain halo implant 26. Where desired, by adding another mask, one can easily make an asymmetric device with, for example, a halo implant in the drain end only. Such asymmetric device generally exhibits a higher read current and has a higher speed as compared with the symmetrical device depicted in the Figures. Next, conventional core CMOS processing is completed, and the hard-mask 24 is removed as part of the core CMOS process to arrive at the novel device represented by Fig. 2. With contacts open to drain, source, CG-1 and CG-2, the device may be used as a NVRAM for low voltage operation. Also, it may be noted that the process sequence allows one to use thicker oxides, formed by the composite of deposited HTO and grown oxide, for use in high voltage devices.

A preferred process for making a small space between FG and CG-1 is shown with reference to Figs. 6-8. The process comprises growing the tunnel oxide 12, depositing the poly-1 layer16, depositing a thin undoped silicon oxide dopant mask layer 30 followed by the deposition of a disposable doped oxide layer 32, e.g. a boron-phosphorous silicate glass (BPTEOS). A patterned photoresist layer 34 is provided and the device is etched removing the exposed portion of the doped oxide layer 32 and undoped oxide mask layer 30 stopping at poly-1. This results in the structure shown in Fig. 6. The photoresist 34 is then removed, the surface is cleaned and a disposable oxide dopant mask 36 is grown/deposited. A BPTEOS spacer oxide 38 is deposited and a timed spacer etch is performed to reach the structure of Fig. 7. Finally, the poly-1 layer 16 is etched to form the separated CG-1 and FG areas. As previously indicated and as shown in Fig. 8, a N-type dopant (e.g. AS) is implanted in the space between the CG-1 and FG areas. Thereafter, the disposable oxide is etched away in an ammonium hydroxide/hydrogen peroxide bath. Device formation may then proceed essentially as described above with reference to Figs. 4A, 4B ,5A and 5B.

Device Operation.

In a conventional prior art split gate device as shown in Fig. 1, the control gates, CG-1 and CG-2, are made of the same polysilicon and are physically connected. Also, the thickness of the tunneling oxides under the FG and CG gates are generally different, making fabrication

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more complex. In operation of the prior art device, one needs to apply a large voltage (~7.5V) on the control gate to achieve programming in a short time (~a few 10's of μs). This however does not allow one to scale the underlying select-gate oxide. In the present invention, the voltage on CG-1 can be limited to ~5V so that one can use the tunnel oxide as the gate of the select-gate oxide. The coupling ratio between the CG-2 and the CG-1 can be high, e.g. ~0.6, which is approximately similar to the coupling between CG-2 and FG.

PROGRAMMING OF THE DEVICE In order to program the novel device, a voltage is first applied to CG-2 (e.g. ~5.0V). Then the node CG-2 is electrically floated and the voltage on CG-1 is brought up, e.g. to ~5V. The coupling between CG-1 and CG-2 is about 0.6 so the voltage on CG-2 is increased to ~8V. Next the drain may be pulsed to initiate hot carrier generation and injection into the FG. Thus , the built in voltage boost on CG-2 allows one to achieve device programming even when power supplies are limited to lower voltages.

Another advantage of using the structure of this invention is that the vertical field in the injection region can be independent of the select-gate voltage. Thus, if one chooses, one can apply a large voltage to CG-2 to increase the vertical field and at the same time apply a small voltage to CG-1 to limit programming current and thus improve injection efficiency, as is done in source side injection cells. Such a programming scheme allows one to conserve power in low power applications.

ERASURE: In a conventional split gate device, during erase a large negative voltage is applied to CG-2 and the drain is held at a large positive voltage. Such a scheme is also possible in the structure of the present invention. With CG-1 open and CG-2 at a negative voltage a positive drain voltage can duplicate the erase of a conventional split gate cell. However, the present cell offers the option of using a lower voltage charge pump and using the built-in charge pump for erase, in a manner analogous to programming but with negative voltages.

Further, in conventional split-gate cells, such as that shown in Figure 1, channel erase is difficult to achieve due to the large coupling ratio between the substrate and FG. Due to this coupling one needs very large substrate voltages, e.g. >15V, to initiate tunneling from the floating gate to the substrate. This voltage appears across the select gate oxide and in order to prevent dielectric breakdown, thicker oxides than those required in the device of the present invention would be required. However, such thicker oxides degrade device performance. In contrast, one can readily utilize a channel erase in the present invention. Here, even if 15 volts

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is applied to the substrate, one can hold CG1 at 7.5V, with CG2 at 0V and thus the fields across the oxides in the select gate region is <7.5V in all cases.

READ: Read of the devices can follow in a normal fashion with the exception that during read, both CG-1 and CG-2 are brought up to the wordline voltage. The effective capacitance of the wordline is thus similar in value to what it would be for a conventional split gate device (with a thinner gate oxide). With a thinner select-gate oxide (cf. to a conventional split gate cell), a higher on-current and thus a higher read speed is to be expected.

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## Claims

1. A semiconductor device comprising a p-type silicon substrate having a tunnel oxide on its surface, an n+-type source and an n+-type drain separated from each other and implanted in said substrate, and on said substrate between said source and drain and over said tunnel oxide, a floating gate polysilicon storage node and a first polysilicon control gate separated from the floating gate storage node on said tunnel oxide, a second polysilicon control gate between and over the polysilicon control gate and the floating gate and isolated therefrom by a dielectric layer.

2. The semiconductor device recited in claim 1 further including a n+-type implant in the substrate in the region under the separation between the floating gate and the first control gate.

3. A split gate memory cell comprising a silicon substrate, a tunnel oxide layer on said substrate, a first control gate and a floating gate over said tunnel oxide, said first control gate and said floating gate being separated from each other by a space, a dielectric layer over the surfaces of said first control gate and floating gate, a second control gate over the dielectric layer and extending within said space, and separated source and drain regions in said substrate adjacent the first control gate and floating gate.

4. The split gate memory cell recited in claim 3 further including a highly doped region in said substrate under said space, of opposite conductivity type from the substrate.

5. The split gate memory cell recited in claim 3 wherein said space is in the order of 0.1 microns.

6. The split gate memory cell recited in claim 3 wherein the first control gate and floating gate are formed from the same conductive layer.

7. The split gate memory cell recited in claim 6 wherein said first control gate and floating gate comprise polysilicon.

8. The split gate memory cell recited in claim 7 wherein said second control gate comprises a member of the group consisting of polysilicon and a silicided polysilicon.

9. The split gate memory cell recited in claim 8 wherein said dielectric layer comprises at least one member of the group consisting of silicon dioxide, an oxide/nitride/oxide composite and a high k dielectric material.

10. A split gate memory cell comprises a silicon substrate having a silicon dioxide tunnel layer thereon, a first control gate electrode and a floating gate electrode spaced from said first control gate electrode overlying said tunnel layer and comprised of polysilicon, a dielectric layer over the surface of said first control gate and said floating gate electrodes, and a second control gate electrode comprised of a polysilicon over said dielectric layer on both the first control gate and floating gate electrodes and in said space between said electrodes.

11. The split gate memory cell recited in claim 10 further comprising an $n^+$ doped region in the substrate under said space.

12. A split gate memory cell comprising a first and a second control gate and a floating gate, said gates isolated one from the other by a dielectric layer and said first control gate and said floating gate being on the same plane and having a space therebetween and overlying a tunnel oxide layer.

13. The split gate memory cell recited in claim 12 wherein said substrate has a highly doped region under said space.

14. A method of programming a split gate memory cell of the type set forth in claim 3 comprising applying a voltage of a first polarity across the second control gate, electrically floating said floating gate, applying a voltage of the first polarity to the first control gate to cause the voltage on the second control gate to increase due to coupling between said control gates, and initiating hot carrier generation and injection into said floating gate.

15. The method recited in claim 14 wherein the magnitude of the voltages applied to the first and second control gates are approximately the same.

16. The method recited in claim 14 wherein the voltage applied to the second control gate is greater than the voltage applied to the first control gate.

17. A method of erasing data stored in a split gate memory cell of the type claimed claim 3 comprising applying a drain voltage of a first polarity and a voltage of opposite polarity to the second control gate while the first control gate is open.

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18. The method of erasing data stored in a split gate memory cell of the type set forth claim 3 comprising the steps set forth in claim 14 for programming, but applying voltages to the control gates of opposite polarity from that used for programming.

19. A method of reading data stored in a split gate memory cell of the type recited claim 3 including the step of bringing the voltage of both the first and second control gates to wordline voltage.

20. The device recited in claim 4 wherein the source and drain regions are n+-type regions and further including at least one p+-type halo-implant region in the substrate adjacent at least one of said regions.

21. The device recited in claim 20 further including a halo implant adjacent both the source and drain regions.

22. The device recited in claim 20 wherein there is a halo-implant adjacent the drain region, but not the source region of the device.

23. A channel erase method for erasing data stored in a split-gate memory cell of the type set forth in claim 3 comprising applying a first voltage to the substrate, holding the voltage to the first control gate at about half of the voltage applied to the substrate and the voltage of the second control gate at or about zero volts such that the fields across the oxides in the select gate region are less than 7.5 mv/cm.

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