REDUCED LEAKAGE DRAM MEMORY CELLS WITH VERTICALLY ORIENTED NANORODS AND MANUFACTURING METHODS THEREOF

RELATED APPLICATION

This patent application claims priority benefit from U.S. Application No. 11/524,343 filed 20 September 2006 which is incorporated herein by reference.

TECHNICAL FIELD

The information disclosed herein relates generally to embodiments of semiconductor devices, including memory cells.

BACKGROUND

The semiconductor device industry has a market-driven need to reduce the size of devices used, for example, in dynamic random access memories (DRAMs) that are found in computers and mobile communications systems. Currently, the industry relies on the ability to reduce or scale the dimensions of its basic devices to increase device density. This includes scaling the channel length of the metal oxide semiconductor field effect transistor (MOSFET). Increased channel scaling of the MOSFET can lower the channel resistance. Consequently, channel leakage currents may increase. This relationship has made the present MOSFET channel design less useful for providing increasingly smaller memory cells, and thus, there is a need to find other mechanisms to generate reduced cell geometry.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, which are not necessarily drawn to scale, like numerals describe substantially similar components throughout the several views. Like numerals having different letter suffixes represent different instances of substantially similar components. The drawings illustrate generally, by way of example, but not by way of limitation, various embodiments discussed in this document.

FIG. 1A-C are cross-sections illustrating nanorod formation according to various embodiments of the invention.

FIG. 1D is a perspective view of nanorods according to various embodiments of the invention.

FIG. 2A-B are cross-sections illustrating a MOSFET according to various embodiments of the invention.

FIG. 3 is a surface view illustrating a MOSFET according to various embodiments of the invention.

FIG. 4 is a cross-section illustrating a memory cell according to various embodiments of the invention.

FIG. 5 is block diagram of a memory device according to various embodiments of the invention

FIG. 6 illustrates a semiconductor wafer according to various embodiments of the invention.

FIG. 7 illustrates a circuit module according to various embodiments of the invention.

FIG. 8 is a block diagram illustrating a circuit module as a memory module according to various embodiments of the invention.

FIG. 9 is a block diagram illustrating an electronic system according to various embodiments of the invention.

FIG. 10 is a block diagram illustrating an electronic system as a memory system according to various embodiments of the invention.

FIG. 11 is a block diagram illustrating an electronic system as a computer system according to various embodiments of the invention.

DETAILED DESCRIPTION

One approach to increasing the on-chip storage capacity of a semiconductor is to increase the number of capacitor cells per unit area, which generally means reducing the overall size of the capacitor. However, reducing capacitor size may result in a lower capacitance per cell. If the lower cell capacitance means more capacitive elements are needed to maintain or improve upon a performance characteristic, such as the ability to maintain a storage charge over time, then any gain in capacitor density may be offset. The double-sided capacitor provides one useful device structure for increasing capacitance without a commensurate increase in area. A double-sided capacitor may be

scaled smaller, for example, by increasing the dielectric constant of the insulator material separating the capacitor plates.

A double-sided capacitor used for a DRAM memory cell is typically coupled to an access transistor located in close proximity. For performance reasons and to maximize cell density, the access transistor and the double-sided capacitor may be formed in a stacked capacitor-transistor arrangement. A continued reduction in the size of the double-sided capacitor for such an arrangement then, may involve further reduction (or scaling) in the access transistor. In the case of a MOSFET, scaling smaller typically means reducing the channel length as well as channel width, which may lead to lower drain-source resistance (r_{ds}). Lower r_{ds}, may allow higher off-state leakage currents to flow between the drain and source. A lower r_{ds} may result from an increase in the channel conduction due to a short channel effect such as drain induced barrier lowering (DIBL). Near the channel inversion threshold, a potential barrier may be formed between the source and the channel blocking drain current flow. The application of a drain voltage may decrease the potential barrier height between the source and channel, increasing the drain current at near and below threshold. The drain current may therefore be due to the drain voltage as well as the gate voltage, effectively reducing r_{ds} at near or below the inversion threshold. A higher gate leakage current may also occur at shorter channel lengths due to the higher gate electric fields. Many embodiments of the invention may operate to reduce the leakage currents as the channel length is reduced.

The bulk (or native) band gap energy of a semiconductor material is the energy separation between the conduction and valance bands having a three dimensional continuum of energy states. A semiconductor material with a three dimensional continuum of energy states does not, generally, exhibit substantial quantum size effects such as discrete energy levels, spin-orbit splitting of heavy and light hole bands and changes in band gap separation. Quantum size effects may be introduced by altering a crystal's dimensions. A change in the physical dimensions of a single crystal semiconductor material does not generally change the bulk band gap energy of the material, if all three crystal dimensions are sufficiently large. Conversely, reducing the size of a semiconductor material

may cause the band gap energy of the material to increase or shift to higher energy, if at least one of the three crystal dimensions is made sufficiently small. For example, a rod shaped from semiconductor material may cause the energy band gap of the material to increase above its bulk band gap energy state as the diameter or the length of the rod is reduced. The change in the energy band gap of a rod-shaped material caused by its small dimensions may be exploited. A rod with a diameter on the order of a nanometer may be termed a "nanorod".

In many embodiments, vertical transistor channels are formed using one or more semiconductor nanorods oriented substantially perpendicular to a surface of a substrate. In some cases, the channels comprise a nanorod shape. In some cases, the channel region is formed using multiple nanorods. And in some cases, a nanorod includes the channel region.

Nanorods offer alternatives to the designers of MOSFET-based devices since the geometry can be used to alter the electronic properties of the MOSFET channel using quantum size effects. As the diameter of the nanorod channel is reduced, a shift in the density of states, from a three-dimensional continuum of states to a two-dimensional density of states in the channel region may occur. Consequently, the electron and hole effective mass may be reduced and the band gap energy of the semiconductor material may increase in the channel. The lower effective masses of the charge carriers may provide improved carrier transport properties such as higher carrier mobilities. A MOSFET channel with a higher band gap energy may provide a low leakage current between source and drain regions, a lower gate-channel leakage current and a faster switching speed.

A common MOSFET channel material is single crystal silicon. Silicon is a material where the electronic band gap increases as the physical size of the crystal decreases. For a MOSFET with a silicon vertical electron channel shaped as a nanorod, or a silicon vertical electron channel formed with multiple nanorods, reducing the diameter of the nanorod, for example from 13 nm to 7 nm, increases the band gap energy at room temperature from its bulk (or native) band gap energy of 1.12 eV to 3.5 eV. Additional energy band gap separation may be possible by decreasing the nanorod diameter ever further. Lowering the surface state density of the channel along the side of the nanorod using a dielectric or a semiconductor with a band gap energy exceeding the higher

energy of the nanorod, may also increase the band gap separation. Increasing the band gap separation may reduce DIBL and other short channel effects, including band-to-band tunneling induced off-state leakage.

FIG. 1A is a cross-section illustrating nanorod formation according to various embodiments of the invention. In many embodiments, substrate 101A comprises a silicon substrate, but substrate materials other than silicon, such as silicon germanium, may be used. In some embodiments, substrate 101A may comprise a wafer, such as a silicon wafer. In various embodiments, substrate 101A may comprise a silicon on sapphire or a silicon on insulator. The substrate 101A may also comprise an isoelectronic material such as isoelectronic silicon. Various embodiments include the substrate 101A with (001), (011) and (111) oriented crystal surfaces. In some embodiments, the substrate 101A may be cut and/or polished off-axis with an angle ranging from 0.5° to 15° relative to the on-axis cut surface normal (shown as Y).

The impurity and/or electrical carrier concentration in layer 102A may be adjusted to obtain the desired layer conductivity. For example, layer 102A may be a doped to provide an n-type conductivity. In some embodiments, the layer 102A may have p-type conductivity. In various embodiments, the layer 102A may be a substantially unintentionally doped (or undoped) layer. In various embodiments, the layer 102A may be of the same conductivity type as the substrate 101A. In some embodiments, the layer 102A has substantially the same electrical impurity concentration as the substrate 101A. In various embodiments, layer 102A is formed from the substrate 101A. In some embodiments, layer 102A may comprise a portion of the substrate 101A. In various embodiments, layer 102A may comprise an epitaxially grown or deposited film. In some embodiments, the impurity concentration and conductivity type of the layer 102A may be adjusted using ion implantation to achieve the desired electrical concentration.

The layer 103A may be formed on layer 102A and, in some embodiments, may be formed from layer 102A. The layer 103A may be formed using an epitaxial process or a deposition process. Layer 103A and layer 102A may be of the same or of a different conductivity type. In various embodiments, layer 103A is a substantially unintentionally doped layer. In some embodiments,

layer 103A is a doped layer having an impurity concentration of less than $1x10^{17}$ cm^{-3}. Examples of n-type impurities include P, As, and Sb. Examples of p-type impurities include B, Ga and In. In some embodiments, layer 103A may have an electrically active concentration of less than $1x10^{17}$ cm^{-3}. In various embodiments, the impurity and/or electrically active concentration is graded in a direction substantially perpendicular to the surface normal. In various embodiments, the impurity and/or electrically active concentration is graded in a direction substantially parallel to the surface normal. In some embodiments, the impurity concentration and conductivity type of layer 103A may be adjusted using ion implantation to provide a particular electrical concentration. In some embodiments, layer 103A has substantially the same conductivity type as the substrate 101A. In various embodiments, layer 103A is formed from the substrate 101A. In some embodiments, layer 103A may form a portion of the substrate 101A. In various embodiments, layers 103A, 102A and substrate 101A may be formed from a single wafer such as a silicon wafer.

As shown in FIG. 1A, layer 105A may be formed on the surface of the layer 103A as a mask layer. Layer 105A may be formed in the shape of a line, square, circle or other geometry as desired. Layer 105A may be formed of any number of patternable materials such a photoresist, a metal, or a dielectric adaptable to various lithography processes. Spacers 104A may be formed adjacent to layer 105A using a suitable etch resistant material. In some embodiments, layer 104A may comprise, without limitation, a semiconductor material such as SiGe, SiC and SiGeC, a dielectric such as silicon nitride, an oxynitride and SiO_2, a polymer such as a photoresist, a block polymer such as diblock copolymer blends of polystyrene and polymethylmethacrylate, a metal such as W, MO, Ta and Al, or some combination of one or more layers of semiconductors, polymers, block polymers, dielectrics and metals. In various embodiments, the spacers 104A may be formed as a self-assembled layer in a shape of an annular ring. In some embodiments, the spacers may be formed as a self-assembled layer with an island-like profile. In various embodiment, the spacers 104A may be formed as a self-assembled layer forming a circular shaped hole. In some embodiment, the spacers 104A may be formed by a self-assembled layer process without the layer 105A.

FIG. 1B is a cross-section illustrating nanorod formation according to various embodiments of the invention. Here, the layer 105A of FIG. 1A is shown removed, leaving spacers 104B substantially unchanged on layer 103B. At this point, layers 102B and/or 103B may be further processed as desired using for example, diffusion, implantation, and anneal processes to adjust the electrical and mechanical properties of the respective layers between the spacers 104B. In some embodiments, 102B and/or 103B may be further processed to adjust the electrical and mechanical properties of a portion of the respective layers directly under the spacers 104B using the spacers as a mask. In various embodiments, the electrical properties of the layer 102B may be adjusted to provide a conductive region adjacent to the spacers 104B. In various embodiments, the electrical properties of the layer 102B may be adjusted to form one or more shared doped regions extending, at least in part, laterally under the spacers 104B. In some embodiments, the electrical properties of the layer 102B may be adjusted to form a region contacting a doped region.

FIG. 1C is a cross-section illustrating nanorod formation according to various embodiments of the invention. Here, layer 103C and a portion of layer 102C are shown removed between the spacers 104C forming a vertical nanorod structure 110C. The material between the spacers 104C may be removed using an etch process, such as a wet chemical etch, a gas etch such as a plasma etch, and other suitable processes. In various embodiments, the depth of the etch may be less than 1 μm. Layer 103C of the vertical nanorod structure 110C forms the channel region and layer 102C forms a shared doped drain/source region of a transistor. In some embodiments, the channel portion of the vertical structure may be less than 0.5 μm.

The nanorods 110C may be formed as a pillars or columns and may have a lateral cross-section shaped substantially in the form of a disk presenting a vertical rod-like structure as illustrated in FIG. 1D.

FIG. 1D illustrates nanorods 110D formed according to various embodiments of the invention. The diameter of the layer 103D below the spacers 104C may range from about 0.5 nm to about 15 nm. In some embodiments, a diameter of the 103D layer below the spacers 104D may range from about 1 nm to about 10 nm. In general, the diameter may be chosen

according to the desired energy band shift. In various embodiments, the layer 103D between the spacers 102D may be partially removed. In some embodiments, layers 102D, 103D and a portion of substrate material 101D may be removed between the spacers 104D such that there is no shared doped region using layer 102D without further processing (not shown).

In some embodiments, layers 102D and 103D are formed from the substrate material 101D. For example, layer 102D and 103D may be a portion of the substrate material 101D that is a semiconductor wafer. In various embodiments, substrate 101D is a single crystal silicon wafer. In some embodiments, layers 102D, 103D and 101D comprise silicon layers. In various embodiments, layer 102D and 103D may comprise SiGe layers. In some embodiments, layer 102D may be a SiGe layer and 103D may comprise a silicon layer. In various embodiments, layer 102D may comprise a silicon layer and 103D a SiGe layer. In some embodiments, layer 102D and/or layer 103D may comprise a SiC layer or a SiGeC layer.

FIG. 2A is cross-section illustrating a MOS transistor according to various embodiments of the invention. Here, the vertical nanorod 210A is first formed, then a gate dielectric 206A is formed in contact with the channel region 203A of the vertical nanorods. Insulator 207A may be formed between the nanorods over layer 202A. An optional field insulator may be further formed between the nanorods (not shown). The gate dielectric 206A may be formed along the sides of the nanorods 210A surrounding or enclosing the channel region. In some embodiments, the insulator 207A and the gate dielectric 206A are formed of the same dielectric material. In various embodiments, the insulator 207A and the gate dielectric 206A may be different materials. Examples of gate dielectric materials include, without limitation, SiO_2, SiN, and nitrides and oxidynitrides formed with Si, Mo, W, Ta, Hf, and Al. In some embodiments the gate dielectric may comprise a composite multi-layer dielectric. The thickness of the gate dielectric 206A may range from about 2 nm to about 20 nm, depending on the gate dielectric material and related properties such as a dielectric constant. In some embodiments, the insulator 207A and the gate dielectric 206A may be formed with the same thickness or with different thicknesses.

FIG. 2B is cross-section illustrating a MOS transistor according to various embodiments of the invention. Here, two access transistors 200B are shown separated by an isolation region 212B formed on the substrate 201B. The isolation region 212B may be a shallow trench isolation region formed in the shared drain/source region 202B to electrically isolate the access transistors 200B. Isolation region 212B may be an etched region filled with a dielectric material such as vapor deposited SiO_2. In some embodiments, the isolation region 212B may be formed in a portion of the substrate 201B. The access transistors include the vertical nanorods 210B with a drain/source region 211B at one end of the nanorod in contact with channel region 203B, and a shared drain/source region 202B at the second end in contact with the channel region. In some embodiments, an isolation region may used to electrically isolate a plurality of vertical nanorods configured in parallel to form a vertical channel transistor. In some embodiments, the length of the vertical channel region 203B may be less than 250 nm. In various embodiments, the length of the vertical channel region 203B may be between about 20 nm and about 150 nm.

The gate conductor 208B may be formed over the gate dielectric 206B that surrounds the nanorods in the channel region 203B. The gate region may be formed as a shared conductive gate region by filling-in the area between the nanorods 210B with a suitable conductive material. In some embodiments, the gate region may be formed such that there is no shared gate region. Examples of conductive gate region materials include, but are not limited to, polysilicon, metals such as Al, W, Mo and Ta, binaries such as TiN and TaN, metal silicides such as WSi_x, NiSi, $CoSi_x$ and $TiSi_x$, a dacecamine, and combinations of layers of conductive material. Field insulator 209B may be formed overlaying gate conductor 208B and may comprise any suitable insulator, including, without limitation, SiO_2, SiN, and oxynitride-based dielectrics containing Si, Al, W, Ta, Ti, and Mo.

Drain/source region 211B and shared source/drain region 202B may be configured to be in electrical contact using the vertical channel region 203B of the nanorods such that no current flows across the channel region with zero gate bias voltage applied to gate conductor 208B. Drain/source region 211B may be formed by epitaxial growth, ion implantation, and deposition processes. In some

embodiments, the drain/source region 211B may be formed as a shared region. In various embodiments, drain/source region 211B may comprise silicon, doped polysilicon, SiC, SiGe or SiGeC. A substantially planar surface may be obtained for the field dielectric 209B and drain source region 211B using a chemical mechanical process as are known to those of ordinary skill in the art. In various embodiments, a conductive region overlaying insulator 209B and the drain/source region 211B may be formed to couple the nanorods 210B (not shown).

FIG. 3 is a surface view of a MOS transistor according to various embodiments of the invention. Here, the access transistor 300 is shown with nine nanorods 310 and an isolation region 312, but may include more or less nanorods. The vertical channel region 203B of FIG. 2B coupled to the drain/source region 302 form a composite of parallel channels, which may be electrically coupled to a capacitor at 311 (not shown). In some embodiments, the isolation region 312 may be used electrically isolate a plurality of vertical channel regions. In various embodiments, the isolation region 312 may be used to electrically isolate the vertical channel regions of an access transistor 300 from the vertical channel regions of an adjacent access transistor 300. In some embodiments, the isolation region 312 may be used to isolate a capacitor coupled to the access transistor 300 from adjacent capacitor cells (not shown). As show by way of example in FIG. 3, but not by limitation, a shared annular gate arrangement of nine nanorods 310 may be formed with a center-to-center spacing of 24 nm using vertical nanorod channels (not shown) having about a 10 nm diameter, a gate dielectric 306 with about a 2 nm radial thickness and gate conductor 308 with about a 5 nm radial thickness. Various embodiments include a gate dielectric thicknesses ranging from about 2 nm to about 20 nm, channel region diameters ranging from about 0.5 nm to about 15 nm, and conductive gate region thicknesses ranging from about 3 nm to about 10 nm. The number of parallel coupled nanorods and/or channels formed as part of the access transistor, or other such transistor, may affect desired performance characteristics. In general, the number of vertical channels per surface area may be determined and adjusted according to specified design rules for a particular manufacturing process.

FIG. 4 is a cross-section illustrating a memory cell according to various embodiments of the invention. Here, a DRAM cell 430 includes an access transistor 400 and double-sided capacitor 425, but any type of capacitor may be configured to be supported by and/or coupled to the access transistor. The double-sided capacitor stores electrical charge received from an input circuit (not shown) such that the charge establishes an electric field across the insulator 422 between capacitor plates 421 and 423. More information regarding fabrication of storage cell capacitors can be found in U.S. Patent No. 6,030,847 entitled Method for Forming a Storage Capacitor Compatible with High Dielectric Constant Material, and U.S. Patent Application Serial No. 10/788,977 entitled Semiconductor Fabrication Using a Collar, both incorporated by reference herein in their entirety.

In various embodiments, and as shown in FIG 4, the n-type drain/source region 411 of the access transistor 400 are in contact the nanorod channels 403 and capacitor plate 421. The electric charge supporting the electric field between capacitor plates 421 and 423 may place each drain/source region 411 in contact with capacitor plate 421 at substantially equal potential. In this case, charge may not flow though the vertical channel region 403 of any nanorod 410 in the absence of a bias potential on gate conductor 408. In some embodiments, the gate conductor 408 shared a conductor coupling the gate region of one or more nanorods. Thus, the gate conductor 408 may comprise multiple discrete gate electrodes coupled using a conductor. The vertical channel 403 of the nanorods 410 may be sufficiently small in diameter so that the electronic band gap energy of the material in the channel region 403 is greater than in the non-channel regions, such as in the unetched portion of the n-type drain/source region 402 and the substrate layer 401. In various embodiments, the substrate 401, the n-type shared drain/source region 402, the channel region 403 and/or the n-type drain/source region 411 are formed from a material with the same lattice constant. In some embodiments, the substrate 401, the shared drain/source region 402, the channel region 403 and/or the drain/source region 411 are formed of silicon. In various embodiments, the drain/source region 411 is made sufficiently large to eliminate quantum size effects, such as a higher energy band gap shift. In some embodiments, the drains/source region 411 may

be shared drains/source region. In various embodiments, a portion of the shared drain/source region 402 is made sufficiently large to eliminate quantum size effects in that portion. In some embodiments, the shared drain/source region 402 is coupled to the ground plane 413 using via holes (not shown). In various embodiments, the shared source drain region 402 may be used as a ground plane or a similar conductive region. In some embodiments, the substrate is coupled to the ground plane 413. In various embodiments, the substrate forms at least a part of a conductive plane such as a ground plane. In some embodiments, an electrical isolation region (not shown) may be formed in the substrate between the nanorods 410. In various embodiments, the substrate may comprise an electrically non-conductive material such as a silicon wafer with a low carrier concentration. In some embodiments, the ground plane 413 may comprise a series of ground planes. In various embodiments, the ground plane 413 is formed as a plurality of conductors coupled to one or more conductors, electrodes, circuit element, voltages and the like.

Charge placed on the capacitor 425 by a voltage signal transmitted by conductor from an input/output circuit (not shown), for example, may be stored during the access transistor's off-state since no further current path is provided. For the memory cell illustrated in FIG. 4, the charge may be used to establish an electric field in the vertical direction between the capacitor plate 421 and the conductive ground plane 413. A portion of the electric field may have a vertical potential gradient across the channel region 403 of the nanorods 410 of the access transistor 400 between the source/drain regions 402, 411. In the absence of voltage applied to the gate conductor 408, substantially no current flows between drain/source regions 402, 411 (off-state).

Application of a voltage to the gate conductor 408 may establish an electric field across gate dielectric 406 with field components perpendicular to the channel 403. A gate voltage in cooperation with the gate dielectric layer 406 may further generate a charge inversion layer (not shown) extending inward from the gate dielectric along the channel 403 between drain/source regions 402, 411. The charge inversion layer may electrically couple the drain/source regions 402, 411 to form a current path there between. In some embodiments, the nanorods may have a circular cross-section and the electric field includes a radial

potential gradient. The formation of a current path between the capacitor plate 421 in contact with the drain/source region 411 and the shared drain/source region 402 and/or substrate 401 and/or conductive ground plane 413, may allow the capacitor 425 to discharge through the channel region, removing the capacitor's charge and the respective voltage and electric field.

In the transistor off-state, the energy band discontinuity (or energy band offset) between the capacitor plate 421 and the channel region 403 may be larger with the nanorods 410 than for a transistor channel formed from the same material with a bulk band gap energy (e.g. without nanorods). This increased energy band offset may provide an increased electron barrier for blocking electrons thereby reducing the amount of charge escaping the capacitor plate 421 though the channel region 403. The increased energy band gap difference between the source/drain region 402 and the channel region 403 may reduce DIBL by improving the sub-threshold ideality factor and sub-threshold voltage swing. Consequently, a reduction in the amount of charge leaking from the capacitor 425 over time may occur through the access transistor 400. As a result, the DRAM cell 430 may retain charge for longer times.

FIG. 5 is block diagram of a memory device 500 according to various embodiments of the invention. The memory device 500 may include an array of memory cells 502, an address decoder 504, row access circuitry 506, column access circuitry 508, control circuitry 510, and an input/output (I/O) circuit 512. The memory cells 502 may comprise one or more capacitor cells operatively coupled to the row access circuit 506 and the column access circuit. The memory device 500 may be operably coupled to an external processor 514, or memory controller (not shown) to provide access to the memory content. The memory device 500 is shown to receive control signals from the processor 514, such as WE*, RAS* and CAS* signals. The memory device 500 may store data which is accessed via I/O lines. It will be appreciated by those of ordinary skill in the art that additional circuitry and control signals can be provided, and that the memory device of FIG. 5 has been simplified to help focus on, and not obscure, various embodiments of the invention. Any of the memory cells, transistors, and associated circuitry may include an integrated circuit structure and/or elements in accordance with various embodiments of the invention. For

example, the array of memory cells 502 may be fabricated according to embodiments of the invention, so as to include one or more nanorods, as shown in FIG. 1D

It should be understood that the above description of a memory device 500 is intended to provide a general understanding of possible memory structures, and is not a complete description of all the elements and features of a specific type of memory, such as DRAM. Further, many embodiments of the invention are equally applicable to any size and type of memory circuit and are not intended to be limited to the DRAM described above. Other alternative types of devices include SRAM (static random access memory) and flash memories. Additionally, the DRAM could comprise a synchronous DRAM, commonly referred to as SGRAM (synchronous graphics random access memory), SDRAM (synchronous DRAM), SDRAM II, and DDR SDRAM (double data rate SDRAM), as well as Synchlink™ or Rambus™ DRAMs and other technologies.

FIG. 6 illustrates a semiconductor wafer 600 according to various embodiments of the invention. As shown, a semiconductor die 610 may be produced from a wafer 600. The semiconductor die 610 may be individually patterned on a substrate layer or wafer 600 that contains circuitry, or integrated circuit devices, to perform a specific function. The semiconductor wafer 600 may contain a repeated pattern of such semiconductor dies 610 containing the same functionality. The semiconductor die 610 may be packaged in a protective casing (not shown) with leads extending therefrom (not shown), providing access to the circuitry of the die for unilateral or bilateral communication and control. The semiconductor die 610 may include an integrated circuit structure or element in accordance with various embodiments of the invention, including one or more nanorods, as shown in FIG. 1D.

FIG. 7 illustrates a circuit module 700 according to various embodiment of the invention. As shown in FIG. 7, two or more semiconductor dice 610 may be combined, with or without a protective casing, into a circuit module 700 to enhance or extend the functionality of an individual semiconductor die 610. The circuit module 700 may comprise a combination of semiconductor dice 610 representing a variety of functions, or a combination of semiconductor dies 610

containing the same functionality. One or more semiconductor dice 610 of circuit module 700 may contain at least one integrated circuit structure or element in accordance with embodiments of the invention, including one or more nanorods, as shown in FIG. 1D.

Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules and application-specific modules, and may include multilayer, multichip modules. The circuit module 700 may be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, a personal digital assistant, a network server such as a file server or an application server, an automobile, an industrial control system, an aircraft and others. The circuit module 700 may have a variety of leads 710 extending therefrom and coupled to the semiconductor dice 610 providing unilateral or bilateral communication and control.

FIG. 8 illustrates a circuit module as a memory module 800, according to various embodiment of the invention. A memory module 800 may include multiple memory devices 810 contained on a support 815 (the number generally depending upon the desired bus width and the desire for parity checking). The memory module 800 may accept a command signal from an external controller (not shown) on a command link 820 and provide for data input and data output on data links 830. The command link 820 and data links 830 may be connected to leads 840 extending from the support 815. The leads 840 are shown for conceptual purposes and are not limited to the positions shown in FIG. 8. At least one of the memory devices 810 may contain an integrated circuit structure or element in accordance with embodiments of the invention, including one or more nanorods, as shown in FIG. 1D.

FIG. 9 illustrates a block diagram of an electronic system 900 according to various embodiment of the invention. Figure 9 shows an electronic system 900 containing one or more circuit modules 700. The electronic system 900 may include a user interface 910 that provides a user of the electronic system 900 with some form of control or observation of the results generated by the electronic system 900. Some examples of a user interface 910 include a keyboard, a pointing device, a monitor or printer of a personal computer; a

tuning dial, a display or speakers of a radio; an ignition switch, gauges or gas pedal of an automobile; and a card reader, keypad, display or currency dispenser of an automated teller machine, as well as other human-machine interfaces.

The user interface 910 may further include access ports provided to electronic system 900. Access ports are used to connect an electronic system 900 to the more tangible user interface components previously provided by way of example. One or more of the circuit modules 700 may comprise a processor providing some form of manipulation, control or direction of inputs from or outputs to the user interface 710, or of other information either preprogrammed into, or otherwise provided to, the electronic system 900. As will be apparent from the lists of examples previously given, the electronic system 900 may be associated with certain mechanical components (not shown) in addition to the circuit modules 700 and the user interface 910. It should be understood that the one or more circuit modules 700 in the electronic system 900 can be replaced by a single integrated circuit. Furthermore, the electronic system 900 may be a subcomponent of a larger electronic system. It should also be understood by those of ordinary skill in the art, after reading this disclosure that at least one of the memory modules 700 may contain an integrated circuit structure or element in accordance with embodiments of the invention, including one or more nanorods, as shown in FIG. 1D.

FIG. 10 illustrates a block diagram of an electronic system as a memory system 1000 according to various embodiment of the invention. A memory system 1000 may contain one or more memory modules 800 and a memory controller 1010. The memory modules 800 may each contain one or more memory devices 810. At least one of memory devices 810 may contain an integrated circuit structure or element in accordance with embodiments of the invention, including one or more nanorods, as shown in FIG. 1D.

The memory controller 1010 may provide and control a bidirectional interface between the memory system 1000 and an external system bus 1020. In some embodiments, the memory controller 1010 may also contain one or more nanorods, as shown in FIG. 1D. The memory system 1400 may accept a command signal from the external system bus 1020 and relay it to the one or more memory modules 800 on a command link 830. The memory system 1000

may provide data input and data output between the one or more memory modules 800 and the external system bus 1020 on data links 1040.

FIG. 11 illustrates a block diagram of an electronic system as a computer system 1100 according to various embodiment of the invention. A computer system 1100 may contain a processor 1110 and a memory system 1000 housed in a computer unit 1105. The computer system 1100 also serves as an example of an electronic system containing another electronic system, i.e., memory system 1000, as a subcomponent. The computer system 1100 optionally contains user interface components, such as a keyboard 1120, a pointing device 1130, a monitor 1140, a printer 1150 and a bulk storage device 1160. Other components associated with the computer system 1100, such as modems, device driver cards, additional storage devices, etc. may also be included. The processor 1110 and the memory system 1000 of the computer system 1100 can be incorporated on a single integrated circuit. Such single package processing units may operate to reduce the communication time between the processor and the memory circuit. The processor 1110 and the memory system 1000 may contain one or more nanorods, as shown in FIG. 1D. In some embodiments, the printer 1150 or the bulk storage device 1160 may contain an integrated circuit structure or element in accordance with embodiments of the invention, including one or more nanorods, as shown in FIG. 1D.

The above Detailed Description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments. These embodiments, which are also referred to herein as "examples," are described in enough detail to enable those skilled in the art to practice the invention. The embodiments may be combined, other embodiments may be utilized, or structural, logical and electrical changes may be made without departing from the scope of the present invention. The Detailed Description is, therefore, not to be taken in a limiting sense, and the scope of the various embodiments is defined only by the appended claims and their equivalents.

In this document, the terms "a" or "an" are used, as is common in patent documents, to include one or more than one. In this document, the term "or" is used to refer to a nonexclusive or, unless otherwise indicated. Furthermore, all

publications, patents, and patent documents referred to in this document are incorporated by reference herein in their entirety, as though individually incorporated by reference. In the event of inconsistent usages between this document and those documents so incorporated by reference, the usage in the incorporated reference(s) should be considered supplementary to that of this document; for irreconcilable inconsistencies, the usage in this document controls.

It is to be understood that the above description is intended to be illustrative, and not restrictive. For example, the above-described embodiments (and/or aspects thereof) may be used in combination with each other. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled. In the appended claims, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein." Also, in the following claims, the terms "including" and "comprising" are open-ended, that is, a system, device, article, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms "first," "second," and "third," etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

The Abstract is provided to comply with 37 C.F.R. §1.72(b), which requires that it allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. A memory cell, comprising:

a vertical channel coupled at a first end of the vertical channel to a capacitor, the vertical channel configured to increase a native band gap energy of material forming the channel;

a dielectric substantially surrounding the vertical channel; and

a field electrode coupled to the vertical channel using the dielectric.

2. The memory cell of claim 1, wherein the capacitor is a double-sided capacitor associated with a dynamic random access memory.

3. The memory cell of one of claims 1 and 2, wherein the vertical channel is coupled to the capacitor using at least one shared doped region.

4. The memory cell of claim 3, wherein the at least one doped region is formed from a silicon substrate.

5. The memory cell of one of claims 1-4, wherein the vertical channel includes a channel portion with a substantially circular cross-section.

6. The memory cell of claim 5, wherein the substantially circular cross-section has a diameter of between about 0.5 nm to about 15 nm.

7. The memory cell of one of claims 1-6, wherein the field electrode is configured to regulate a discharge current associated with the capacitor.

8. The memory cell of one of claims 1-7, wherein a length of the vertical channel is less than 250 nm.

9. The memory cell of one of claims 1-8, wherein the dielectric is configured to support an electric field along the vertical channel to couple a charge at the first end with a shared doped region.

10. The memory cell of one of claims 1-9, wherein the dielectric is configured to cooperate with at least one of a channel dimension and the channel material to increase the native band gap energy.

11. A system comprising:

a plurality of capacitive cells coupled to an input/output circuit, wherein some of the plurality of capacitive cells include a capacitor coupled to an access transistor comprising a vertical channel region configured to transfer charge between the capacitor and a conductive region based on a signal associated with a processor, and wherein the vertical channel region comprises at least one nanorod configured to reduce a leakage current between the capacitor and the conductive region using a band gap energy difference.

12. The system of claim 11, wherein the at least one nanorod shares a gate region channel material.

13. The system of one of claims 11 or 12, wherein the gate region channel material includes at least one of a dielectric and a gate conductor.

14. The system of one of claims 11-13, wherein the dielectric includes a gate dielectric configured to support an inversion field in the vertical channel region.

15. The system of one of claims 11-14, wherein the at least one nanorod is formed from at least one of a silicon substrate and a silicon wafer.

16. The system of one of claims 11-15, wherein the capacitor includes a double-sided capacitor.

17. The system of one of claims 11-16, wherein the plurality of capacitive cells are configured to form a portion of a memory module.

18. The system of one of claims 11-17, wherein the memory module comprises a DRAM module.

19. The system of one of claims 11-18, wherein the at least one nanorod includes a region with a band gap energy greater than 1.12 eV.

20. A memory unit, comprising:

a channel region comprising at least one nanorod, wherein the at least one nanorod includes a vertical transport region of semiconductor material;

a gate region encompassing at least a portion of the at least one nanorod in the vertical transport region; and

a first drain/source region coupled to the at least one nanorod at an end supporting a capacitor cell.

21. The memory unit of claim 20, wherein the channel region is configured to use a shifted band gap energy.

22. The memory unit of one of claims 20-21, wherein the at least one nanorod is configured to provide a shifted band gap energy.

23. The memory unit of one of claims 20-22, wherein the channel region is configured to reduce an off-state leakage current associated with the capacitor cell.

24. The memory unit of one of claims 20-23, wherein the gate region includes a shared gate material comprising at least one of a gate dielectric and a gate conductor.

25. The memory unit of one of claims 20-24, wherein the gate region is configured to use a common gate electrode.

26. The memory unit of one of claims 20-25, wherein a diameter of the at least one nanorod is between about 0.5 nm and about 20 nm.

27. The memory unit of one of claims 20-26, wherein the vertical transport region includes a portion with a quantization energy that is greater than a bulk band gap energy.

28. The memory unit of one of claims 20-27, wherein the channel region is coupled to a second drain/source region.

29. The memory unit of one of claims 20-27, wherein at least one of a second drain/source region and the least one nanorod is formed from a single crystal semiconductor substrate.

30. The memory unit of one of claims 20-29, wherein the vertical transport region includes at least one of a silicon, silicon germanium, and a silicon carbide.

31. The memory unit of one of claims 20-30, wherein the gate region includes a material comprising at least one of a metal and a polysilicon.

32. The memory unit of one of claims 20-31, wherein the capacitor cell is coupled to at least one of a row access circuit and a column access circuit.

33. A method comprising:

propagating charge through a predefined vertical region in a semiconductor material according to a specified signal, the vertical region coupled to an electrode associated with a capacitor; and

blocking charge flow using the predefined vertical region, wherein the semiconductor material has an electronic energy band gap greater than its native band gap energy.

34. The method of claim 33, wherein propagating includes propagating through at least one nanorod.

35. The method of one of claims 33-34, wherein propagating includes propagating charge to discharge the capacitor.

36. The method of one of claims 33-35, wherein blocking includes blocking charge associated with a leakage current.

37. The method of one of claims 33-36, wherein blocking includes selectively blocking using the electronic energy band gap in combination with a bias field associated with a gate potential.

38. A method comprising:

forming a vertical channel transistor using a first semiconductor material and a second semiconductor material, the first semiconductor material incorporating a nanorod geometry to increase an electronic energy gap of the first semiconductor material, and the second semiconductor material having a native electronic band gap energy less than the electronic band gap energy of the first semiconductor material; and

forming a gate region enclosing a portion of first semiconductor material.

39. The method of claim 38, wherein forming a vertical channel transistor includes forming with a material that includes silicon.

40. The method of one of claims 38-39, wherein forming a vertical channel transistor using the first semiconductor material includes using a first semiconductor material with the same lattice constant as silicon.

41. The method of one of claims 38-40, wherein forming a vertical transistor channel includes forming using a self assembled layer.

42. A method comprising:

forming an access transistor comprising at least one vertical nanorod;

forming a capacitor cell supported by the access transistor; and

connecting the access transistor to the capacitor cell using a plurality of electrodes.

43. The method of claim 42, wherein forming an access transistor includes forming an annular gate structure.

44. The method of claim 43, wherein forming an annular gate structure includes forming an annular gate dielectric and an annular gate electrode.

45. The method of one of claims 42-44, wherein forming an access transistor includes forming a shared drain/source region.

46. The method of one of claims 42-45, wherein forming an access transistor includes removing material using a spacer layer.

47. The method of claim 46, wherein removing includes removing material supported by a substrate.

48. The method of one of claims 46-47, wherein removing includes removing at least one of a substrate material and a portion of a semiconductor wafer.

49. The method of one of claims 42-48, wherein forming an access transistor includes first forming the at least one vertical nanorod.

50. The method of one of claims 42-49, wherein connecting the access transistor includes coupling the at least one nanorod to the capacitor cell using a capacitor plate.

51. The method of one of claims 42-49, wherein connecting the access transistor includes connecting the access transistor to the capacitor cell using a gate electrode.

52. A memory cell comprising:

an access transistor adjacent to a substrate layer, the access transistor comprising at least one vertical channel shaped as a rod, the at least one vertical channel sharing a gate electrode and at least one drain/source region with another vertical channel; and

a capacitor coupled to one end of the access transistor.

53. The memory cell of claim 52, wherein the gate electrode encloses a region including a quantized band gap energy.

54. The memory cell of one of claims 52-53, wherein the at least one vertical channel is formed from the substrate layer.

55. The memory cell of one of claims 52-54, wherein the substrate layer is a silicon wafer.

56. The memory cell of one of claims 52-55, wherein the at least one vertical channel, the substrate layer, and the at least one drain/source region are formed with materials having the same lattice constant.

57. The memory cell of one of claims 52-56, wherein the at least one vertical channel, the substrate layer, and the at least one drain/source region are a formed of a single material.

58. A method comprising:

establishing a first electric field in a vertical electron channel;

establishing a second electric field in the vertical electron channel to discharge a capacitor, wherein the vertical electron channel includes a semiconductor material with a first band gap energy greater than silicon, and wherein the vertical electron channel is coupled to a region of material with a second band gap energy lower than the first band gap energy, and wherein at least one of the vertical electron channel and the region of material have a lattice constant equal to silicon.

59. The method of claim 58, wherein establishing a first electric field includes establishing a charge on a capacitor plate.

60. The method of claim 59, wherein establishing a charge includes establishing a charge on the capacitor plate associated with a double sided capacitor.

61. The method of one of claims 58-60, wherein establishing a first electric field includes establishing a charge on a capacitor plate.

62. The method of one of claims 58-61, wherein establishing a first electric field includes establishing a first electric field with a vertical potential gradient.

63. The method of one of claims 58-62, wherein establishing a second electric field includes discharging a capacitor associated with a dynamic read only memory cell.

64. The method of one of claims 58-63, wherein establishing a second electric field includes establishing a second electric field with a radial potential gradient.

65. A system comprising:

a user interface coupled to a memory, the memory comprising a plurality of capacitor cells, at least a portion of the capacitor cells including at least one access transistor, the access transistor comprising at least one vertical channel shaped as a rod, wherein the rod includes a first band gap energy region and a second band gap energy region, the second band gap energy being lower than the first band gap energy, and wherein the first band gap energy region and the second band gap energy region cooperate to reduce a channel leakage current.

66. The system of claim 65, wherein the user interface is coupled to at least one of a personal digital assistant, a cell phone, a television, a computer and a network server.

67. The system of one of claims 65-66, wherein the user interface is configured to receive a signal associated with at least one of a processor and a modem.

68. The system of one of claims 65-67, wherein the user interface is configured to transmit a signal to at least one of a processor, a display and a storage device.