FIG. 1

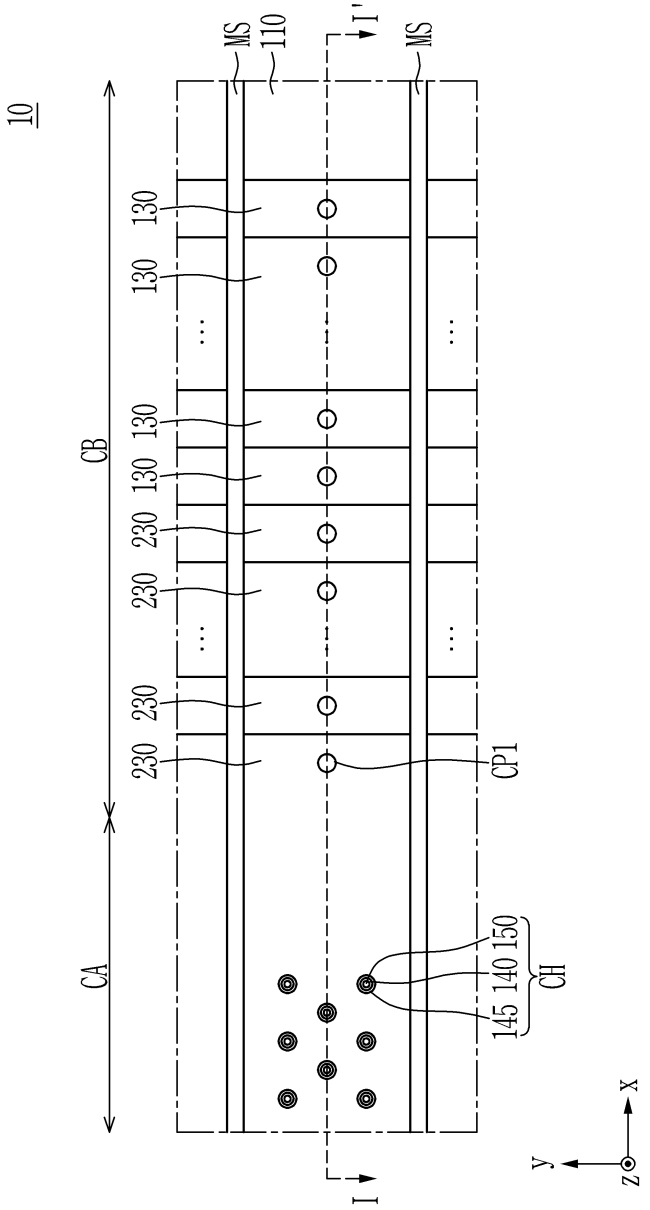

10
MS
110
I'
MS
130
130
130
130
230
230
230
230
CB
CA
CP1
150
140
145
CH
I
y
x
z

FIG. 2

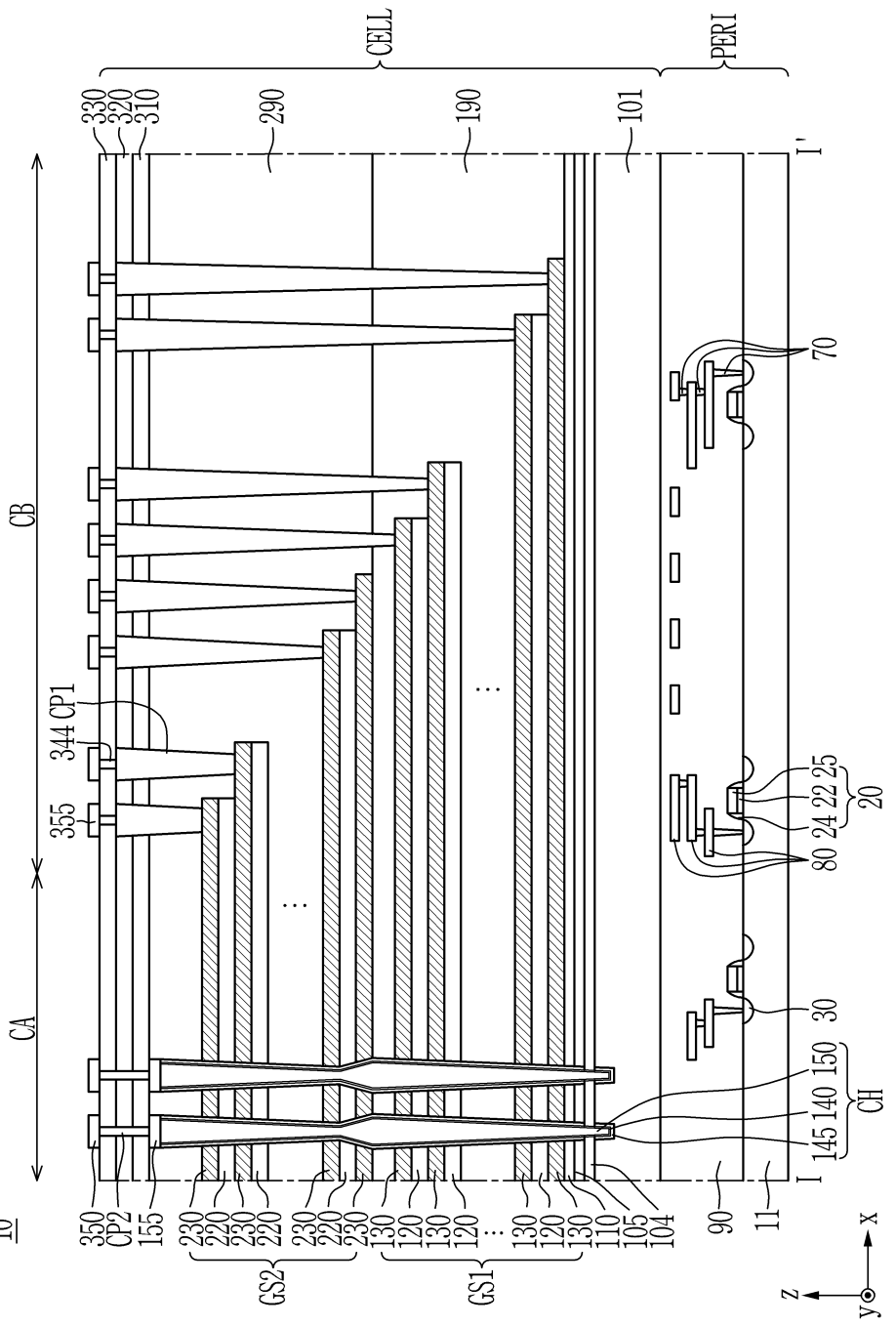

CELL
PERI
330
320
310
290
190
101
I'
I
70
80
24
22
25
20
30
150
140
145
CH
CB
CA
344
CP1
355
10
350
CP2
155
230
220
GS2
130
120
GS1
110
105
104
90
11
z
y
x

FIG. 3

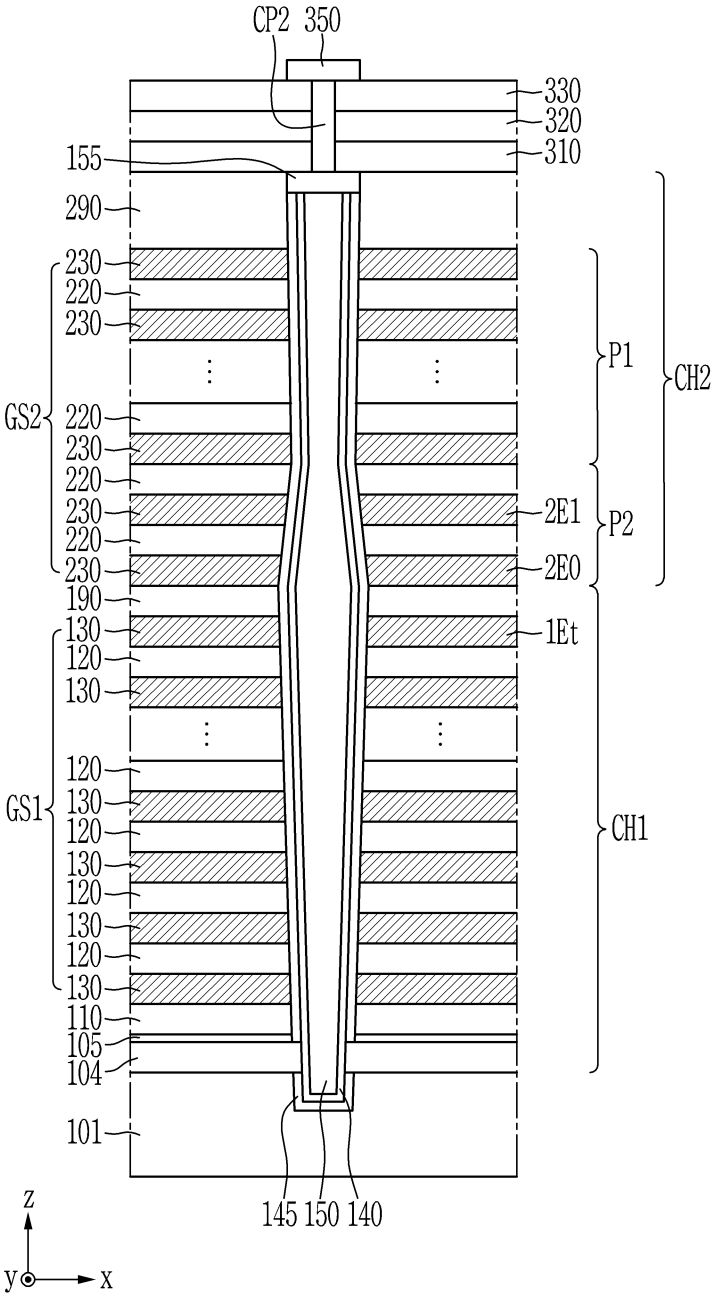

CP2
350
330
320
310
155
290
230
220
230
GS2
220
230
220
230
220
230
190
130
120
130
120
130
120
130
120
130
120
130
110
105
104
101
GS1
P1
CH2
P2
2E1
2E0
1Et
CH1
145
150
140
z
y
x

FIG. 4

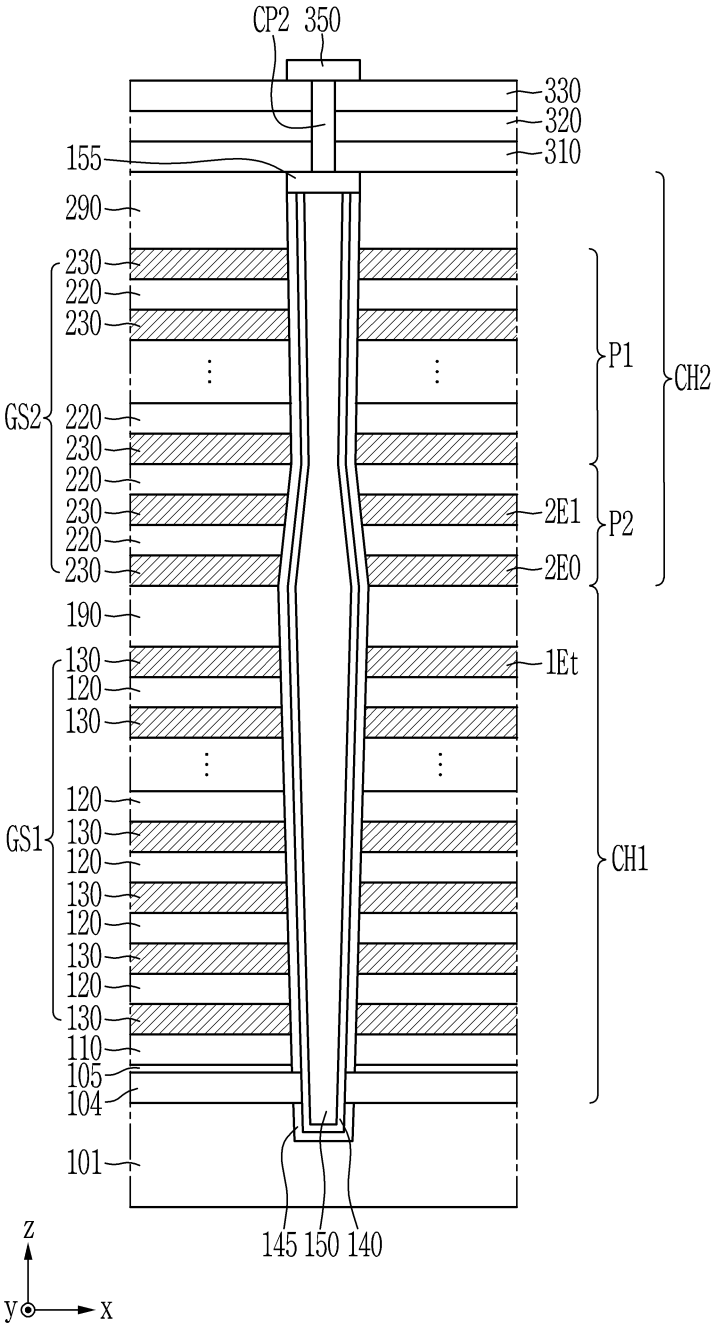

CP2
350
330
320
310
155
290
230
220
230
GS2
220
230
220
230
220
230
190
130
120
130
120
130
120
130
120
130
120
130
110
105
104
101
GS1
P1
CH2
2E1
P2
2E0
1Et
CH1
145
150
140
z
y
x

FIG. 5

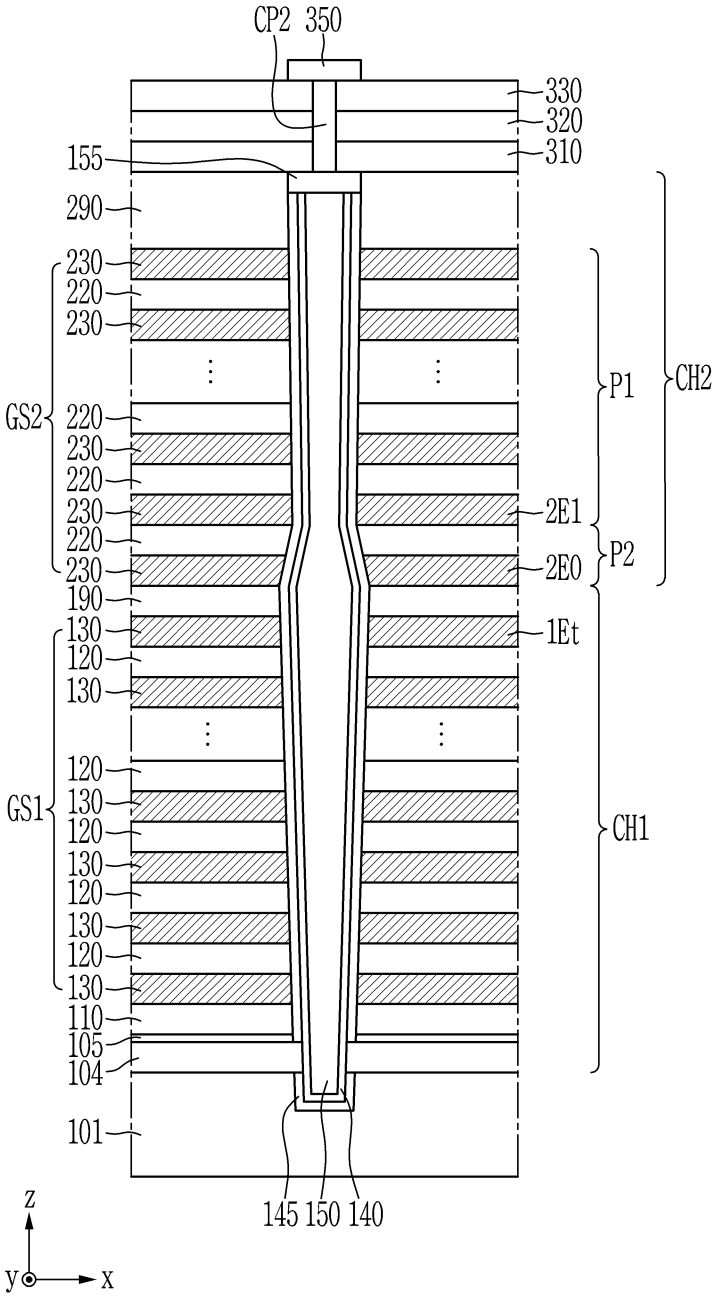

CP2
350
330
320
310
155
290
230
220
230
GS2
220
230
220
230
220
230
190
130
120
130
120
130
120
130
120
130
120
130
110
105
104
101
GS1
P1
CH2
2E1
P2
2E0
1Et
CH1
145
150
140
z
y
x

FIG. 6

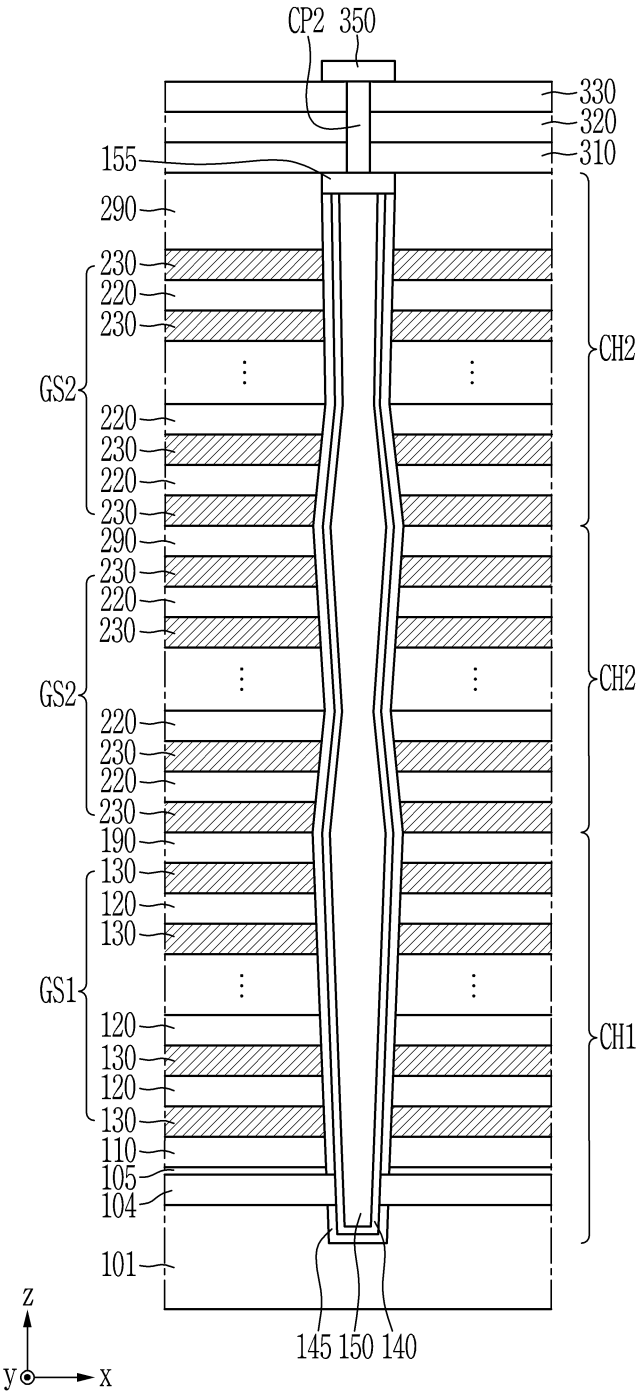

CP2
350
330
320
310
155
290
230
220
230
GS2
CH2
220
230
220
230
290
230
220
230
GS2
CH2
220
230
220
230
190
130
120
130
GS1
CH1
120
130
120
130
110
105
104
101
145
150
140
z
y
x

FIG. 7

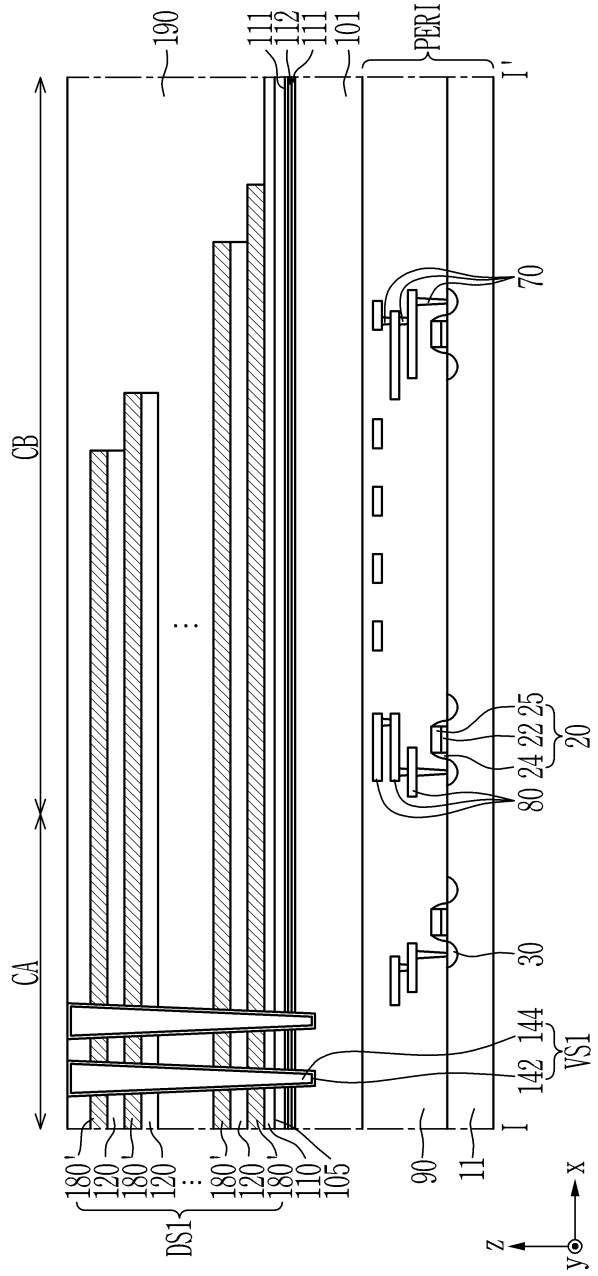

190
111
112
111
101
PERI
I'
CB
CA
70
25
22
24
20
80
30
144
142
VS1
180'
120
180
120
180'
120
180
110
105
DS1
90
11
I
z
x
y

FIG. 8

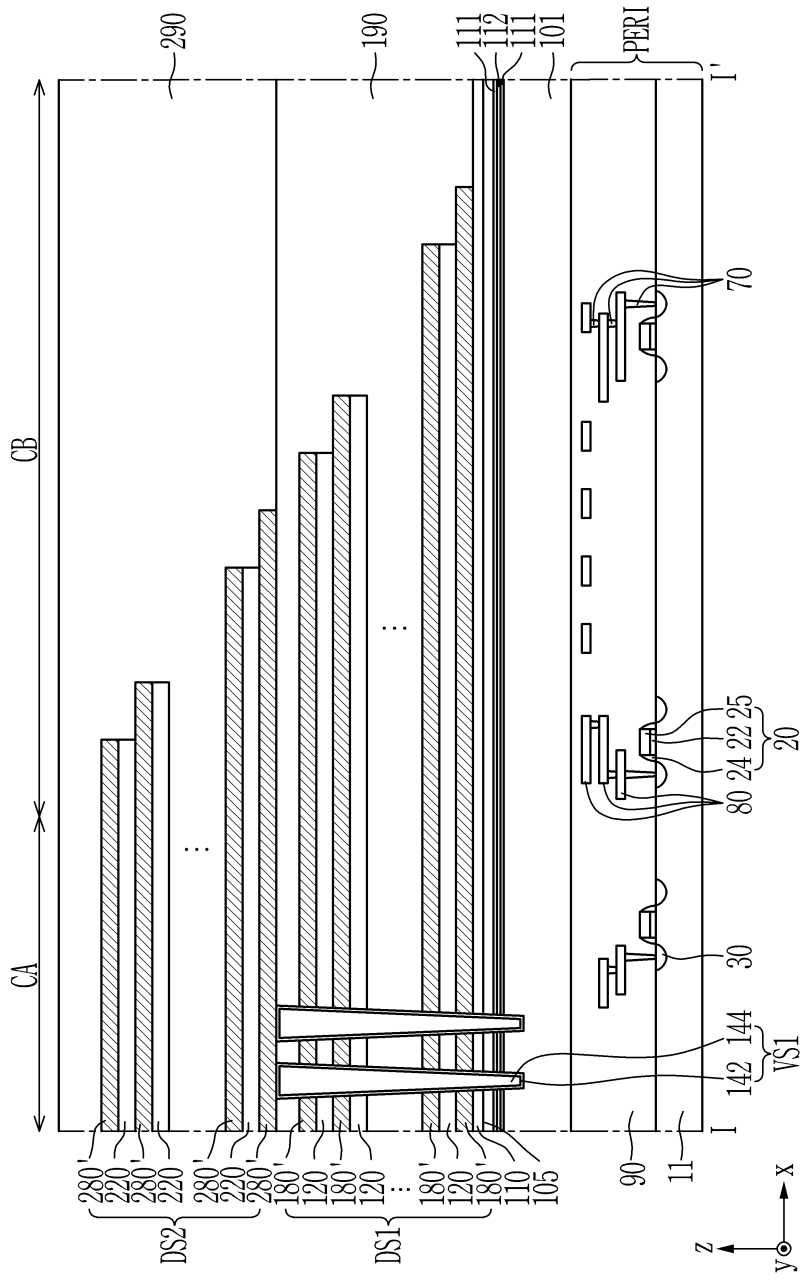

290
190
111
112
111
101
PERI
I'
CB
CA
70
80 24 22 25
20
30
144
VS1
142
I
90
11
280'
220'
280'
220
DS2
280'
220'
280'
180'
120'
180'
120
DS1
180'
120'
180'
110
105
z
y
x

FIG. 9

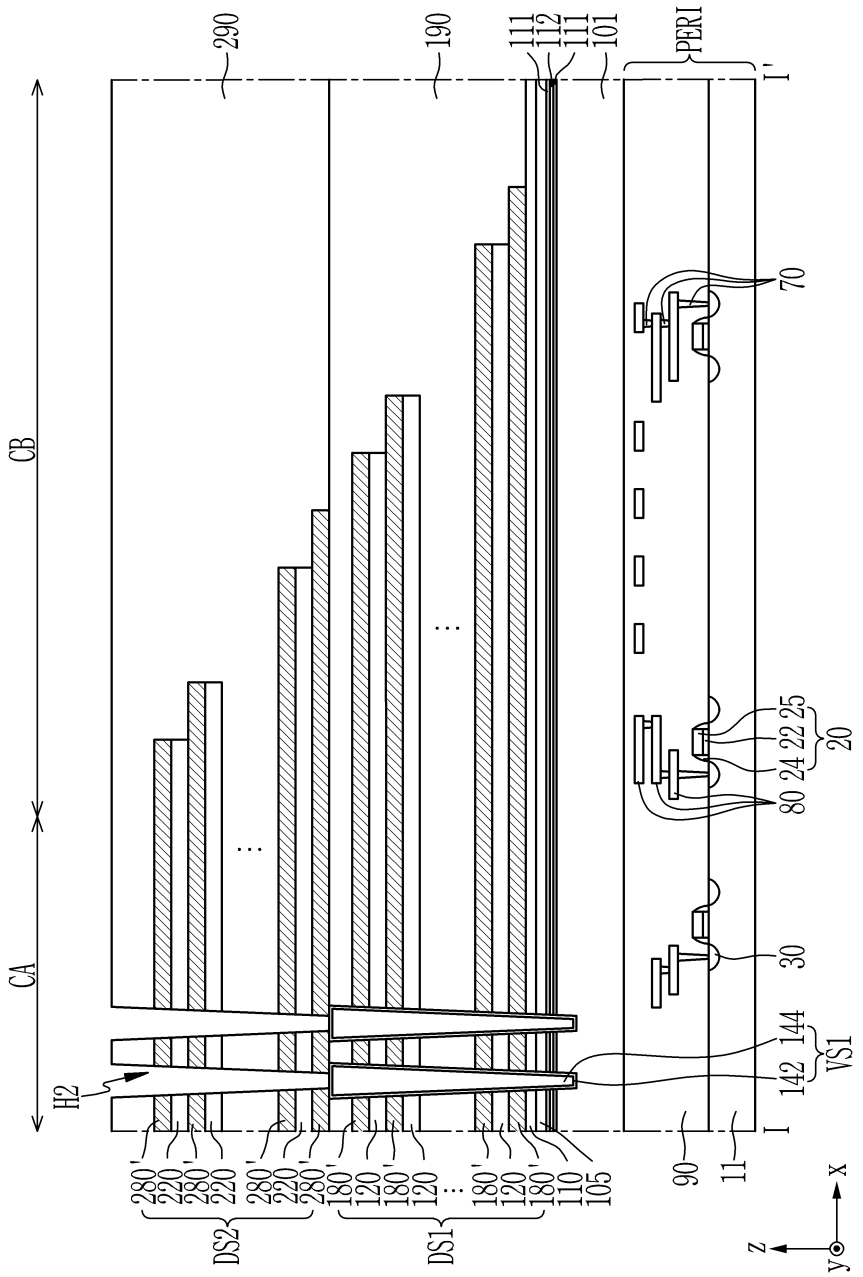

290
190
111
112
111
101
PERI
I'
CB
CA
H2
70
25
22
24
80
20
30
144
142
VS1
280'
220'
280'
220
280'
220'
280'
180'
120'
180'
120
180'
120'
180'
110
105
DS2
DS1
90
11
I
z
y
x

FIG. 10

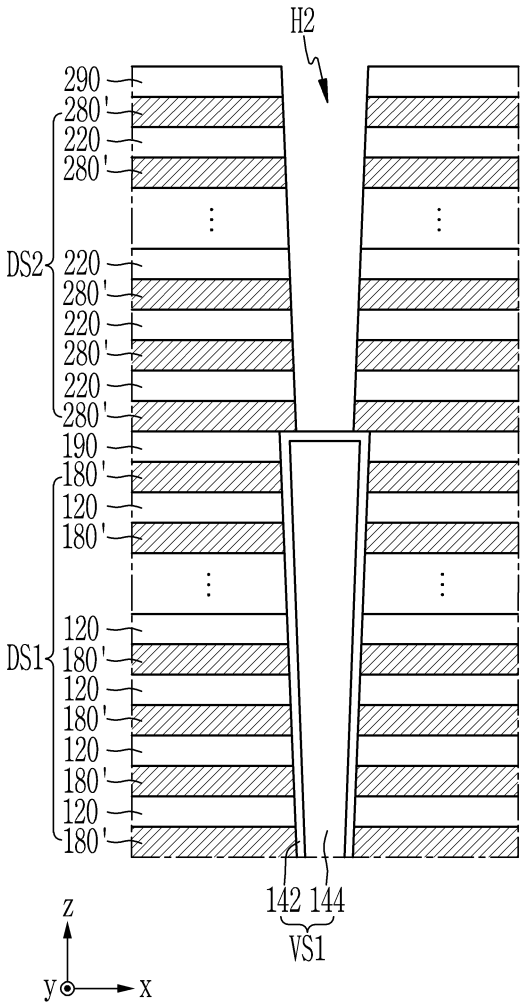

H2
290
280'
220
280'
DS2
220
280'
220
280'
220
280'
190
180'
120
180'
DS1
120
180'
120
180'
120
180'
120
180'
142 144
VS1
z
y
x

FIG. 11

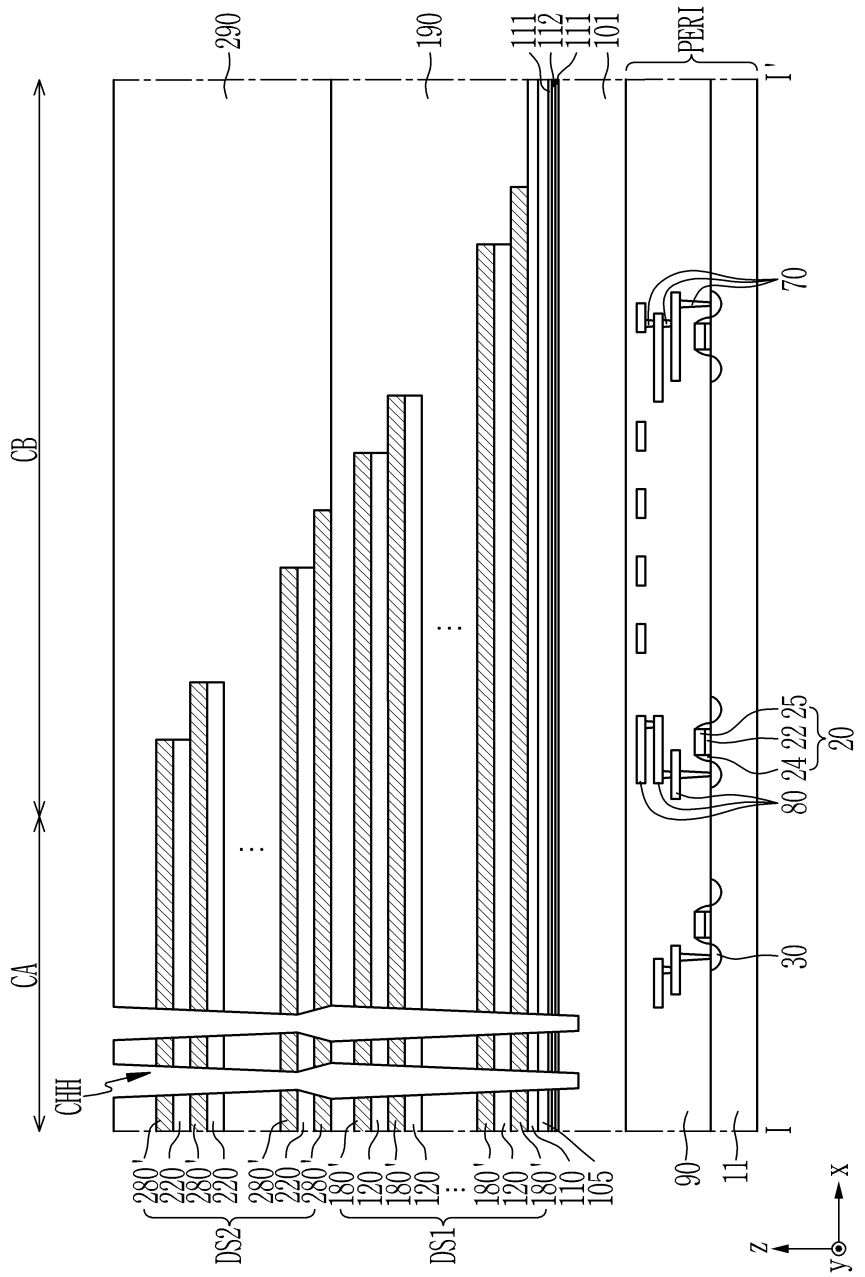

290
190
111
112
111
101
PERI
I'
CB
CA
CHH
70
80
24
22
25
20
30
280'
220'
280'
220'
280'
220'
280'
180'
120'
180'
120'
180'
120'
180'
110
105
DS2
DS1
90
11
I
z
y
x

FIG. 12

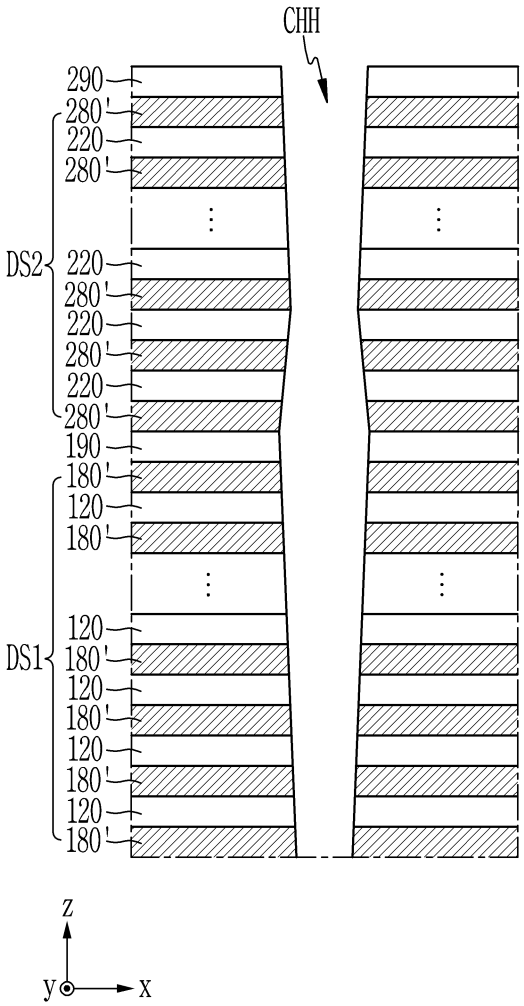

CHH
290
280'
220
280'
DS2
220
280'
220
280'
220
280'
190
180'
120
180'
DS1
120
180'
120
180'
120
180'
120
180'
z
y
x

FIG. 13

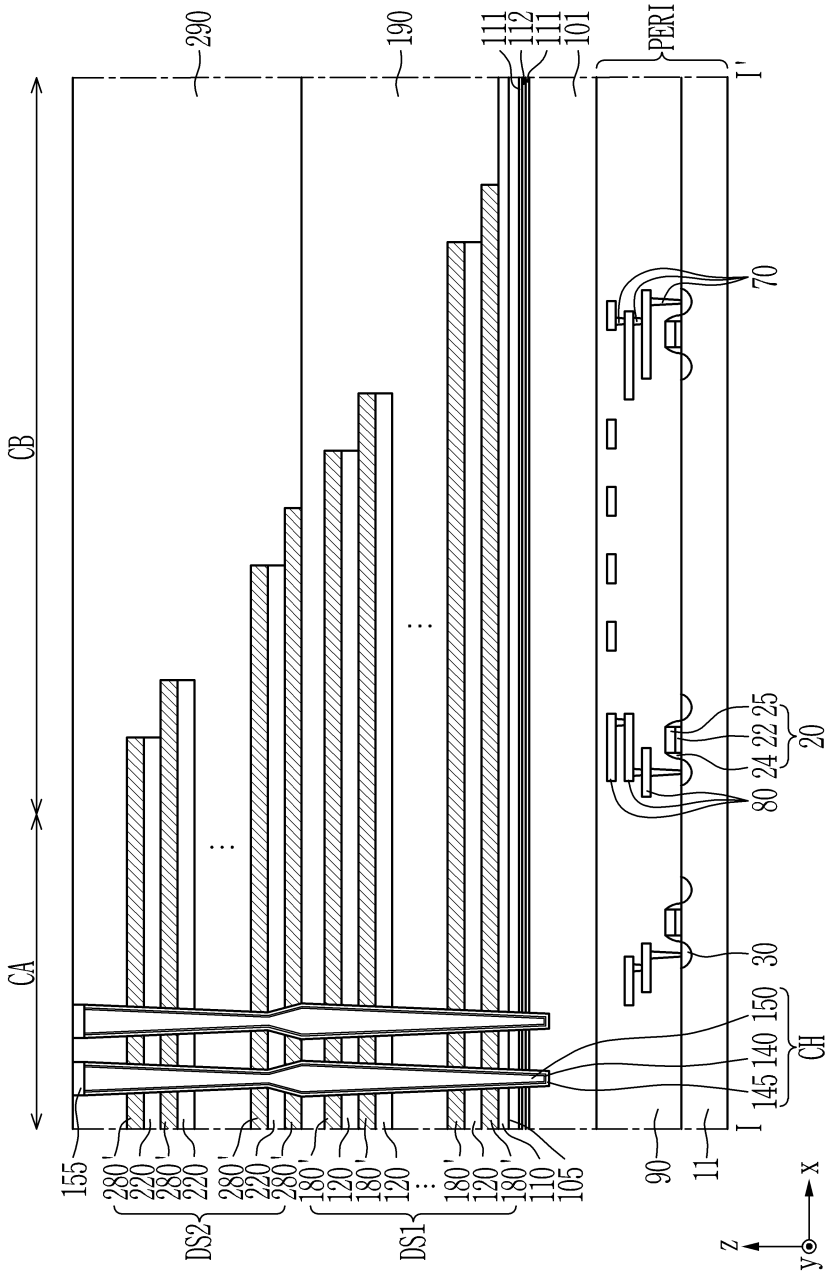

290
190
111
112
111
101
PERI
I'
CB
CA
70
25
22
24
80
20
30
150
140
145
CH
155
280'
220'
280'
220'
DS2
180'
120'
180'
120'
DS1
180'
120'
180'
110
105
90
11
I
z
y
x

FIG. 14

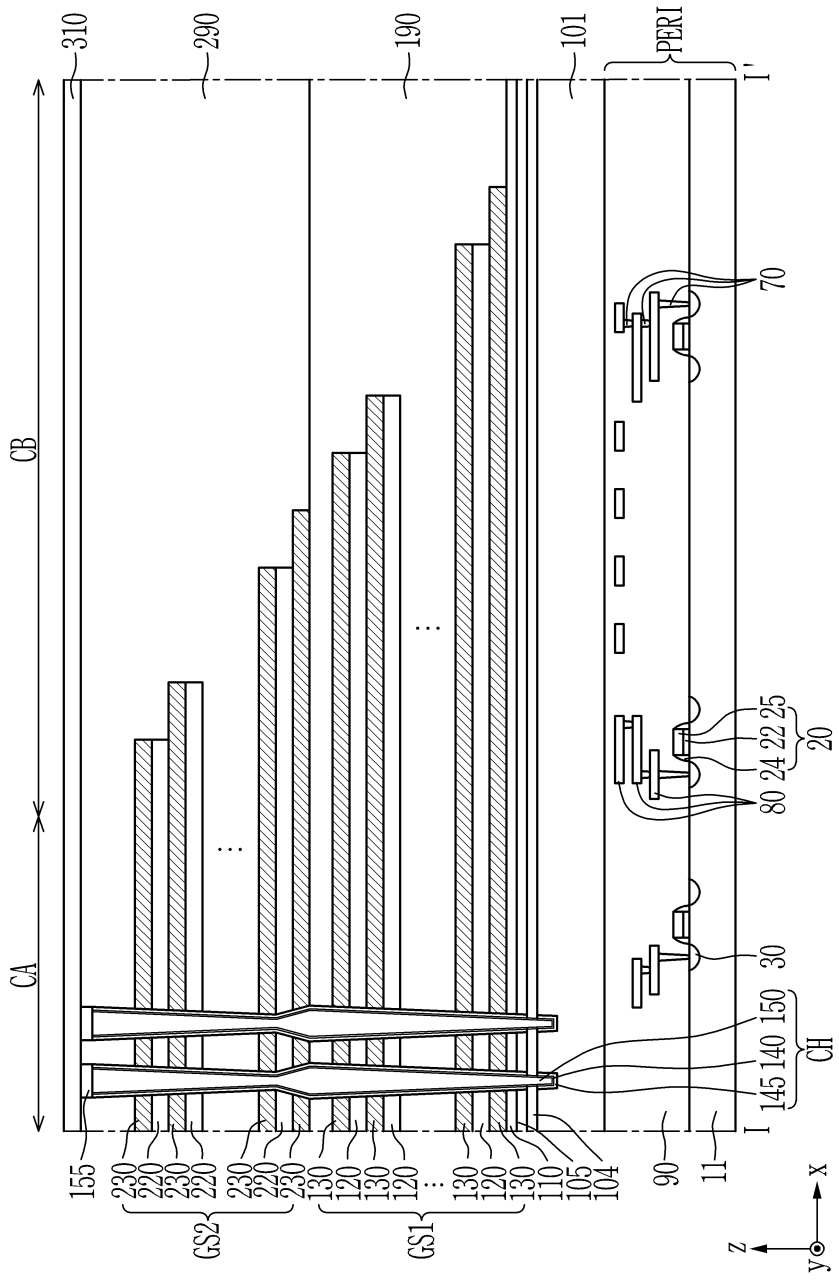

310
290
190
101
PERI
I'
CB
CA
70
80
24
22
25
20
30
150
140
145
CH
155
230
220
230
220
230
220
230
130
120
130
120
130
120
130
110
105
104
90
11
I
GS2
GS1
z
y
x

FIG. 15

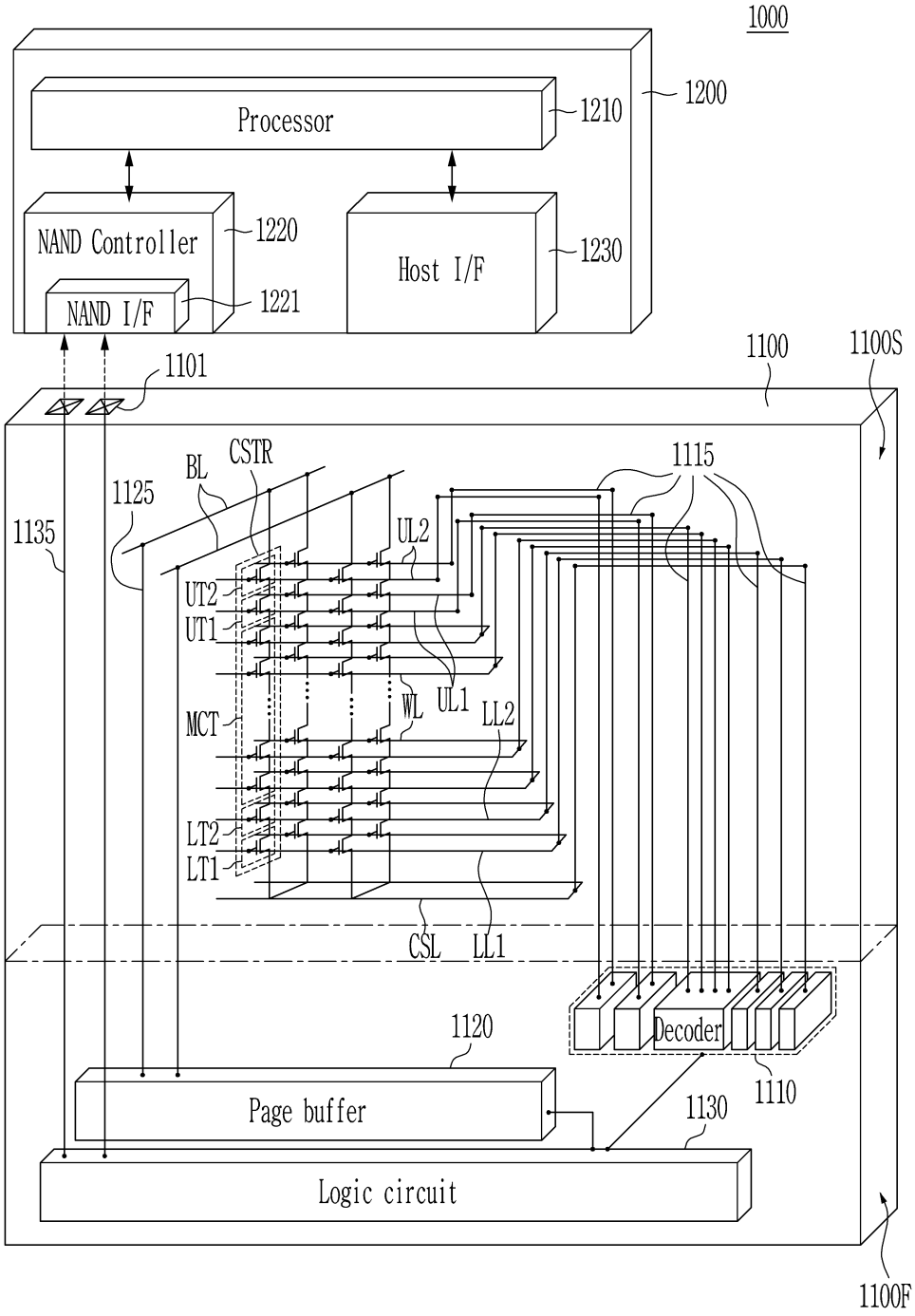

1000
Processor
1210
1200
NAND Controller
1220
Host I/F
1230
NAND I/F
1221
1100
1100S
1101
1115
BL
CSTR
1125
1135
UL2
UT2
UT1
MCT
WL
UL1
LL2
LT2
LT1
CSL
LL1
Decoder
1120
1110
Page buffer
1130
Logic circuit
1100F

FIG. 16

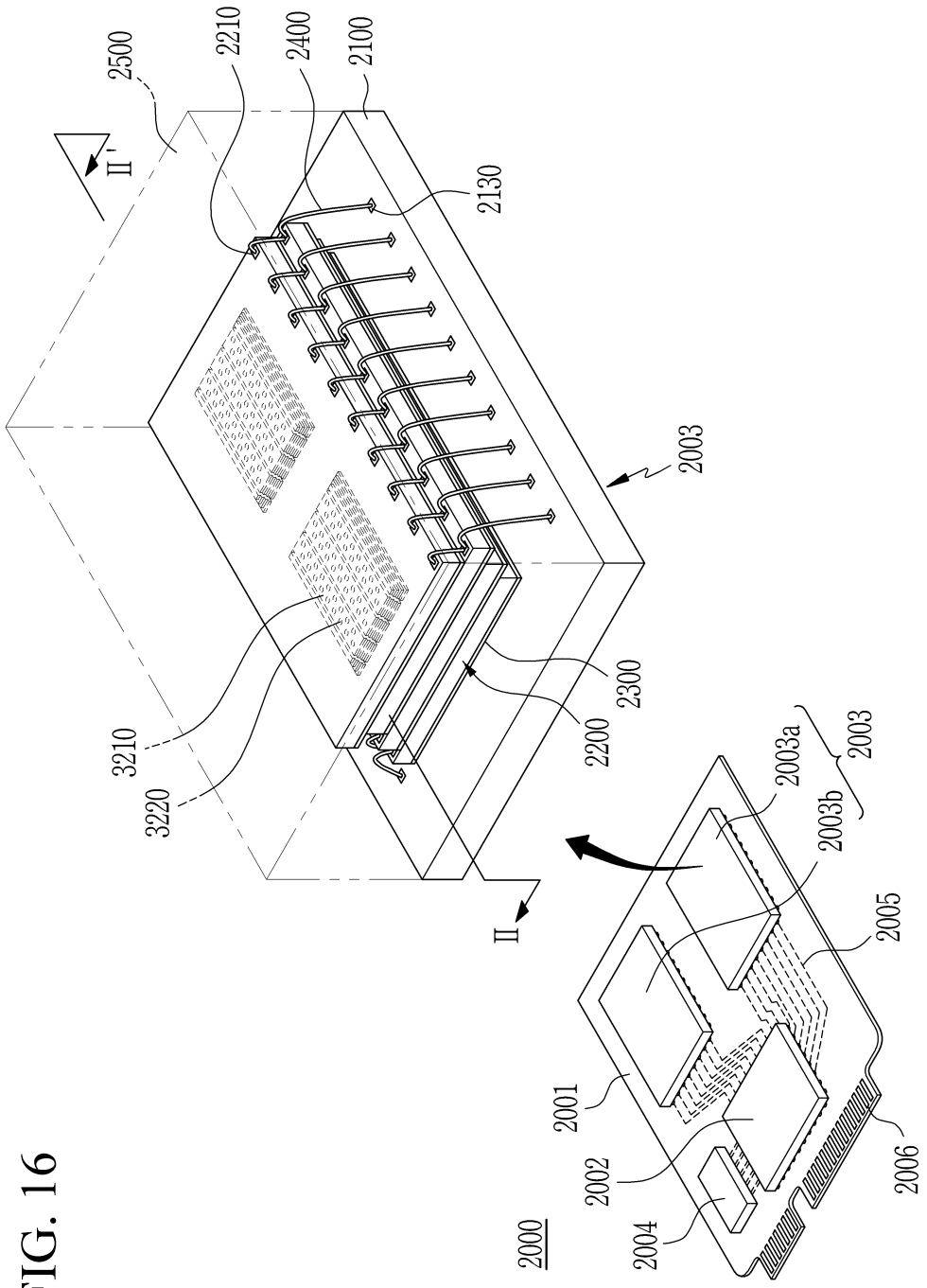

2500
2210
2400
2100
II'
2130
2003
3210
3220
2300
2200
II
2003a
2003b
2003
2005
2001
2002
2004
2006
2000

FIG. 17

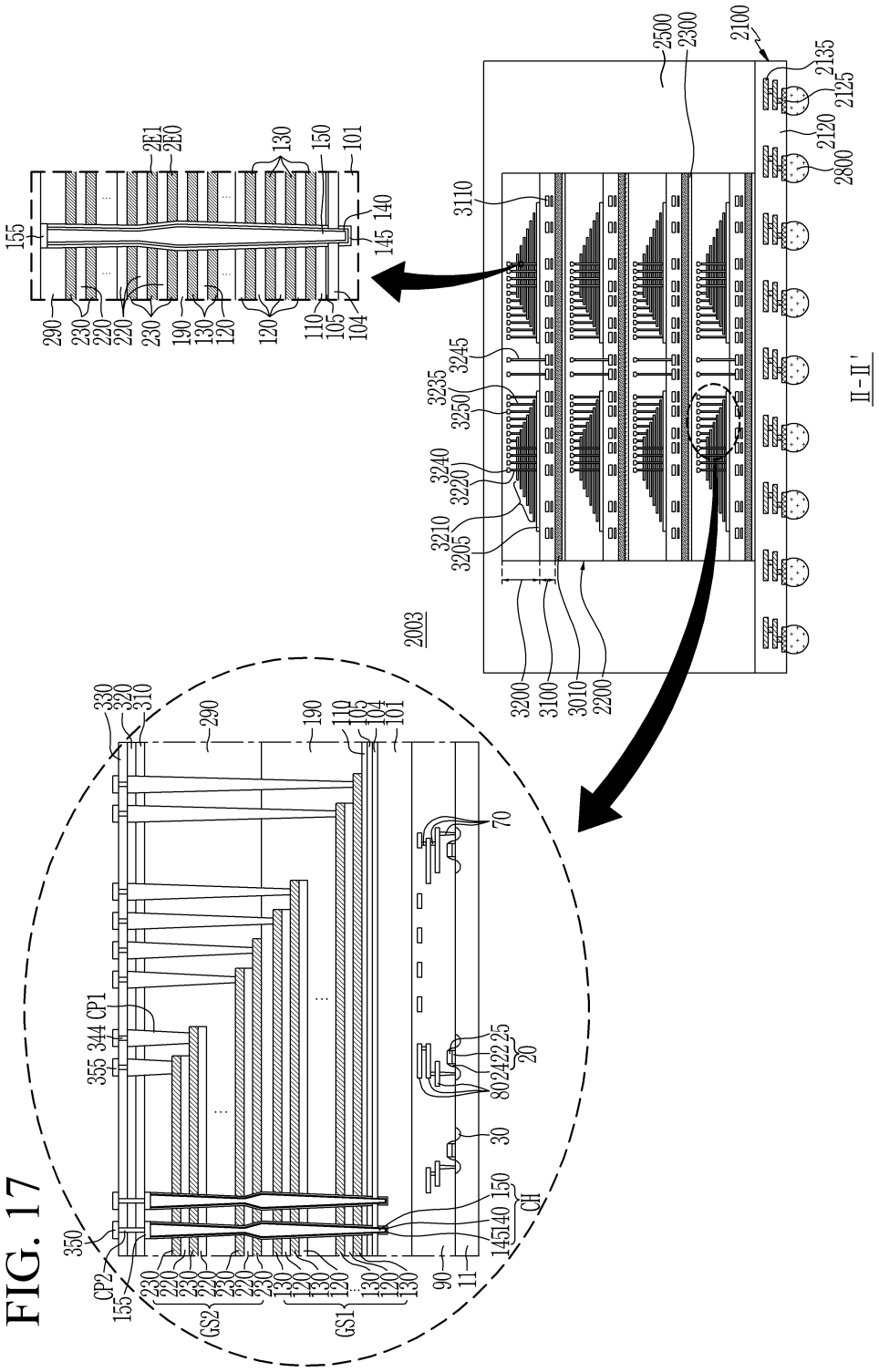
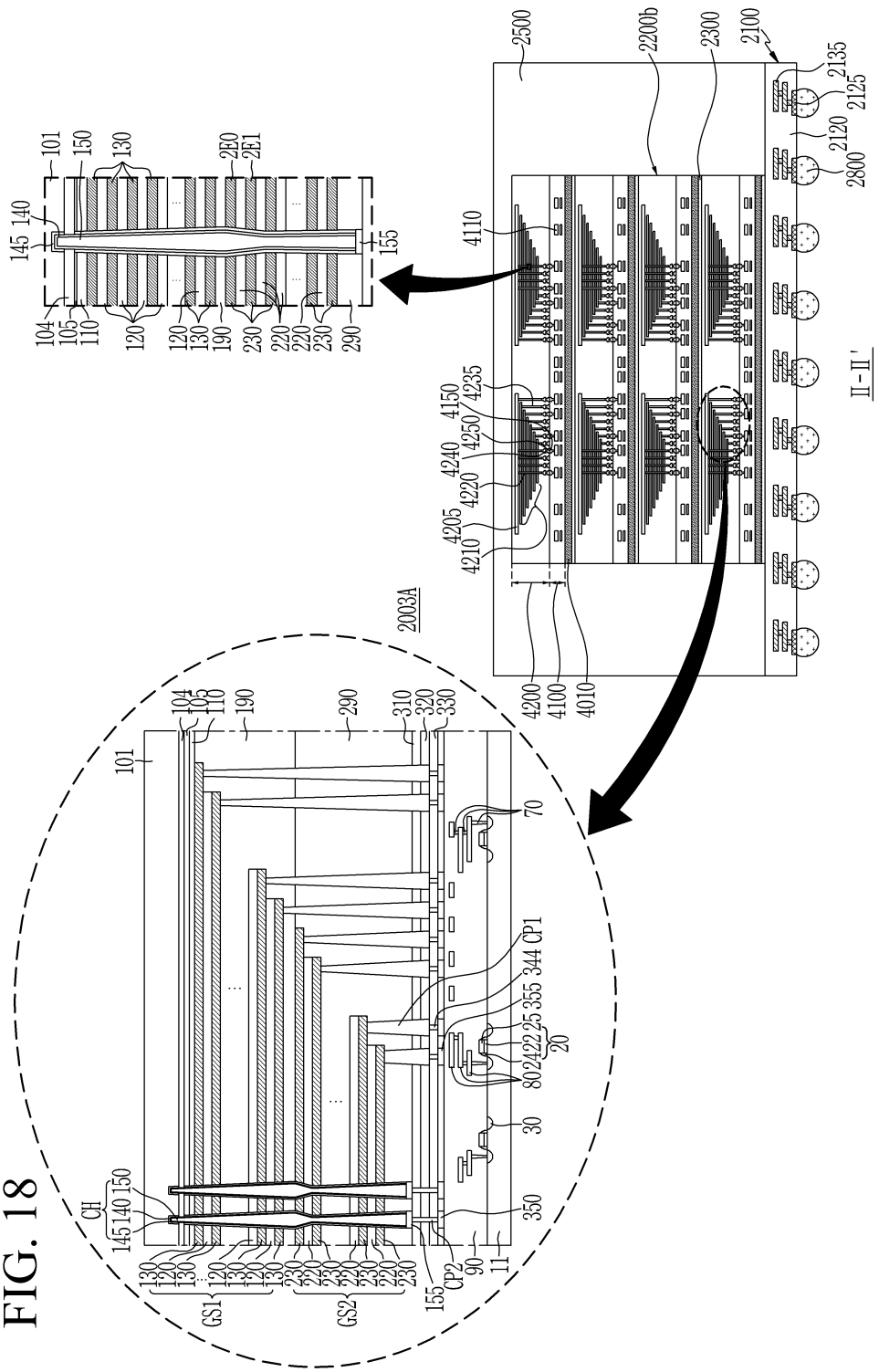

II-II'
2003
2100
2500
2300
2135
2125
2120
2800
3110
3245
3235
3250
3240
3220
3210
3205
3200
3100
3010
2200
155
290
230
220
220
230
190
130
120
120
110
105
104
2B1
2B0
130
150
101
140
145
330
320
310
290
190
110
105
104
101
70
355
344
CP1
25
22
20
80
30
150
CH
140
145
350
CP2
155
230
220
220
230
130
120
120
130
GS2
GS1
90
11

FIG. 18


2003A
II-II'
2500
2200b
2300
2100
2135
2125
2120
2800
4110
4150
4235
4240
4250
4220
4205
4210
4200
4100
4010
101
150
130
2E0
2E1
140
145
155
104
105
110
120
190
230
220
290
310
320
330
70
CP1
344
355
25
422
802
20
30
350
CH
CP2
90
11
GS1
GS2