

ELECTRONIC LIGHTING APPARATUS

TECHNICAL FIELD

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The present invention relates to an electronic lighting apparatus and in particular, to an electronic lighting apparatus suitable for being powered by an AC source or DC source.

10 BACKGROUND

Electronic lighting apparatus such as LED lamps are widely used in industrial and household environments to provide illuminations at night. Such LED lamps are typically powered by AC power supplies or DC power supplies such as batteries. In some applications where AC power supply is available, the lamps are powered by the AC source. In the event of power interruption or failure, the power source is switched to DC source to provide the lamps with continued illumination. Some conventional electronic lamps of such type require complicated electronics circuits, components, and multiple sets of batteries and/or lamps to adapt to both the AC and DC power supply source and to switch therebetween, upon detection of any power interruption. It is therefore desirable to provide an electronic apparatus with single light source suitable for both AC and DC sources with simple yet efficient control electronics circuits.

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BRIEF DESCRIPTION OF THE DRAWINGS

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These and other aspects of the present invention will be described in detail with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram illustrating AC soft start in accordance with one embodiment of the invention;

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Fig. 2 is a circuit diagram illustrating a manual switch in accordance with one embodiment of the invention;

Fig. 3 is a circuit diagram illustrating a digital switch in accordance with one embodiment of the invention;

Fig. 4 is a circuit diagram illustrating a time up circuit of the digital switch in accordance with one embodiment of the invention;

5 Fig. 5 illustrates a circuit diagram to detect power trip in accordance with one embodiment of the invention;

Fig. 6 illustrates a circuit diagram to detect power trip in accordance with one embodiment of the invention;

10 Fig. 7 illustrates a circuit diagram to detect power trip in accordance with one embodiment of the invention;

Fig. 8 illustrates a circuit diagram for attenuation in accordance with one embodiment of the invention;

Fig. 9 illustrates a circuit diagram for multiple attenuation in accordance with one embodiment of the invention;

15 Fig. 10 illustrates a circuit diagram for selecting AC in accordance with one embodiment of the invention;

Fig. 11 illustrates a circuit diagram for selecting AC in accordance with one embodiment of the invention;

20 Fig. 12 illustrates a circuit diagram for selecting AC in accordance with one embodiment of the invention;

Fig. 13 illustrates an overheating protection circuit in accordance with one embodiment of the invention;

Fig. 14 illustrates an overheating protection circuit in accordance with one embodiment of the invention;

25 Fig. 15 illustrates a circuit diagram of a power supply in accordance with one embodiment of the invention;

Fig. 16 illustrates a circuit diagram of an analog charger in accordance with one embodiment of the invention;

30 Fig. 17 illustrates a circuit diagram of a digital charger in accordance with one embodiment of the invention;

Fig. 18 illustrates a circuit diagram of a LED driver in accordance with one embodiment of the invention;

Fig. 19 illustrates a board diagram of an electronic lamp in accordance with one embodiment of the invention;

Fig. 20 illustrates a board diagram of LED driver in accordance with one embodiment of the invention;

5 Fig. 21 illustrates a board diagram of LED lamps in accordance with one embodiment of the invention;

Fig. 22 illustrates a board diagram of LED assembly in accordance with one embodiment of the invention;

10 Fig. 23 illustrates a board diagram of lamp adaptor in accordance with one embodiment of the invention;

Fig. 24 illustrates a board diagram of LED driver assembly holder in accordance with one embodiment of the invention;

Fig. 25 illustrates a board diagram of Light Dispersal Holder in accordance with one embodiment of the invention;

15 Fig. 26 illustrates a board diagram of the pogo pin and ground plate in accordance with one embodiment of the invention;

Fig. 27 illustrates an outline of the electronic lamp in accordance with one embodiment of the invention; and

20 Fig. 28 illustrates an isometric drawing of the electronic lamp in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the present invention are novel in at least the following aspects:

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(A) Auto single path of selecting power supply.

(B) Auto gain select with constant output for detection (compare to feedback to auto selecting the gain). It has a constant amplitude output. The output amplitude is control by selecting gain of the amplifier / attenuator. The feedback resistor in series in analog switch (ASW) can be extended to into multiple sets. The tradition amplifier / attenuator do not have this property. ($V_{out} = \frac{R_f}{R_{in}} * V_{in}$)

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(C) AC Soft Start or DC Soft Start, output supply is slowly transferred to the load to reduce current surge and prevent sudden drop in the supply. Tradition way, the output is fast direct applied to the load cause current surge and interrupts the supply. The effect is great when the load has low impendence. DC Soft Start or AC Soft Start can also act as a fuse / anti surge fuse. The current solution to this problem is to use anti surge fuse.

(D) Percent (%) Vi converter uses percentage or fraction to define the V_{IL} or V_{IH} . User can define its own V_{IL} or V_{IH} . User can also define it V_{OH} , V_{OL} is depend on V_{cc} or V_{ds} . Traditional the V_{IL} is smaller than 2.4V, the V_{IH} is greater than 3.5V. 2.4V to 3.5V is undefined. Currently those with Vcc equal to 3.3V the undefined state is smaller. It can be easily applied to the logic gate family.

AC Soft start

Figure 1 illustrates AC soft start in accordance with one embodiment of the invention.

$$\text{Equation } V_C = V[1 - e^{(-\frac{t}{RC})}]$$

The Hard Main In 102 supply negative cycle is block by the diode D131 108. The Hard Main In 102 is clamp by zener ZD131 112 to 50Vdc. The resistor R131 110 is the current limiting resistor. The zener ZD131 112 is parallel to R132 114 and the capacitor C131 118. The voltage developed at ZD131 112 becomes the charging source for R132 114 and the capacitor C131 118. The voltage is charged up by the equation V_C . The FET Q131 104 is just start to turn on when the V_C charges to the reverse break down of ZD132 116. The FET Q131 104 turn on slowly and the channel resistance of Q131 104 decreases slowly and the Hard Main In 102 voltage at Q131 104 (V_d) is transfer to Q131 104 source (V_s) (Main In voltage 106). When the FET Q131 104 is fully turned on the Hard Main In 102 voltage is equal to Q131 104 source (V_s) (Main In 106 voltage).

The ZD131 112 (mean constant voltage/current source) also help to produce same charging time (constant delay) for both 230Vac and 110Vac.

Manual Switch (SWM Manual)

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Alternative Circuit Digital Switch (SWD Digital)

Figure 2 illustrates a manual switch in accordance with one embodiment of the invention. When the manual switch 206 (SW1 DPDT) is closed the Main In 204 voltage flows from manual switch 206 (SW1 DPDT) pin 1 to pin 2 becomes AC In 210. At the same time the BatSWP2 202 voltage flows into switch SW1 206 (DPDT) pin3 to pin 4 becomes Bat 208. The Bat 208 is feed into Regulator 120 214 to produce 5V output. The output from the regulator 214 is used to charge the capacitor C123 218 via R125 216. The FET Q121 222 turns on when the V_C charges to the reverse break down of ZD121 220. The FET Q121 222 turn on slowly and the channel resistance of FET Q121 222 decreases slowly and the regulator voltage at FET Q121 222 (V_d) is transfer to FET Q121 222 source (V_s) (Bat5DC 224). When the FET Q121 222 is fully turned on the regulator 120 output voltage is equal to FET Q121 222 source (V_s) (Bat5DC 224).

Digital Switch (SWD Digital)

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Alternative Circuit Manual Switch (SWM Manual)

Figure 3 illustrates a digital switch in accordance with one embodiment of the invention. The Battery voltage 338 (BatSWP2) is supplied to the regulator 121 336. The output of the regulator 336 is used to charge the capacitor C123 332 via R125 334. The FET Q121 328 turns on when the V_C charges to the reverse break down of ZD121 330. The FET Q121 328 turn on slowly and the channel resistance of Q121 328 decreases slowly and the regulator voltage at Q121 328 (V_d) is transfer to Q121 328 source (V_s). When the FET Q121 328 is fully turned on the regulator voltage is equal to Q121 328 source (V_s). The regulator 121 output voltage is use to power on the AND1 364, NOR1 362, INV121 368 NAND1 366 and DFF1 370. Upon the D Flip Flop 316 (DFF1) receives

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the power, the logic of DFF1 316 are $D=0$, $Q=0$, $\bar{Q}=1$ as there will be no triggering. The DFF1 316 $\bar{Q}=1$ is inverted by an inverter INV121-2 308 to produce logic '0'. The output of INV121-2 308 is feed into the AND gate 314 (AND1-1). Since one of the input AND1-1 314 is '0' therefore the output of the AND1-1 314 is '0'. The DFF1 316 $Q=0$ and the output of (AND1-1 314) are feed into the two inputs NAND gate 326 (NAND1-2). The output of NAND1-2 326 is logic '1'. The relay 340 (RLY 121) does not energize so the contact remain normally closed (NC) position therefore no power is delivered to the RLY 121 340 pin 2 & 4. In this situation it does not depend on the ambient light.

When the press button switch 304 (SW121) is pressed, logic '0' is send into the input of NOR gate 306 (NOR1-2). Since both of the inputs of NOR1-2 306 are logic '0' therefore the output of the NOR1-2 306 is logic '1'. The output of the NOR1-2 306 triggers the DFF1 316 (+ve edge trigger) and changes the status of DFF1 316. The status of DFF1 316 become $D=1$, $Q=1$, $\bar{Q}=0$ The $\bar{Q}=0$ is inverted by an inverter INV121-2 308 to logic '1'. The output of INV121-2 308 is feed into the AND gate 314 (AND1-1), at this moment it depend on the other input of the AND1-1 314. Under the bright environment the phototransistor 310 conduct, the collector of phototransistor 310 (V_c) is zero means logic '0'. Since one of the inputs AND1-1 314 is logic '0' therefore the output of the AND1-1 314 is logic '0'. The DFF1 316 $Q=1$ and the output of (AND1-1 314) are feed into the two inputs NAND1-2 326. Since one of the inputs of the NAND1-2 326 is logic '0', therefore the output of NAND1-2 326 is logic '1'. The relay 340 (RLY 121) does not energize so the contact remain normally closed (NC) position therefore no power is delivered to the RLY 121 340 pin 2 & 4. In this situation the ambient light is bright.

Under the dark environment the phototransistor 310 does not conduct, the collector of phototransistor 310 (V_c) is 5v means logic '1'. The collector of phototransistor 310 (V_c) (logic '1') is feed into the input of the AND gate 314 (AND1-1), The DFF1 316 $\bar{Q}=0$ is inverted by an inverter INV121-2 308 to logic '1', now both input AND gate 314 (AND1-1) are logic '1' therefore the output of AND gate 314 (AND1-1) is logic '1'. Since both of the input NAND1-2 326 are logic '1' therefore the output of the NAND1-2 326 is

logic '0'. The relay 340 (RLY 121) energize, the contact move to normally open (NO) position therefore power is delivered to the RLY 121 340 pin 2 & 4. Main In 344 from RLY 121 340 pin1 flow to pin 2 become AC In 342. Battery voltage (BatSWP2) 338 from RLY 121 340 pin 3 flow to pin 4 become Bat 348. The Bat 348 is feed into Regulator 120 346 to produce 5V output. The output from the regulator 346 is used to charge the capacitor C123-1 356 via R125-1 358. The FET Q121-1 350 turns on when the V_C charges to the reverse break down of ZD121-1 354. The FET Q121-1 350 turn on slowly and the channel resistance of Q121-1 350 decreases slowly and the regulator voltage at Q121-1 350 (V_d) is transfer to Q121-1 350 source (V_s) become Bat5DC 352. When the FET Q121-1 350 is fully turned on the regulator 120 output voltage is equal to Q121-1 350 source (V_s) (Bat5DC 352). The Bat5DC 352 is use to power other components. In this situation the ambient light is dark.

One of the input of the Nor gate (NOR1-2) is tie to logic '0'. The other input depends on the switch (SW121) and the inverter INV121-1 via resistor R130. The inverter INV121-1 and the resistor does not have any effect when the switch (SW121) is not pressed because the Time up is logic '0' and is inverted by the inverter INV121-1 to produce logic '1'.

When the press button switch 304 (SW121) is pressed again logic '0' is send into the input of NOR gate 306 (NOR1-2). Since both of the inputs of NOR1-2 306 are logic '0' therefore the output of the NOR1-2 306 is logic '1'. The output of the NOR1-2 306 triggers the DFF1 (+ve edge trigger) and changes the status of DFF1. The status of DFF1 become $D='0'$, $Q='0'$, $Q \text{ bar}='1'$ The DFF1 316 $Q \text{ bar}='1'$ is inverted by an inverter INV121-2 308 to logic '0'. The output of INV121-2 308 is feed into the AND gate 314 (AND1-1). Since one of the input AND1-1 314 is '0' therefore the output of the AND1-1 314 is '0'. The output of the AND gate (AND1-1) and the DFF1 316 $Q='0'$ is feed into NAND1-2 gate 326 (NAND1-2). Since both of the inputs NAND1-2 326 are logic '0' therefore the output of the NAND1-2 326 is '1'. The relay 340 (RLY 121) does not energize so the contact move to normally closed (NC) position therefore no power is delivered to the RLY 121 340 pin 2 & 4. In this situation the power is cut off by the push button although the environment is dark.

The Time up signal is inverted by an inverter IVN121-1 to produce logic '0' to pull one of the input of the Nor gate (NOR1-2) to zero volt logic '0'. When the output of the inverter INV121-1 is at logic '0' the voltage drop the resistor R130 is almost zero volt (logic '0') because the R122 is much greater than R130. R122 and R130 form a potential divider when the inverter INV121-1 is at logic '0'.

When the press button switch 304 (SW121) is not pressed again and the time is up. The Time Up signal 318 is logic '1'. The Time up signal is inverted by the inverter INV121-1 to produce logic '0'. Since both of the inputs of NOR1-2 306 are '0' therefore the output of the NOR1-2 306 is '1'. The output of the NOR1-2 306 triggers the DFF1 316 (+ve edge trigger) and changes the status of DFF1 316. The status of DFF1 316 become D='0', Q='0', Q bar='1' The DFF1 316 Q bar='1' is inverted by an inverter INV121-2 308 to produce logic '0'. The output of INV121-2 308 is feed into the AND gate 314 (AND1-1). Since one of the input AND1-1 314 is '0' therefore the output of the AND1-1 314 is '0'. The DFF1 316 Q='0' is and the AND1-1 output 314 are feed into the two inputs NAND1-2 326. Since both of the inputs are logic '0' therefore output of NAND1-2 326 is logic '1'. The relay 340 (RLY 121) does not energize so the contact move to normally closed (NC) position therefore no power is delivered to the RLY 121 340 pin 2 & 4. In this situation the power cut off by timing although the environment is dark.

The push button is not press the Time Up circuit will not activate. The CLR 320 signal is at logic '0'. The push button is press the Time Up circuit activate. The CLR signal is at logic '1'.

Digital Switch Time Up Up <Note only used under SWD1-1> (SWD1-2 Time Up)

Figure 4 illustrates a time up circuit of the digital switch in accordance with one embodiment of the invention. When the power is first applied to the circuit, DECODE Out 420 initializes to logic '1'. The CLR 402 is at logic '0' and is inverted by the inverter 406 (INV141-1) and produce logic '1'. The raising edge of the of the RESET 426 (IC MC14536B 414) cause the DECODE Out 420 to go to logic '0' and remain logic '0' for

$2^n/2$ of the oscillator period, then it goes to logic '1'. The DECODE Out 420 is denote as Time Up. The R_s 408, C_x 424, R_{tc} 410 and the IC MC14536B 414 (OUT1 & OUT2) form an oscillator to provide a Clock signal for the Digital Charger2.

5 **Detect Pwr Trip (DPWRT1-Logic)**

Alternative Circuit DPWRT2 (Photo-couple), DPWRT3 (Infra-Red), DPWRT4 (Attenuation), DPWRT5 (Multi Attenuation).

10 Figure 5 illustrates a circuit diagram to detect power trip in accordance with one embodiment of the invention. The Main In supply 502 negative cycle is block by the diode D12 506 via fuse F1 504 and it is clamp to 4Vdc by ZD2 512. The resistor R41 508 is current limiting resistor. This voltage is hold by the capacitor C41 510 and is compared by the logic gate XOR1 514. The XOR1 514 detects the Main In 502 supply and produce an output denotes as No AC 516. The input to the XOR1 514 is 4Vdc (logic '1'), it produces
15 output logic '1' for the present of Main In 502 supply. The input to the XOR1 514 is 0 Vdc (logic '0'), it produce an output logic '0' for the absent of main supply [XOR1 514 Output logic '0' = No AC 516 present logic '1' AC present].

20 **Detect Pwr Trip (DPWRT2 -Photo-couple)**

Alternative Circuit DPWRT1(Logic), DPWRT3 (Infra-Red), DPWRT4 (Attenuation), DPWRT5 (Multi Attenuation).

25 Figure 6 illustrates a circuit diagram to detect power trip in accordance with one embodiment of the invention. The Main In supply 602 negative cycle is block by the diode D12 606 via fuse F1 604 and it is clamp to 4Vdc by ZD2 612. The zener ZD2 612 and the current limiting resistor R41 608 is parallel to R49 614 and the photo couple 1 LED 616. The voltage drop across the photo couple 1 LED 616 is greater than the thresh hold
30 therefore the photo couple 1 LED 616 is turn on. The light is couple to the phototransistor and the phototransistor is turn on. A 5v volt is produced at emitter (voltage drop across R48 622 is 5v). This 5v is feed to the input of XOR1-1 624 to produce output denote as

No AC 630. The No AC 630 at XOR1 624 output is logic '1' indicates the Main in 602 is present.

When the Main In supply 602 is absent there will be no voltage drop across the photo couple 1 LED 616 thus the photo couple 1 LED 616 turn off. No light is couple to the phototransistor and the phototransistor is turn off. Zero volts are produce at emitter (voltage drop across R48 622 is 0v). This zero volts is feed to the input of XOR1-1 624 feed to the input of XOR1-1 624 to produce a output logic '0'. The No AC 630 at XOR1 624 output is logic '0' indicate the Main in is absent.

[XOR1 624 Output logic '0'= No AC 630 present logic '1' AC present].

Detect Pwr Trip (DPWRT3 -Infra-Red)

Alternative Circuit (DPWRT1-Logic), DPWRT2 (Photo couple), DPWRT4 (Attenuation), DPWRT5 (Multi Attenuation)

Figure 7 illustrates a circuit diagram to detect power trip in accordance with one embodiment of the invention. The Main In supply 702 negative cycle is block by the diode D12 706 via fuse F1 704. The Main In supply 702 is clamp by zener ZD2 714 to 4Vdc. The zener ZD2 714 and the current limiting resistor R41 710 is parallel to R49 708 and the Infrared Emitting Diode 716. The voltage drop across the Infrared Emitting Diode 716 is greater than the thresh hold therefore the Infrared Emitting Diode 716 is turn on. The Infrared light is couple into the IR Receiver Modules 718 and the IR Receiver Modules 718 is turn on. Logic '0' is produced output pin1 and feed into input inverter 722 (INV4-1). The logic is inverted by INV4-1 722 and is used to detect the present of Main In supply 702 by the XOR1-1 724. The XOR1-1 724 produces an output denotes as No AC 726. The No AC 726 at XOR1 724 output is logic '1' indicate the Main in 702 is present.

When the Main In supply 702 is absent there will be no voltage drop across the Infrared Emitting Diode 716 thus the Infrared Emitting Diode 716 turn off. No light is couple to the IR Receiver Modules 718 and the IR Receiver Modules 718 is turn off.

Logic '1' is produced output pin1 and feed into input the inverter 722 (INV4-1). The logic is inverted by INV4-1 722 and is used to detect the present of MAIN IN 702 by the XOR1-1 724. This zero volts is feed to the input of XOR1-1 724 to produce a output logic '0', The No AC 726 at XOR1 724 output is logic '0' indicate the Main in 702 is absent.

5 [XOR1 724 Output logic '0'= No AC 726 present logic '1' AC present].

Detect Pwr Trip (DPWRT4 - Attenuation)

10 Alternative Circuit (DPWRT1-Logic), DPWRT2 (Photo couple), DPWRT3 (Infra-Red), DPWRT5 (Multi Attenuation)

Fig. 8 illustrates a circuit diagram for attenuation in accordance with one embodiment of the invention. The Main In supply 802 is attenuated by the op amp 822 (OP2-3) to constant amplitude sitting on a DC level regardless of the Main In supply 802 amplitude is 230Vac or 110Vac. The resistor 808 (R52) & resistor 810 (R53) provide a DC level (6Vdc) at the output op amp 822 (OP2-3). The Select AC 812 issue a SelG230/110 to the ASW1 814. The SelG230/110 812 is low level logic '0' a gain G230 (– R55/R51) is established as the ASW1 814 (L=Com & NC) are connected. The op amp 822 (OP2-3) produce an output (11.2Vpp sitting at 6Vdc). The SelG230/110 812 is high level logic '1' a gain G110 (– R54/R51) is established as the ASW1 814 (H=Com & NO) are connected. The op amp 822 (OP2-3) produce an output (11.2Vpp sitting at 6Vdc). The op amp 822 (OP2-3) output is $G_{230} \times \text{Main In } 802$ for 230Vac and $G_{110} \times \text{Main In } 802$ for 110Vac. The gain G230 and G110 are select by resistor R55 820 & R51 806 or R54 818 & R51 806 to produce the constant amplitude output. The constant amplitude output is passed through the capacitor 826 (C556) and the DC level is block by the capacitor 826 (C556). The diode 828 (D550) converts the constant amplitude output into half rectifier and is use to basis transistor 836 (Q550). The capacitor 832 (C551) is use to hold the DC level. The transistor 836 (Q550) conduct as the constant amplitude V_{dc} is greater the transistor V_{be} . Therefore the transistor 836 (Q550) collector V_c is zero volts (logic'0'). The transistor 836 (Q550) collector V_c is inverted by the inverter 842 (INV550-1). The inverter INV550-1 842 output is feed into the XOR1 844 to detect the present of Main In 802 and

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produce an output denotes as No AC 846. The No AC 846 at the output of XOR1 844 is logic '1' indicate the Main is present.

5 When the Main 802 is absent there will be no AC signal output at op amp 822 (OP2-3) except DC level (6Vdc). Since this DC level is blocked by capacitor 826 (C556), the V_{be} will be zero volt and the transistor 836 (Q550) will not conduct therefore the transistor 836 (Q550) collector V_c is Bat5DC 840 (Logic '1') The transistor 836 (Q550) collector V_c is inverted by the inverter 842(INV550-1). The inverter INV550-1 842 output is feed into the XOR1 844 to detect the present of Main In 802 and produce an output
10 denotes as No AC 846. The No AC 846 at the output of XOR1 844 is logic '0' indicate the Main is absent.

[XOR1 844 Output logic '0'= No AC present logic '1' AC present].

15 Note R550 830, R551 834, Q550 836, R552 838 & INV550-1 842 is solve the undefined state (2.4V to 3.4v)

The output from the D550 828 is applied to the resistor R550 830 and R551 834 which form the potential to basis the transistor Q550 836 when there is an input the
20 potential drop R551 834 will be half of the voltage at diode (-ve side). The transistor Q550 836 turn on and the potential drop R551 834 is pull to the V_{be} of Q550 836. The V_{ce} of the transistor Q550 836 will be zero volts (logic '0') and is inverter by an inverter INV550-1 842 logic '1'.

25 When there is no output from the D550 828, the potential drop R551 834 is zero volts therefore the V_{be} is zero volts and the transistor Q550 836 is turned off. The V_c of the transistor Q550 836 will be Bat5DC 840 (logic '1') volts and is inverted by an inverter INV550-1 842 to produce logic '0'.

30 The input of the INV550-1 842 is redefined (smaller than 0.7v is logic '0' at output of INV550-1 842, 0.7v to 1.78v is logic '1' at output of INV550-1 842). That is % V_i converter ($0.7/1.78 \times 100\% = 39.3\%$ is logic '0' and $[100-39.3] = 60.7\%$ is logic '1').

Detect Pwr Trip (DPWRT5 -Multi - Attenuation)

Alternative Circuit (DPWRT1-Logic), DPWRT2 (Photo couple), DPWRT3 (Infra-
5 Red), DPWRT4(Attenuation)

Fig. 9 illustrates a circuit diagram for multiple attenuation in accordance with one
embodiment of the invention. The Main In supply 902 is attenuated by the op amp 974
(OP2-3) to constant amplitude sitting on a DC level regardless of the Main In supply 902
10 amplitude is 230Vac or 110Vac. The resistor 908 (R52) & resistor 910 (R53) provide a
DC level (6Vdc) at the output op amp 974 (OP2-3). The Select AC (multiple comparisons)
issue SelG110 916, SelG230 914 & SelG330 912. At only one time only one type of gain
is selected.

15 The SelG110 916 is logic '1' a gain G110 930 ($-R54/R51$) is established as the
ASW1-1 922 (L=Com & NO) are connected. The op amp 974 (OP2-3) produce an output
(11.2Vpp sitting at 6Vdc). The other gain SelG230 914 & SelG330 912 are at logic '0'
The gain will not be established as the ASW1-2 920 & ASW1-3 918 are at normally close
position (NC) (L=Com & NC) that are not connected to resistor R55 & resistor R60
20 respectively.

The SelG230 914 is logic '1' a gain G230 928 ($-R55/R51$) is established as the
ASW1-2 920 (L=Com & NO) are connected. The op amp 974 (OP2-3) produce an output
(11.2Vpp sitting at 6Vdc). The other gain SelG110 916 & SelG330 912 are at logic '0'
25 The gain will not be established as the ASW1-1 916 & ASW1-3 912 are at normally close
position (NC) (L=Com & NC) that are not connected to resistor R54 & resistor R60
respectively.

The SelG330 is logic '1' a gain G330 926 ($-R60/R51$) is established as the
30 ASW1-3 918 (L=Com & NO) are connected. The op amp 974 (OP2-3) produce an output
(11.2Vpp sitting at 6Vdc). The other gain SelG110 916 & SelG230 914 are at logic '0'
The gain will not be established as the ASW1-1 916 & ASW1-2 914 are at normally close

position (NC) (L=Com & NC) that are not connected to resistor R54 & resistor R55 respectively.

5 The op amp 974 (OP2-3) output is $G_{230} \times \text{Main In}$ for 230Vac and $G_{110} \times \text{Main In}$ for 110Vac and $G_{330} \times \text{Main In}$ for 330Vac. The gain G_{330} 926 or G_{230} 928 or G_{110} 930 are select by resistor R60 & R51 or R55 & R51 or R54 & R51 to produce the constant amplitude output. The constant amplitude output is passed through the capacitor 932 (C556) and the DC level is block by the capacitor 932 (C556). The diode 934 (D550) converts the constant amplitude output into half rectifier and is use to basis transistor 946 (Q550). The capacitor 948 (C551) is use to hold the DC level. The transistor 946 (Q550) conduct as the constant amplitude V_{dc} is greater the transistor V_{be} . Therefore the transistor 946 (Q550) collector V_c is zero volts (logic'0'). The transistor 946 (Q550) collector V_c is inverted by the inverter 940 (INV550-1). The inverter INV550-1 940 output is feed into the XOR1 942 to detect the present of Main In 902 and produce an output denotes as No AC 944. The No AC 944 at the output of XOR1 942 is logic'1' indicate the Main 902 is present.

20 When the Main 902 is absent there will be no AC signal output at op amp 974 (OP2-3) except DC level (6Vdc). Since this DC level is blocked by capacitor 932 (C556), the V_{be} will be zero volt and the transistor 946 (Q550) will not conduct therefore the transistor 946 (Q550) collector V_c is Bat5DC 936 (Logic '1') The transistor 946 (Q550) collector V_c is inverted by the inverter 940 (INV550-1). The inverter INV550-1 940 output is feed into the XOR1 942 to detect the present of Main In 902 and produce an output denotes as No AC 944. The No AC at the output of XOR1 942 is logic '0' indicate the Main 902 is absent.

[XOR1 942 Output logic '0'= No AC 944 present logic '1' AC present].

30 Note R550 952, R551 950, Q550 946, R552 938 & INV550-1 940 is solve the undefined state (2.4V to 3.4v)

The output from the D550 934 is applied to the resistor R550 952 and R551 950 which form the potential to basis the transistor Q550 946 when there is an input the potential drop R551 950 will be half of the voltage at diode (-ve side). The transistor Q550 946 turn on and the potential drop R551 950 is pull to the V_{be} of Q550 946. The V_{ce} of the transistor Q550 946 will be zero volts (logic '0') and is inverter by an inverter INV550-1 940 logic '1'.

When there is no output from the D550 934, the potential drop R551 950 is zero volts therefore the V_{be} is zero volts and the transistor Q550 946 is turned off. The V_c of the transistor Q550 946 will be Bat5DC 936 (logic '1') volts and is inverter by an inverter INV550-1 940 to produce logic '0'.

The input of the INV550-1 940 is redefined (smaller than 0.7v is logic '0' at output of INV550-1 940, 0.7v to 1.78v is logic '1' at output of INV550-1 940). That is % Vi converter ($0.7/1.78 \times 100\% = 39.3\%$ is logic '0' and $[100-39.3] = 60.7\%$ is logic '1'.)

SELECT AC (SelAC1 – Logic)

Alternative (SelAC2 – Photo couple), (SelAC3 – Multi comparison)

Fig. 10 illustrates a circuit diagram for selecting AC in accordance with one embodiment of the invention.

For 230V _{ac} $V_{rms} = 0.707V_p$ $V_p = 230 \div 0.707 = 325.2V_p$ $V_{dc} = 0.318 \times 325.2 = 103.4V_{dc}$	For 110V _{ac} $V_{rms} = 0.707V_p$ $V_p = 110 \div 0.707 = 155.6V_p$ $V_{dc} = 0.318 \times 155.6 = 49.5V_{dc}$
Voltage drop across R58 $R58/(R58+R57) \times 103.4$ $5K/(5K+115K) \times 103.4 = 4.31V_{dc}$ $103.4/4.31 = 24 \text{ time}$	Voltage drop across R58 $R58/(R58+R57) \times 49.5$ $5K/(5K+115K) \times 49.5 = 2.06V_{dc}$ $49.5/2.06 = 24 \text{ time}$

The AC In supply 1002 ($230V_{ac}$) negative cycle is block by the diode D11 1004. The voltage is step down by approximate 24 times by the potential divider (Resistor R57 1006 & R58 1010). The capacitor C42 1008 holds the voltage and is feed into the inverter INV1-4 1012 to invert the logic. The inverter INV1-4 1012 controls the relay RLY3 1016 to switch the AC In 1020 to 230AC or 110AC. At the same time the inverter INV1-4 1012 also output a gain select signal denote as SelG230/110 1022. The inverter INV1-4 1012 output is at logic '0', the relay RLY3 1016 energize, the relay RLY3 1016 switch to normally open (NO) position, the AC In 1020 become 230AC.

The AC In supply 1002 ($110V_{ac}$) negative cycle is block by the diode D11 1004. The voltage is step down by approximate 24 times by the potential divider (Resistor R57 1006 & R58 1010). The capacitor C42 1008 holds the voltage and is feed into the inverter INV1-4 1012 to invert the logic. The inverter INV1-4 1012 controls the relay RLY3 1016 to switch the AC In 1020 to 230AC or 110AC. At the same time the inverter INV1-4 1012 also output a gain select signal denote as SelG230/110 1022. The inverter INV1-4 1012 output is at logic '1', the relay RLY3 1016 de-energize, the relay RLY3 1016 switch to normally closed (NC) position, the AC In 1020 become 110AC.

[INV1-4 1012 Output logic '0'= 230Vac is selected logic '1'= 110Vac is selected].

SELECT AC (SelAC2 – Photo couple)

Alternative (SelAC1 – Logic), (SelAC3 – Multi comparison)

Fig. 11 illustrates a circuit diagram for selecting AC in accordance with one embodiment of the invention.

For $230V_{ac}$	For $110V_{ac}$
$V_{rms} = 0.707V_p$	$V_{rms} = 0.707V_p$
$V_p = 230 \div 0.707 = 325.2V_p$	$V_p = 110 \div 0.707 = 155.6V_p$
$V_{dc} = 0.318 \times 325.2 = 103.4V_{dc}$	$V_{dc} = 0.318 \times 155.6 = 49.5V_{dc}$

Voltage drop across R58 $R58/(R58+R57) \times 103.4$ $5K/(5K+115K) \times 103.4 = 4.31V_{dc}$ $103.4/4.31 = 24 \text{ time}$	Voltage drop across R58 $R58/(R58+R57) \times 49.5$ $5K/(5K+115K) \times 49.5 = 2.06V_{dc}$ $49.5/2.06 = 24 \text{ time}$
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The AC In supply 1102 (230Vac) negative cycle is block by the diode D11 1104. The voltage is step down by approximate 24 times by the potential divider (Resistor R57 1106 & R58 1110). The capacitor C42 1108 holds the voltage. The voltage across the resistor R58 1110 is parallel to ZD10 1134 and the photo couple 2 LED 1114.

The AC In 1102 is 230V_{ac} the voltage drop across resistor R58 1110 is 4.31V_{dc}. After the zener ZD10 1134 drop the voltage is greater than the thresh hold voltage of the photo couple 2 LED 1114, therefore the photo couple 2 LED is turn on. The light is couple to the phototransistor and the phototransistor is turn on. A 5v volt is produced at emitter (voltage drop across R59 1120 is 5v). This 5v logic '1' is feed to the input of inverter INV1-4 1122 and is inverted by inverter INV1-4 1122. At the same time the inverter INV1-4 1122 also output a gain select signal denote as SelG230/110 1124. The inverter INV1-4 1122 controls the relay RLY3 1128 to switch the AC In 1020 to 230AC or 110AC. The inverter INV1-4 1122 output is at logic '0', the relay RLY3 1128 energize, the relay RLY3 1128 switch to normally open (NO) position, the AC In 1132 become 230AC.

The AC In supply 1102 (110V_{ac}) negative cycle is block by the diode D11 1104. The voltage is step down by approximate 24 times by the potential divider (Resistor R57 1106 & R58 1110). The capacitor C42 1108 holds the voltage. The voltage across the resistor R58 1110 is parallel to ZD10 1134 and the photo couple 2 LED 1114.

The AC In 1102 is 110V_{ac} the voltage drop across resistor R58 1110 is 2.06V_{dc}. After the zener ZD10 1134 drop the voltage is smaller than the thresh hold voltage of the photo couple 2 LED 1114, therefore the photo couple 2 LED is turn off. No light is couple to the phototransistor and the phototransistor is turn off. A 0v volt is produced at emitter (voltage drop across R59 1120 is 0v). This 0v logic '0' is feed to the input of inverter

INV1-4 1122 and is inverted by inverter INV1-4 1122. At the same time the inverter INV1-4 1122 also output a gain select signal denote as SelG230/110 1124. The inverter INV1-4 1122 controls the relay RLY3 1128 to switch the AC In 1132 to 230AC or 110AC. The inverter INV1-4 1122 output is at logic '1', the relay RLY3 1128 de-energize, the relay RLY3 1128 switch to normally closed (NC) position, the AC 1132 In become 110AC.

[INV1-4 1122 Output logic '0'= 230Vac is selected logic '1'= 110Vac is selected].

SELECT AC (SelAC3 – Multi comparison)

Alternative (SelAC1 – Logic), (SelAC2 – Photo couple)

Fig. 12 illustrates a circuit diagram for selecting AC in accordance with one embodiment of the invention.

For 230V_{ac} $V_{rms} = 0.707V_p$ $V_p = 230 \div 0.707 = 325.2V_p$ $V_{dc} = 0.318 \times 325.2 = 103.4V_{dc}$	For 110V_{ac} $V_{rms} = 0.707V_p$ $V_p = 110 \div 0.707 = 155.6V_p$ $V_{dc} = 0.318 \times 155.6 = 49.5V_{dc}$
Voltage drop across R58 $R58/(R58+R57) \times 103.4$ $5K/(5K+115K) \times 103.4 = 4.31V_{dc}$ $103.4/4.31 = 24 \text{ time}$	Voltage drop across R58 $R58/(R58+R57) \times 49.5$ $5K/(5K+115K) \times 49.5 = 2.06V_{dc}$ $49.5/2.06 = 24 \text{ time}$

The AC In 1202 supply negative cycle is block by the diode D11 1204. The voltage is step down by 24 times by the potential divider (Resistor R57 1206 & R58 1210). The capacitor C42 1208 holds the voltage.

Three set of comparator (R560 1214, OP5-3 1220, R561 1216, OP5-2 1224, R562 1218, and OP5-1 1226) are used to detect the amplitude of AC In 1202. The XOR gate (XOR5-3 1228, XOR5-2 1230, and XOR5-1 1232) will determine which path of gain to be selected.

When the Ac In is 110 is the OP5-1 1226 V+ is greater than the V- , the output of the OP5-1 1226 is high (logic '1'), the OP5-2 1224 V+ is smaller than the V- the output of the OP5-2 1224 is low (logic '0'), the OP5-3 1220 V+ is smaller than the V- the output of the OP5-3 1220 is low (logic '0'). The output of OP5-1 1226 and OP5-2 1224 are feed into the XOR5-1 1232. The output XOR5-1 1232 produce logic '1' (SelG110 1238) therefore the gain SelG110 1238 is selected. The output of OP5-2 1224 and OP5-3 1220 are feed into the XOR5-2 1230. The output XOR5-2 1230 produce logic '0' (SelG230 1236) therefore the gain SelG230 1236 is not selected. The output of OP5-3 1220 and GND (logic'0') are feed into the XOR5-3 1228. The output XOR5-3 1228 produce logic '0' (SelG330 1234) therefore the gain SelG330 1234 is not selected.

When the Ac is 230 is the OP5-1 1226 V+ is greater than the V- , the output of the OP5-1 1226 is high (logic '1'), the OP5-2 1224 V+ is greater than the V- the output of the OP5-2 1224 is high (logic '1'), the OP5-3 1222 V+ is smaller than the V- the output of the OP5-3 1222 is low (logic '0'). The output of OP5-1 1226 and OP5-2 1224 are feed into the XOR5-1 1232. The output XOR5-1 1232 produce logic '0' (SelG110 1238) therefore the gain SelG110 1238 is not selected. The output of OP5-2 1224 and OP5-3 1222 are feed into the XOR5-2 1230. The output XOR5-2 1230 produce logic '1' (SelG230 1236), therefore the gain SelG230 1236 is selected. The output of OP5-3 1228 and GND (logic'0') are feed into the XOR5-3 1228. The output XOR5-3 1228 produce logic '0' (SelG330 1234) therefore the gain SelG330 1234 is not selected.

When the Ac is 330 is the OP5-1 1226 V+ is greater than the V- , the output of the OP5-1 1226 is high (logic '1'), the OP5-2 1224 V+ is greater than the V- the output of the OP5-2 1224 is high (logic '1'), the OP5-3 1220 V+ is greater than the V- the output of the OP5-3 1220 is high (logic '1'). The output of OP5-1 1226 and OP5-2 1224 are feed into the XOR5-1 1232. The output XOR5-1 1232 produce logic '0' (SelG110 1238) therefore the gain SelG110 1238 is not selected. The output of OP5-2 1224 and OP5-3 1220 are feed into the XOR5-2 1230. The output XOR5-2 1230 produce logic '0' (SelG230 1236) therefore the gain SelG230 1236 is not selected. The output of OP5-3 1220 and GND

(logic'0') are feed into the XOR5-3 1228. The output XOR5-3 1228 produce logic '1' (SelG330 1234) therefore the gain SelG330 1234 is selected.

[<SelG110 1238 = logic '1' = gain selected, SelG110 1238 = logic '0' = gain not selected>, <SelG230 1236 = logic '1' = gain selected, SelG230 1236 = logic '0' = gain not selected>, <SelG330 1234 = logic '1' = gain selected, SelG330 1234 = logic '0' = gain not selected>]

OVER HEATING PROTECTION (OHP – Analog)

Alternative OHP-Digital

Fig. 13 illustrates an overheating protection circuit in accordance with one embodiment of the invention. The op amp OP2-4 1310, resistor R61 1302, R62 1306, R63 1308, the thermistor TH61 1304, both the field effect transistor Q41 1316 form the overheat detection circuit. The thermistor 1304 has a negative temperature coefficient. The ambient temperature is set to approximate 70°C. The ambient temperature is smaller than the set temperature the OP2-4 1310 V+ is greater than V-; the output of the OP2-4 1310 is high. It is then feed to a potential divider resistor R64 1312 and R66 1314 to turn the Q41 1316. The R64 1312 and R66 1314 is biased at the V_{gs} thresh hold voltage. The Q41 1316 is turned on the voltage from Q41 1316 V_d (Pt B1 1318) equal to V_s (Pt V_z 1320). The ambient temperature is greater than the set temperature the OP2-4 1310 V+ is smaller than V-; the output of the OP2-4 1310 is low. The Q41 1316 V_g is zero volt the Q41 1316 is turn off. The Q41 1316 V_d voltage is Pt B1 1318 and the voltage V_s is zero volts (Pt V_z 1320).

OVER HEATING PROTECTION (OHP-Digital)

Alternative OHP – Analog

Fig. 14 illustrates an overheating protection circuit in accordance with one embodiment of the invention.

For AC 230 or 110

The electronic lamp is in normal operation the Pt V_z 1402 voltage is 21.5v. This voltage is feed to the ZD171 1410 via resistor R173 1412 and ZD173 1406 via resistor R174 1404. The ZD171 1410 is open as the voltage is smaller than the reverse break down voltage; the voltage drop across the ZD172 1414 is 21.5v as the result the V_{gs} is zero volts therefore the Q171 1416 is cut off (V_{gs} is smaller than the thresh hold of Q171 1416) thus the V_d of Q171 1416 is Bat5DC 1420 voltage (logic '1'). The ZD173 1406 clamp this voltage to 15.5v. The voltage is drop across the ZD174 1470 is 13.5v leaving 2v drop across the V_{gs} of Q172 1424 therefore the Q172 1424 is turn on (V_{gs} is greater than the thresh hold of Q172 1424) thus the V_d of Q172 1424 is zero volts (logic '0'). This logic is inverter by the inverter INV171-1 1426 to get logic '1'. The V_d of Q171 1416 (logic '1') and the output of the inverter INV171-1 1426 (logic '1') are feed into the two input AND gate 1428 (AND 171-1) to get logic '1'. The AND 171-1 1428 output is denotes as AND171-1Out 1430.

The Pt V_z 1402 is over voltage that is greater than 24v. This voltage is feed to the ZD171 1410 via resistor R173 1412 and ZD173 1406 via resistor R174 1404. The ZD171 1410 clamp this voltage to 24v. The voltage is drop across the ZD172 1414 is 21.5v leaving 2.5v drop across the V_{gs} of Q171 1416 therefore the Q171 1416 is turn on (V_{gs} is greater than the thresh hold of Q171 1416) thus the V_d of Q171 1416 is zero volts (logic '0'). The ZD173 1406 clamp this voltage to 15.5v. The voltage is drop across the ZD174 1470 is 13.5v leaving 2v drop across the V_{gs} of Q172 1424 therefore the Q172 1424 is turn on (V_{gs} is greater than the thresh hold of Q172 1424) thus the V_d of Q172 1424 is zero volts (logic '0'). This logic is inverter by the inverter INV171-1 1426 to get logic '1'. The V_d of Q171 1424 and the output of the inverter INV171-1 1426 are feed into the two input AND gate 1428 (AND 171-1) to get logic '0'. The AND 171-1 1428 output is denotes as AND171-1Out 1430.

The Pt V_z 1402 is under voltage that is smaller than 15.5v. The ZD171 1410 is open as the voltage is smaller than the reverse break down voltage; the ZD172 1414 is

open as the voltage is smaller than the reverse break down voltage and the V_{gs} is zero volts therefore the Q171 1416 is cut off (V_{gs} is smaller than the thresh hold of Q171 1416) thus the V_d of Q171 1416 is Bat5DC 1420 voltage (logic '1'). The ZD173 1406 is open as the voltage is smaller than the reverse break down voltage; the voltage drop across the ZD174 1470 is 13.5v leaving 1.9v drop across the V_{gs} of Q172 1424 therefore the Q172 1424 cut off (V_{gs} is smaller than the thresh hold of Q172 1424) thus the V_d of Q172 1424 is Bat5DC 1420 voltage (logic '1'). This logic is inverter by the inverter INV171-1 1426 to get logic '0'. The V_d of Q171 1416 and the output of the inverter INV171-1 1426 are feed into the two input AND gate 1426 (AND 171-1) to get logic '0'. The AND 171-1 1426 output is denotes as AND171-1Out 1430.

For battery

The electronic lamp is in power trip operation (battery is in normal operation) the battery voltage via switch SW122 is Bat 1408 (12v). This voltage is feed to the ZD175 1462 via resistor R177 1464 and ZD177 1468 via resistor R178 1466. The ZD175 1462 is open as the voltage is smaller than the reverse break down voltage; the voltage is drop across the ZD176 1460 is 12.4v as the result the V_{gs} is zero volts therefore the Q173 1458 is cut off (V_{gs} is smaller than the thresh hold of Q173 1458) thus the V_d of Q173 1458 is Bat5DC voltage (logic '1'). The ZD177 1468 clamp this voltage to 9v. The voltage is drop across the ZD178 1456 is 7.0v leaving 2v drop across the V_{gs} of Q174 1450 therefore the Q174 1450 is turn on (V_{gs} is greater than the thresh hold of Q174 1450) thus the V_d of Q174 1450 is zero volts (logic '0'). This logic is inverter by the inverter INV171-2 1448 to get logic '1'. The V_d of Q173 1458 and the output of the inverter INV171-2 1448 are feed into the two input AND gate 1446 (AND 171-2) to get logic '1'. The AND 171-2 1446 output is denotes as AND171-2Out 1444.

When the battery voltage via switch SW122 (Bat) is over voltage. That is greater than 14.4. This voltage is feed to the ZD175 1462 via resistor R177 1464 and ZD177 1468 via resistor R178 1466. The ZD175 1462 clamp this voltage to 14.4v. The voltage is drop across the ZD176 1460 is 12.4v leaving 2v drop across the V_{gs} of Q173 1458 therefore the Q173 1458 is turn on (V_{gs} is greater than the thresh hold of Q173 1458) thus the V_d of

Q173 1458 is zero volts (logic '0'). The ZD177 1468 clamp this voltage to 9v. The voltage is drop across the ZD178 1456 is 7v leaving 2v drop across the V_{gs} of Q174 1450 therefore the Q174 1450 is turn on (V_{gs} is greater than the thresh hold of Q174 1450) thus the V_d of Q174 1450 is zero volts (logic '0'). This logic is inverter by the inverter
5 INV171-2 1448 to get logic '1'. The V_d of Q173 1458 and the output of the inverter INV171-2 1448 are feed into the two input AND gate 1446 (AND 171-2) to get logic '0'. The AND 171-2 1446 output is denotes as AND171-2Out 1444.

When the battery voltage via switch SW122 (Bat) is under voltage. That is smaller
10 than 9v. The ZD175 1462 is open as the voltage is smaller than the reverse break down voltage; the ZD176 1460 is open as the voltage is smaller than the reverse break down voltage and the V_{gs} is zero volts therefore the Q173 1458 is cut off (V_{gs} is smaller than the thresh hold of Q173 1458) thus the V_d of Q173 1458 is Bat5DC voltage (logic '1'). The ZD177 1468 is open as the voltage is smaller than the reverse break down voltage; the
15 voltage drop across the ZD178 1456 is 7v leaving 1.9v drop across the V_{gs} of Q174 1450 therefore the Q174 1450 cut off (V_{gs} is smaller than the thresh hold of Q174 1450) thus the V_d of Q174 1450 is Bat5DC voltage (logic '1'). This logic is inverted by the inverter INV171-2 1448 to get logic '0'. The V_d of Q173 1458 and the output of the inverter INV171-2 1448 are feed into the two input AND gate 1446 (AND 171-2) to produce logic
20 '0'. The AND 171-2 1446 output is denotes as AND171-2Out 1444.

The No AC signal is feed into the inverter INV173-3 to produce an inverted logic. The output of the inverter INV173-3 and the AND171-1 Out are feed into the OR gate OR171-1 to produce an output denotes as OR171-1 Out.

25 The No AC signal is at logic '1' (supply present), this No AC signal is inverted by the inverter INV173-3 to produce logic '0'. Since one of the input of the OR gate OR171-1 is at logic '0', the output of the OR gate OR171-1 (OR171-1 Out) depend on the AND171-1 Out signal.

30 Under normal condition the OR171-1 Out is at logic '1' as the AND171-1 Out signal input logic '1' to the OR171-1.

When the supply is under/over voltage the OR171-1Out is at logic '0' as the AND171-1Out signal input logic '0' to the OR171-1.

5 The No AC signal is at logic '0' (supply absent) this No AC signal is inverted by the inverter INV173-3 to produce logic '1'. Since one of the input of the OR gate OR171-1 is at logic '1' the output of the OR gate OR171-1 (OR171-1Out) is at logic '1'.

Note the inverter INV171-3 and OR171-1 and distinguish it is an over/under voltage or the supply is present/absent.

10 The OR gate OR171-1Out and AND172-1Out are feed into AND171-3 to produce an output to turn on Q41 so that the Voltage can flow from PT B1 to Pt Vz. Both the OR171-1Out and AND171-2Out are at logic '1', the Q41 will be turn on as the Vgs is basis greater than the thresh hold voltage by resistor R64 and R66.

PWR Supply

Fig. 15 illustrates a circuit diagram of a power supply in accordance with one embodiment of the invention. This is a power source that can accept three types of input. 20 Firstly is the AC 230V_{ac} 1508 input. Secondly is the AC 110V_{ac} 1510 input. Thirdly is the DC input (Bat 1514). The transformer 1512 accept two type of AC (230/110 AC) input and is step down to 21.5V_{rms} +/- 10%. The bridge (B1) 1520 is a full wave rectifier that converts both type of AC to DC.

25 Under normal operation the power supply accepts a No AC (logic '1') 1502 signal from Detect Pwr Trip. This No AC signal 1502 is inverted by the inverter INV1-6 1504 to energize the relay (RLY 4) 1516. The relay (RLY 4) 1516 is energized, the contact is switched to the normally open (NO) position, this allow the stepped down to flow to the bridge (B1) 1520.

30 At the same time the Pt Vz flows to the regulator 15v via RLY4 to produce 15Vdc.

Under Main AC trip operation the power supply accepts a No AC (logic '0') signal 1502 from Detect Pwr Trip. This No AC signal 1502 is inverted by the inverter INV1-6 1504 to de-energize the relay (RLY 4) 1516. The relay (RLY 4) 1516 is de-energized, the contact return to the normally closed (NC) position, this allows the battery voltage (Bat) 1514 to flow to the bridge (B1) 1520.

At the same time no voltage flows to the regulator 15v via RLY4 therefore 0 volts is produced.

Note: The auto single means the different type power is auto switched and running the same path to power up the same load. There is another regulated power supply (15V_{dc}) 1526 for powering up the 15v device. The input comes from the Pt Vz 1522.

CHARGER1 – Analog

Alternative Charge 1 – Digital

Fig. 16 illustrates a circuit diagram of an analog charger in accordance with one embodiment of the invention. The battery 1632 is maintained at a voltage of 12.5V by op amp OP1-1 1612 and field effect transistor Q31 1616. The V₊ of the op amp 1612 is set to 12.5V by potential divider (resistor R31 1610 and R32 1608). When the battery 1632 is below 12.5V the OP1-1 1612 output is high and the OP1-1 1612 turn on the field effect transistor Q31 1616 to charge the battery. When the battery 1632 reaches 12.5V the OP1-1 1612 is turn off and the field effect transistor Q31 1616 is turn off, the charging process stops. The op amp OP1-2 1626, the LED1 1628 and the resistor R34 1620, R35 1622 indicate the status of the battery (charge or uncharged). The OP1-1 1612 output is feed into the V₋ of OP1-2 1626 and is compare to the voltage drop across R35 1622. The OP1-2 1626 V₊ smaller than V₋, the output of OP1-2 1626 is low LED1 1628 light on indicate charging is in progress.

The OP1-2 1626 V₊ greater than V₋, the output of OP1-2 1626 is high LED1 1628 light off indicate charging is there is no charging. The Battery voltage is passed to the

isolation switch (SW122 pin 2) 1624 denotes as BatSWP2. The BatSWP2 is feed into the switch (SW1 pin 3) (SWM manual) or the regulator 121 and RLY pin 3 (SWD digital). The isolation SW122 1624 is to isolate the supply from the battery when necessary.

5 **CHARGER1 – Digital**

Alternative Charge 1- Analog

Fig. 17 illustrates a circuit diagram of a digital charger in accordance with one embodiment of the invention.

Useful voltage	Q151 V_s	Q152 V_d	O/P NAND151-1	O/P XNOR	O/P AND 115-2
< 10.8	0	1	1	0	0
10.81 to 12.5	1	1	0	1	CLK
➤ 12.5	1	0	0	0	0

When the battery 1702 is undercharged, the undercharge voltage is less than 10.8v or 10% less (mean (90%) of the battery voltage). Fast charging is active. The under charge voltage is feed to the zener diode ZD151 1704 and ZD152 1746. The voltage drop across the ZD151 1704 is 7.8v leaving 2v drop across the resistor R151 1750. The V_{sg} is greater than the thresh hold voltage thus the Q151 1752 (P-channel) is conduct. Therefore the V_s of Q151 1752 is zero volts. The V_s of Q151 1752 is sent to the two inputs NAND gate 1710 (NAND 115-1) with one input tie to Bat5DC 1706 therefore logic ‘1’ is produced at NAND 115-1 1710 output. The voltage drop across the ZD152 1746 is 10.5v leaving 0.3v drop across the resistor R152 1748. The V_{gs} is smaller than the thresh hold voltage thus the Q152 1742 (N-channel) is cut off. Logic ‘1’ is produced at V_d of Q152 1742. The V_s of Q151 1752 and V_d of Q152 1742 are input to the XNOR gate 1738 (XNOR 151-1). The output of the XNOR 151-1 1738 logic ‘0’ is used to disable the clock CLK 1740 from passing to the AND gate AND 115-2 1736. Since one of the input of AND 115-2 1736 is at logic ‘0’, there for the output of the AND 115-2 1736 is logic ‘0’. The output of the NAND gate 1710 (NAND 115-1) and the AND gate 1736 (AND 115-2) are input to the

OR gate 1712 (OR 151-1). Logic '1' is produced at the output of OR 151-1 1712. The output is feed into the comparator OP151-1 1734 and is compare to the DC 0v. The V+ is greater than V- the output of the comparator OP151-1 1734 is high (15v). It is then turn on the Q31 1720. When the Q31 1720 is turn on it make a complete path to charge the battery as the isolation switch SW122 (DPDT) 1728 is normally closed (NC).

When the battery voltage is 10.81v to 12v or 90% to 100% of the battery voltage, slow charging is active. This voltage is feed to the zener diode ZD151 1704 and ZD152 1746. The voltage drop across the ZD151 1704 is 7.8v leaving 3.01v drop across the resistor R151 1750. The V_{sg} is smaller than the thresh hold voltage thus the Q151 1752 is cut off. Therefore the V_s of Q151 1752 is Bat5DC 1706 voltage (logic '1') pulls up by the resistor R153 1708. The V_s of Q151 1752 is sent to the two inputs NAND gate 1710 (NAND 115-1) with one input tie to Bat5DC 1706 therefore logic '0' is produced at the output of NAND115-1. The voltage drop across the ZD152 1746 is 10.5v leaving 0.31v drop across the resistor R152 1748. The V_{gs} is smaller than the thresh hold voltage thus the Q152 1742 is cut off. Logic '1' is produced at V_d of Q152 1742. The V_s of Q151 1752 and V_d of Q152 1742 are input to the XNOR gate 1738 (XNOR 151-1). The output of the XNOR gate 1738 (XNOR 151-1) is logic '1' is used to enable the AND gate 1736 (AND 115-2) so that the clock signal (CLK) can pass through the AND gate (AND115-2) and then OR gate (OR 115-1) to turn on the Q31 via the op amp (OP 151-1).

The output of the NAND gate 1710 (NAND 115-1) and the AND gate 1736 (AND 115-2) are input to the OR gate 1712 (OR 151-1). Waveform is produced at the output. The output is feed into the comparator OP151-1 1734 and is compare to the DC 0v. The waveform cause the V+ is greater than V- , then V+ smaller than V- , the output of the comparator OP151-1 1734 is high and then goes low(15v then 0v). It is then turn on and off the Q31 1720. When the Q31 1720 is turn on it make a complete path to charge the battery as the isolation switch SW122 (DPST) 1728 is normally closed (NC). When the Q31 1720 is turn off Q31 1720 is open and no charging is in progress. The isolation switch SW122 1728 (DPST) is still at normally closed (NC) making the complete path. The slow charging is in operation. The fasting charging stops because the output of NAND gate 1710 (NAND 115-1) is logic '0'.

When the battery is overcharged, the overcharge voltage is greater than 12.5v or 4.16% greater than the battery voltage. There will be no charging. The overcharge voltage is feed to the zener diode ZD151 1704 and ZD152 1746. The voltage drop across the ZD151 1704 is 7.8v leaving 4.7v drop across the resistor R151 1750. The V_{sg} is smaller than the thresh hold voltage thus the Q151 1752 is cut off. Therefore the V_s of Q151 1752 is Bat5DC 1706 voltage (logic '1') pulls up by the resistor R153 1708. The V_s of Q151 1752 is sent to the two inputs NAND gate 1710 (NAND 115-1) with one input tie to Bat5DC 1706 therefore logic '0' is produced. The voltage drop across the ZD152 1746 is 10.5v leaving 2v drop across the resistor R152 1748. The V_{gs} is greater than the thresh hold voltage thus the Q152 1742 is conduct. Logic '0' is produced at V_d of Q152 1742. The V_s of Q151 1752 and V_d of Q152 1742 are input to the XNOR gate 1738 (XNOR 151-1). The output of the XNOR gate 1738 logic '0' (XNOR 151-1) is used to disenable the AND gate 1736 (AND 115-2) so that the clock CLK 1740 cannot pass through the AND gate 1736 (AND 115-2). The output of the NAND gate 1710 (NAND 115-1) and the AND gate 1736 (AND 115-2) are input to the OR gate 1712 (OR 151-1). Logic '0' is produced at the output of OR 151-1 1712. The output is feed into the comparator OP151-1 1734 and is compare to the DC 0v. The V_+ is smaller than V_- the output of the comparator OP151-1 1734 is low (0v). It is then turn off the Q31 1720. When the Q31 1720 is turn off no complete path is established to charge the battery therefore the battery stop charging. Both the slow and fasting charging stops as the output of NAND gate 1710 (NAND 115-1) and the AND gate 1736 (AND 115-2) are at logic '0'. The isolation switch SW122 1728 (DPST) is normally closed (NC). The battery voltage is passed to the isolation switch 1728 (SW122 pin 2) denotes as BatSWP2. The BatSWP2 is feed into the switch (SW1 pin 3) (SWM manual) or the regulator 121 and RLY pin 3 (SWD digital). The isolation SW122 is to isolate the supply from the battery when necessary.

The resistor R36 1718, LED1 1716 and inverter INV151-1 1724 form an indicator for the charger. The output of OR151-1 1712 at logic '1', it is inverted by the inverter INV151-1 1724 to logic '0', the LED1 1716 light up permanently indicate battery is at fast charging, the LED1 1716 blink indicate the battery is at slow charging, the LED1 1716 off indicate no charging to the battery.

LED Driver

Fig. 18 illustrates a circuit diagram of a LED driver in accordance with one embodiment of the invention. The Pt V_z 1802 carry 18Vdc in AC mode and carry 12Vdc in DC mode is applied to both regulators 121-1 1810 and 121-2 1812 to produce an output voltage 8V to drive the LED. The zener diode ZD13 1808 clamps the input to 30Vdc to protect the two regulators against high voltage. A jumper can be used to connector the two output together to increase in current flowing to the load and thus reduce the heat generate by the regulator. The Battery voltage is supplied to the regulator 121-1 1810 and 121-2 1812. The output of the regulator is used to charge the capacitor C81-1 1822 & C81-2 1824 via R81-1 1820 & R81-2 1814. The V_C (C81-1 1820 & C81-2 1824) charges to the reverse break down of ZD81-1 1850 ZD81-2 1826, the voltage charge up further cause the FET Q121-1 1818 & Q121-2 1816 turns on slowly and the channel resistance of Q121-1 1818, Q121-2 1816 decreases slowly and the regulator voltage at Q121-1 1818, Q121-2 1816 (V_d) is transfer to Q121-1 1818, Q121-2 1816 source (V_s). When the FET Q121-1 1818 & Q121-2 1816 is fully turn on the voltage at Q121-1 1818, Q121-2 1816 (V_d) is equal to Q121-1 1818, Q121-2 1816 source (V_s). The voltage is feed to the connector CON1 to CON5 & CON21 to CON25 via R1 1830 to R5 1838 & ($\frac{1}{5}$ R21 1840) to (R25 1848). Each connector is link to 9 to 16 LEDs in parallel.

Assembly Board 1

Fig. 19 illustrates a board diagram of an electronic lamp in accordance with one embodiment of the invention. All the components are mounted on to board 1 1902 except the LED Driver components. Note: dimension is not drawn to scale.

LED DRIVER

Fig. 20 illustrates a board diagram of LED driver in accordance with one embodiment of the invention. All the electronic components in LED Driver, connector, the pogo pin, grounding plate, (GNDING PLATE) are soldered on to this board. The pogo pin

is solder at the center of the hole and the grounding plate is solder at either side of the hole.

Lighting Element (Electronic Lamp LED 9 / 16 max)

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Fig. 21 illustrates a board diagram of LED lamps in accordance with one embodiment of the invention. The lighting element consists of 9 LED per set. It can be extended to a maximum of 16 LED. Five set of lighting element is required. One set is mounted at the center and the other four set is mount at the side, tilted an angle from the horizon at the dispersal holder (Electronic Lamp Dispersal Holder) to produce light dispersion and help to increase the intensity. The voltage drop across each LED is 3.0 V to 4.5 V. (Electronic Lamp Dispersal Holder). The LED can increase to more than 16 with larger size of Electronic Lamp.

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Lighting Element Assembly (Electronic Lamp LED 9 / 16 max assembly)

Fig. 22 illustrates a board diagram of LED assembly in accordance with one embodiment of the invention. All the LEDs are assembled on to this board. Minor changes need to be made in order to place 10 to 16 LEDs on to this board to increase the light intensity. Change can be made on this board to place other type of LED. The size of the Lighting Element Assembly can be increase to assemble more LEDs (greater than 16).

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Lamp Adaptor (Electronic Lamp Adaptor)

Fig. 23 illustrates a board diagram of lamp adaptor in accordance with one embodiment of the invention. This is an n-shape adaptor. The center of the hole is threaded. At the top of the n-shape adaptor it is firmly secured by a hemisphere conductor material. . The external of this adaptor is also firmly secured by a conductor material, this conductor material is extended to the base of the n-shape adaptor, and it does not make any continuity to the hemisphere conductor material. It is thread at the surrounding area.

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LED Driver Assembly Holder (Electronic Lamp LED DRIVER Assembly Holder)

Fig. 24 illustrates a board diagram of LED driver assembly holder in accordance with one embodiment of the invention. The center of the LED Driver Assembly Holder has a through hole to insert the pogo pin and it is solder to the LED Driver Assembly. The outer surface is threaded. The Grounding Plate is place in the cavity and is solder to the LED Driver Assembly too. The Lamp Adaptor is screw to the LED Driver Assembly Holder. When it is fully tighten the hemisphere conductor material at the Lamp Adaptor make contact with the pogo pin and also the base of Lamp Adaptor makes contact with the Grounding Plate. The Power Source Assembly is attached to the PS Assembly Holder by screws or bolts and nuts. The most outer part has a screw thread to secure the Light Dispersal Holder. The size can be increase to hold the larger Light Dispersal Holder.

Light Dispersal Holder (Electronic Light Dispersal Holder)

Fig. 25 illustrates a board diagram of Light Dispersal Holder in accordance with one embodiment of the invention. The Light Dispersal Holder looks circular (all shape). Four side are tilted at an angle of 1° to 89° . This is to disperse the light for covering a larger area with smaller size and also help to increase the intensity. This include two side tilted at an angle of 1° to 89° for all shape. The top and the side are coated with reflecting material to reflect the light the down. In front of the LEDs is seal with high temperature transparent plastic for the light to pass through. Five sets the Lighting Element Assembly are attached to the Light Dispersal Holder. Clips are designed to hold this Lighting Element Assembly. At the top of Light Dispersal Holder has internal thread to hold it to the LED Driver Assembly Holder. The circular stud is to prevent it from over screwing. The warm air is released out through the eight ventilation holes at 45° apart.

Pogo Pin and Ground plate

Fig. 26 illustrates a board diagram of the pogo pin 2602 and ground plate 2604 in accordance with one embodiment of the invention.

Electronic lamp outline

Fig. 27 illustrates an outline of the electronic lamp in accordance with one embodiment of the invention.

5 **Electronic lamp isometric drawing**

Fig. 28 illustrates an isometric drawing of the electronic lamp in accordance with one embodiment of the invention.

CLAIMS

1. An electronic lighting apparatus comprising:

a power supply device;

5 a light emitting diode, and

a control circuit coupled to the power supply device and the light emitting diode.