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TITLE OF THE INVENTION

Apparatus Capable of Varying Number of Wait States for Access

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an information processing apparatus with an interchangeable external memory such as a ROM card.

Related Background Art

In the conventional information processing apparatus, the number of wait states of the CPU at the access to an interchangeable external memory is either fixed by an incorporated hardware, or controlled by a hardware provided in the external memory.

However, such conventional structure has been associated with following drawbacks:

(1) When the number of wait states for access to the external memory by the CPU is fixed by a hardware incorporated therein, the processing speed cannot be improved even with a memory of higher access speed, capable of functioning with a fewer number of wait states, as the number is fixed in the hardware.

(2) When the number of wait states for access to the external memory by the CPU is controlled by a hardware of the external memory, each external memory has to be provided with such hardware for controlling the

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number of wait states.

Also there is required a signal line for controlling the number of wait states in the interface with the external memory.

SUMMARY OF THE INVENTION

In consideration of the foregoing, an object of the present invention is to provide an apparatus capable of varying the number of wait states for access to the external memory by the CPU.

Another object of the present invention is to provide an apparatus capable of effecting a process responding to the access time of the memory.

The foregoing objects can be attained, according to an embodiment of the present invention, by an information processing apparatus comprising:

interchangeable external memory means storing data therein and holding information on the number of wait states for access;

process means for making access to said external memory means and processing the data stored therein;

reading means for reading, from the external memory means, the information on the number of wait states for access;

setting means for setting the number of wait states for access to the external memory means by the process means, based on the information on the number of

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wait states for access, read by the reading means; and

control means for controlling the access by the process means, according to the number of wait states set by the setting means.

In another embodiment of the present invention, the information processing apparatus comprises:

plural interchangeable external memory means for storing data, each holding information on the number of wait states for access;

process means for making access to the plural external memory means and processing the stored therein;

reading means for reading the information on the number of wait states for access, from each of the plural external memory means;

setting means for setting the number of wait states for access to the external memory means by the process means, based on the plural information on the number of wait states for access, read by the reading means; and

control means for controlling the access by the process means, according to the number of wait states set by the setting means.

In still another embodiment of the present invention, the information processing apparatus comprises:

interchangeable external memory means storing data therein and holding a number of wait states for access;

process means for making access to the external memory means and processing the data stored therein;

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reading means for reading, from the external memory means, the number of wait states for access;

setting means for setting the number of wait states for access to the external memory means by the process means at the value read by the reading means; and

control means for controlling the access by the process means, according to the number of wait states set by the setting means.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an information processing apparatus in accordance with an embodiment of the present invention; and

Fig. 2 is a flow chart of a process for setting the number of wait states.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now the present invention will be clarified in more detail by an embodiment thereof, of which block diagram is shown in Fig. 1.

In Fig. 1 there are shown a CPU 1 for controlling the entire apparatus; an address bus 2 for transferring an address signal indicating the object of control of the CPU 1; a data bus 3 for transferring data among different units of the apparatus; a ROM 4 storing various programs and data, including a program for setting the number of wait states to be explained later, the ROM

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being replaceable by an equivalent device capable of storing programs and data; a RAM 5 used as a work area for the CPU 1; an interface circuit 6 composed ordinarily of a buffer circuit for an external memory; and an external memory 7 which can be a non-volatile memory such as a ROM or an NVRAM and to which access is made by the CPU 1 through the external memory interface circuit 6.

A programmable wait state number control circuit 8 controls the number of wait states for access to the external memory 7 by the CPU 1, according to a number of wait state designated in the program of the CPU 1. A wait state number control signal 9 is supplied from the control circuit 8 to the CPU 1.

Fig. 2 is a flow chart of a process for setting the number of wait state for access to the external memory.

In the following there will be explained the sequence of setting the number of wait states for the access to the external memory 7, with reference to Fig. 2. At first, prior to the access to the external memory 7, a step S10 sets a largest settable number of wait states in the programmable wait state number control circuit 8. Then, in a step S11, the CPU 1 reads, through the external memory interface circuit 6, the information on the number of wait states provided in advance on the external memory 7 such as ROM or NVRAM. The information can be the number of wait states itself, or the access time of

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the external memory 7. A step S12 determines the number of wait states, based on the information on the number of wait states obtained in the step S11. The number is either obtained directly from the information if the information represents the number itself, or calculated by the CPU 1 if the information indicates the access time of the external memory 7. Then a step S13 sets the number of wait states, determined in the step S12, in the programmable control circuit.

Through the above-explained process, the number of wait states for the access to the external memory 7 by the CPU 1 through the interface circuit 6 is set in the programmable wait state number control circuit 8, so that the access to the external memory 7 by the CPU 1 is thereafter made with thus set number of wait states.

The foregoing embodiment allows the CPU 1 to make access to the external memory 7 with a number of wait states watching the access speed thereof, without a hardware for controlling the number in the part of the external memory.

In the foregoing embodiment, the external memory 7 is assumed to have only one number of wait states, but memories with different numbers of wait states may be mixedly present in the external memory 7. In such case, information on such different numbers of wait states are stored in advance in memories in the external memory 7, and the step S11 in Fig. 2 reads the information

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respectively from the memories in the external memory 7 and selects the largest number of wait states among the information, whereby the access to the external memory 7 is made with the number of wait state matching the lowest access speed of the plural memories present in the external memory 7.

As explained in the foregoing, the present invention is to obtain the information, on the number of wait states for access to an interchangeable external memory by the CPU, from the external memory and to control the number of wait states in the access of the CPU to the external memory according to the information, thereby enabling access to the external memory with a number of wait states matching the access speed thereof, without a hardware for controlling the number of wait states on the part of the external memory.

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CLAIMS:

1. An information processing apparatus comprising:

interchangeable external memory means for storing data, holding information on the number of wait states for access;

process means for making access to said external memory means and processing data stored therein;

reading means for reading, from said external memory means, said information on the number of wait states for access;

setting means for setting the number of wait states for access to said external memory means by said process means, based on the information on the number of wait states for access, read by said reading means; and

control means for controlling the access by said process means, according to the number of wait states set by said setting means.

2. An information processing apparatus according to Claim 1, wherein said external memory means is adapted to hold the access time thereof, as said information on the number of wait states for access.

3. An information processing apparatus comprising:

plural interchangeable external memory means for storing data, and holding respectively information on the number of wait states for access;

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process means for making access to said plural external memory means and processing the data stored therein;

reading means for reading, from each of said plural external memory means, the information on the number of wait states for access;

setting means for setting the number of wait states for access to said external memory means by said process means, based on plural information on the number of wait states, read by said reading means; and

control means for controlling the access by said process means, according to the number of wait states set by said setting means.

4. An information processing apparatus according to Claim 3, wherein said setting means is adapted to determine plural numbers of wait states for access, corresponding to plural information on said number, and select the largest one among said plural numbers.

5. An information processing apparatus comprising:

interchangeable external memory means for storing data, and holding a number of wait states for access;

process means for making access to said external memory means and processing the data stored therein;

reading means for reading, from said external memory means, said number of wait states for access;

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setting means for setting the number of wait states for the access to said external memory means by said process means, at the value read by said reading means; and

control means for controlling the access by said process means, according to said number of wait states set by said setting means.

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