DESCRIPTION

TITLE: METHOD FOR TREATING A SUBSTRATE HAVING A SURFACE MADE OF A SEMICONDUCTOR MATERIAL

FIELD OF THE INVENTION

The present invention relates to a process for treating a substrate having a surface made of a semiconductor material, notably a single-crystal semiconductor material. The treatment process comprises a surface stabilization step and a heat treatment step. The invention also relates to a process for manufacturing a semiconductor structure, comprising a step of stabilizing a surface of a semiconductor material, notably a single-crystal semiconductor material, and a step of heat-treating said surface.

PRIOR ART

Semiconductor materials, in particular silicon carbide (SiC), are widely used for manufacturing electronic power or radio frequency components. In certain applications, bulk single-crystal SiC substrates, substrates including a single-crystal SiC surface layer, or substrates including other semiconductor materials such as aluminium nitride (AlN), gallium nitride (GaN), alloys of these nitrides, indium phosphide (InP) or gallium arsenide (GaAs) are used. In certain cases, the semiconductor substrates or layers are polycrystalline.

Substrates for electronic applications often require heat treatments during their manufacture, for example annealing to cure defects in the crystal lattice caused during implantation of ionic species or to modify the crystal structure of the substrate. Such treatments are often performed at high temperatures that may be up to 2000°C.

However, the surface of the semiconductor materials under consideration is liable to become destabilized under the effect of high temperature. This destabilization may be reflected by a degradation of the surface, notably by a change in its morphology and/or composition.

In particular, as illustrated in Figure 1, smooth SiC surfaces are sensitive to treatments at high temperature, typically from about 1300°C upwards. In the absence of adequate protection of said surface, the morphology reorganizes to minimize the surface energy, forming terraces. This effect is known as “step bunching”. The reorganization of the surface 222 is due to diffusion of surface atoms when the surface is exposed to high temperatures. It also depends on the atmosphere and pressure to which the surface is exposed. It also depends on the angle of disorientation of the surface relative to the axis of high symmetry of the semiconductor material crystal. Such disorientation is used to facilitate control of the 4H polytype of SiC during subsequent epitaxy of single-crystal SiC and to avoid polytype changes during growth of the

single-crystal SiC. An angle of 4° is often chosen for such an epitaxy process. However, the greater the angle of inclination, the higher the steps between the terraces.

Such disorientations may also be seen spontaneously on a polycrystalline SiC surface, where the orientation of the grains is random.

The surfaces of other semiconductor materials may have the same kind of steps. On surfaces comprising GaN, gallium beads may be seen on the surface during exposure to high temperature.

In order to obtain smooth surfaces, it is thus sought to avoid the formation of terraces or to remove them in a subsequent step, and, where appropriate, to avoid the appearance of gallium beads or beads of another material.

For example, mechanical or chemical mechanical polishing (CMP) may be performed after the heat treatment. However, if the height of the terraces formed is too great, for example greater than 80 nm between two consecutive plates, the thickness to be removed is too great, which implies a long and laborious process. Furthermore, the remaining thickness is often too thin for the intended applications.

The article by J. Bao *et al*. proposes the use of very fast annealing ramps to limit the appearance of terraces. This method requires very rapid temperature rises of about 400°C per minute and thus is not compatible with industrial furnaces.

Alternatively, a silane overpressure may be applied to limit the sublimation of silicon in the SiC, thus preventing the formation of terraces. This method is described in the article by R. Zhang et al. However, it requires the introduction of an SiH_4 gas and the equipment to create the overpressure. Also, silicon droplets may be seen on the SiC surface at temperatures above 1600°C.

Another possibility for avoiding the formation of terraces is to use a protective layer, typically a carbon film about 1 μm thick. This technique involves adding additional steps to the formation process, such as depositing a resin, carbonizing said resin at a temperature of between 600°C and 1000°C, and using additional equipment, and entails a risk of contamination of the substrate and furnace with the resin. Furthermore, resin deposition and the removal of a micrometric layer of carbon are long and costly steps.

In certain cases, the protective layer may also be formed from aluminium nitride (AlN). However, this material is difficult to remove, in particular after heat treatment at a high temperature.

The presence of oxygen in the atmosphere of the furnace may limit the formation of terraces, but it runs the risk of forming pits on the surface that are incompatible with the resumption of epitaxy. Furthermore, high temperature furnaces typically comprise graphite elements which are sensitive to the presence of oxygen during annealing.

DESCRIPTION OF THE INVENTION

One aim of the invention is to provide a process for treating a substrate having a surface made of a semiconductor material, said process comprising a step of stabilizing said surface and a heat treatment step. The process is directed towards avoiding the formation of terraces and/or beads during the heat treatment via a step that is simple to perform. The stabilization step must be readily incorporated into the process for manufacturing a substrate including a surface made of a semiconductor material, and must not have any risk of contaminating such a substrate.

To this end, the invention proposes a process for treating a substrate having a free surface made of a semiconductor material, notably a single-crystal semiconductor material, comprising a process for stabilizing said surface against the formation of terraces and/or beads, said process involving

- the formation in the gaseous phase, on said surface, of a layer of vitreous carbon at a temperature above 700°C, preferably above 800°C, and strictly below 1000°C, preferably below 950°, and more preferably below 900°C, and
- a heat treatment of said substrate after stabilizing said surface, in which the vitreous carbon layer limits the reorganization of the surface into a semiconductor material in the form of terraces,

the deposition of the carbon layer and the heat treatment being performed in the same furnace.

The formation of the carbon layer at a temperature of between 700°C and 1000°C results in very low surface roughness of the semiconductor material relative to stabilization processes performed at higher temperatures. Furthermore, under such conditions, the density and size of the carbon particles forming on the surface of the semiconductor material during the growth of the carbon layer and the subsequent annealing process may be reduced.

Preferably, the formation of the vitreous carbon layer is performed under a gas pressure of between 0.1 and 100 kPa.

Advantageously, the formation of the carbon layer is performed in a gas stream comprising a carbon-based gas and a carrier gas, the carrier gas preferably being argon.

Advantageously, the carbon-based gas is propane.

Preferably, the formation of the vitreous carbon layer is performed at a partial pressure of the carbon-based gas of between 0.1 and 1 kPa.

The semiconductor material may be silicon carbide.

Advantageously, the carbon layer has a thickness of less than or equal to 100 nm.

In certain embodiments, the furnace comprises inner walls and support elements configured to hold at least one substrate, said inner walls, said supports and the gas inside the furnace having the same temperature.

Advantageously, the furnace has at least one carbon inner wall.

The furnace may contain a plurality of substrates comprising a surface of said semiconductor material, said substrates being vertically superposed, a vertical space being provided between two adjacent substrates, a carbon layer being formed on the surface of the semiconductor material of each of said substrates.

At least part of the heat treatment may be performed at a temperature above 1500°C.

Preferably, the process also comprises, after the heat treatment, a step of removing the carbon layer by chemical-mechanical polishing and/or by reactive ion etching and/or by plasma etching.

The invention also relates to a process for manufacturing a semiconductor structure, comprising the following steps:

- forming an embrittlement area by implanting ionic species in a donor substrate made of a semiconductor material, notably a single-crystal semiconductor material,
- bonding said donor substrate to a support substrate,
- detaching the donor substrate along the embrittlement area so as to transfer a layer of semiconductor material onto the support substrate,
- a treatment process as described above, so as to heal the defects created in the layer of semiconductor material during implantation of the ionic species, in which the carbon layer is formed on the free surface of the layer of semiconductor material transferred onto the support substrate.

DESCRIPTION OF THE FIGURES

Figure 1 illustrates the formation of terraces on one face of a single-crystal semiconductor material.

Figure 2 illustrates a substrate including a portion made of a single-crystal semiconductor material on its front face.

Figure 3 illustrates the substrate of Figure 2 after deposition of a carbon layer.

Figure 4 illustrates the substrate of Figure 3 after ablation of the carbon layer.

Figures 5A to 5C illustrate the manufacture of a substrate including a portion made of a single-crystal semiconductor material on its front face.

Figure 6A shows an example of a thermal profile used for a first embodiment of a process according to the invention.

Figure 6B shows an example of a thermal profile used for a second embodiment of a process according to the invention.

Figure 7A is an atomic force microscopy (AFM) image illustrating the roughness induced by the terraces on the surface of a substrate that has undergone heat treatment at 1500°C without the application of a carbon layer.

Figure 7B is an atomic force microscopy image illustrating the roughness of the surface of a substrate that has undergone heat treatment at 1500°C with a layer of vitreous carbon according to the invention.

Figure 8A is an AFM image showing the roughness of the surface of a carbon layer obtained by deposition at 900°C for 10 minutes after annealing at 1700°C.

Figure 8B is an AFM image showing the surface roughness of a carbon layer obtained by deposition at 1000°C for 10 minutes after annealing at 1700°C.

Figure 9 shows an annealing furnace suitable for forming a carbon layer according to a preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 2 illustrates a substrate 10 including a support substrate 11 and a portion 20 made of a single-crystal or polycrystalline semiconductor material on its front face. The support substrate 11 may be any type of support substrate suitable for depositing or transferring a portion 20 made of a single-crystal or polycrystalline semiconductor material, for example a support substrate made of a polycrystalline semiconductor material.

Alternatively, the substrate 10 may be a bulk substrate made of a single-crystal or polycrystalline semiconductor material, i.e. the support substrate 11 and the portion 20 together constitute a single portion made of a bulk single-crystal or polycrystalline semiconductor material.

Preferably, the portion 20 on the front face of the substrate is made of a single-crystal semiconductor material. However, the semiconductor material which forms the front face of the substrate 10, and which thus makes up either the portion 20 (in the case of a substrate 10 including a support substrate 11 and a portion 20) or the substrate 10 (in the case of a bulk substrate) is also likely to be a polycrystalline material.

In the remainder of the description, since the case of a substrate 10 including a support substrate 11 and a single-crystal portion 20 is detailed, the material which makes up the portion 20 will be denoted by the expression “single-crystal semiconductor material” to distinguish it from the material making up the support substrate 11. However, the process described below is also applicable to the case of a polycrystalline semiconductor material, each grain thus being able to be considered as a single crystal.

According to a preferred embodiment, the single-crystal semiconductor material is silicon carbide.

According to other embodiments, the single-crystal semiconductor material is chosen from: aluminium nitride (AlN), gallium nitride (GaN), alloys of these nitrides $Al_xGa_{(1-x)}N$, x being a number between 0 and 1, indium phosphide (InP) or gallium arsenide (GaAs).

Typically, the surface 200 of the portion 20 made of a single-crystal semiconductor material or, where appropriate, of the substrate made of a bulk single-crystal semiconductor material, is slightly offset. For example, if the semiconductor material is SiC, the surface may be offset relative to the SiC crystal structure to facilitate control of 4H polytype during growth.

In the case of a polycrystalline semiconductor material, some of the grains may have such an offset relative to the SiC crystal structure. For example, following cutting or polishing of the substrate 10 in such a way as to reveal a specific face of the substrate 10, grains whose orientation is randomly oriented relative to this face will have an offset.

Formation of the protective layer

Subsequently, with reference to Figure 3, a layer of vitreous carbon 30 is formed on the surface 200 of the portion 20 of a single-crystal semiconductor material. The vitreous carbon layer is continuous and covers the entire surface to be protected, i.e. the front face of the single-crystal material. Typically, the vitreous carbon layer 30 is deposited on all the free surfaces of the substrate and thus simultaneously covers the front face and the rear face of the substrate. This allows the rear face to be protected simultaneously against the formation of terraces and, in the case of a silicon carbide substrate, against evaporation of the silicon during the heat treatment.

Said carbon layer protects the surface of the substrate against the formation of terraces when heated to a high temperature. It thus stabilizes the crystalline structure of the surface. The carbon layer is removed after the high-temperature treatments have been completed to obtain a clean single-crystal semiconductor material surface with good crystalline quality. The thickness of the carbon layer is preferably less than 100 nm to allow it to be readily removed at the end of a high temperature process.

The vitreous character of the carbon layer is obtained from a carbon thickness of a few nanometres; for a thinner layer, the carbon is in the form of one or two graphene monolayers. When the thickness is sufficient to obtain vitreous carbon, the protective layer has a long-distance, unorganized three-dimensional structure, which is stable throughout the range of temperatures to which the surface is exposed during the process, and which allows total coverage of the substrate surface. The uniformity of a vitreous carbon layer is more readily controllable over the extent of the substrate surface.

Advantageously, the formation of the vitreous carbon layer is performed in a furnace which will be described later. The carbon layer is formed in the gaseous phase, i.e. the carbon is present in the furnace in a gaseous form. The substrate is heated in the furnace to a

temperature at which the protective layer is deposited, and the gaseous phase of carbon is transformed into solid carbon by reaction with the hot surface of the substrate.

The temperature and gas pressure in the furnace are chosen to avoid degradation of the surface to be protected during deposition of the carbon layer. During the formation of the carbon layer, the temperature in the furnace is above 700°C and strictly below 1000°C, advantageously below 950°C. Preferably, the temperature during formation of the carbon layer is between 800°C and 900°C so as to protect the substrate surface in an effective manner.

Temperatures below 800°C slow down the process. At temperatures below 700°C, the slowdown is such that it adversely affects the efficiency of the process.

During the formation of the carbon layer and the subsequent heat treatment, carbon particles often appear on the surface of the substrate. The density and size of said carbon particles is considerably reduced at a carbon layer formation temperature strictly below 1000°C and more advantageously below 900°C. Higher temperatures, notably above 1000°C, lead to the appearance of large particles, which may be up to about 60 nm in size. These particles form on the surface of the substrate during the formation of the carbon layer and the subsequent heat treatment. A carbon layer formation temperature of 1000°C and above thus increases the roughness of the substrate surface.

A polishing step, for example chemical mechanical polishing to remove the carbon layer, is easier to perform and involves less risk of scratching the surface when the number and size of such particles are reduced.

Furthermore, reducing the density and size of carbon particles on the surface reduces the risk of contamination of other substrates or components with such particles, for example in an electronic component production environment.

The reduction in surface roughness also allows the thickness of the deposited carbon layer to be more readily controlled.

The temperature range between 700 and 950°C, preferably between 800 and 900°C, thus allows the thickness of the deposited carbon layer to be readily controlled via an efficient process, avoiding the appearance of carbon particles with a size and density that are too large for the manufacture of power and radio frequency electronic components.

Advantageously, the carbon source is a carbon-based gas, for example propane (C_3H_8). Alternatively, the carrier gas may be methane (CH_4) or ethane (C_2H_6). Using propane as the carrier gas allows the carbon layer to be formed more quickly due to the C-C bond of the carbon atoms, which is easier to break than the C-H bonds in methane and ethane.

The carbon-based gas is mixed with a carrier gas, for example argon or a mixture of argon and hydrogen. The carrier gas is a neutral gas which is not involved in the chemical reaction of layer formation. Typically, the mixture of gases is produced in the furnace chamber

at the deposition temperature. The gas flow rate may be readily controlled and adjusted to the carbon layer deposition conditions.

Typically, the carbon layer is deposited under a gas pressure of between 0.1 and 100 kPa (between 1 mbar and 1 bar), which is readily maintained in an industrial furnace. The partial pressure of the carbon-based gas is typically adjusted to a value of between 0.1 and 1 kPa (between 1 mbar and 10 mbar). Such a concentration allows saturation of the furnace atmosphere to be avoided, which allows better control of the thickness of the deposited carbon layer.

Advantageously, the thickness of the protective carbon layer is less than 100 nm, for example between 50 nm and 100 nm. The time required to produce such a layer depends on the temperature and the partial pressure of the carbon-based gas and is typically between two seconds and two hours. The temperature during the formation of the layer, the pressure and type of carbon-based gas and the duration of the step allow the thickness of the deposited carbon layer to be adjusted.

The carbon layer may be characterized by surface analysis techniques, for example by atomic force microscopy (AFM), X-ray reflectivity (XRR), Raman spectroscopy or low energy electron microscopy (LEEM).

The carbon layer is stable at least up to a temperature of 2000°C and thus allows the formation of terraces to be limited while the substrate is exposed to a temperature above the terrace formation temperature.

<u>High-temperature steps requiring the protective layer</u>

Following the formation of the carbon layer, further steps may be performed on the substrate at a temperature above the terrace formation temperature. Such steps are, for example, annealing so as to heal defects in the crystal lattice caused during the implantation of ionic species, to modify the crystal structure of the substrate, or for the activation of dopants. During these steps, the surface of the single-crystal semiconductor material is protected with the carbon layer and the formation of terraces on said surface is avoided. The annealing steps are performed at temperatures of between 1300°C and 1900°C, typically above 1500°C.

The formation of the carbon layer and the heat treatment are performed in the same furnace, which is advantageously a furnace traditionally used for batch annealing of substrates.

A furnace rising to temperatures above 1500°C generally comprises graphite elements because of the good stability of this material at high temperatures. In any case, the formation of the carbon layer in such a furnace only causes the deposition of a very thin layer of carbon which does not affect the functioning of these elements consisting of the same material as the layer.

Removal of the protective layer

At the end of the annealing steps, the temperature is lowered to a temperature below the terrace formation temperature, i.e. below 1300°C.

In certain embodiments, the removal may be performed in the same furnace as that in which the steps for forming the protective carbon layer and/or the high-temperature steps were performed. In this case, the temperature is lowered to a temperature for ablation of the carbon layer, for example about 900°C. The carbon layer may then be removed because the temperature is low enough for no terrace formation to take place on the surface of the semiconductor material. The thinness of the carbon layer promotes removal from the substrate quickly and without residue.

Removal of the carbon layer may be performed by a reactive plasma, for example an oxygen plasma, according to the reaction:

$$C(\text{solid}) + O_2(\text{gaseous}) \rightarrow CO_2(\text{gaseous})$$

In other embodiments, the substrate is cooled after the heat treatment step and transferred to another chamber or device for removal of the carbon layer. Such a transfer is necessary, for example, if parts of the furnace are made of unprotected graphite or other materials which may be damaged by contact with the reactive plasma, and if the removal of the carbon layer is performed by plasma.

Alternatively, the carbon layer may be removed by reactive ion etching (RIE), for example with oxygen ions or a mixture of oxygen and sulfur hexafluoride after transfer to a suitable chamber.

In order to remove any carbon residues and/or to ensure a good surface quality of the single-crystal semiconductor material, a suitable chemical-mechanical polishing step may be performed after removing the carbon layer.

In certain cases, the carbon layer is removed during a finishing step of the substrate after leaving the furnace, for example during a chemical-mechanical polishing or mechanical polishing step.

On conclusion of the removal step, with reference to Figure 4, the substrate 11 is finished and the carbon layer is removed. The substrate 11 and the free surface of the single-crystal semiconductor material may now be used for the epitaxial growth of a layer of a single-crystal semiconductor material (identical to or different from that of the substrate 11) and/or the manufacture of a power or radio-frequency electronic component.

In certain cases, the carbon layer on the rear face of the substrate is removed together with the layer on the front face. In other embodiments, the vitreous carbon layer arranged on the rear face of the substrate is retained in this step and during the manufacture of an electronic device on the front face to protect the rear face during these steps. In this case, the carbon

layer on the rear face is removed before or during a substrate thinning step, for example by grinding.

Process for manufacturing a semiconductor structure

A process for manufacturing a semiconductor structure for electronic applications, having a single-crystal silicon carbide surface, will now be described.

A donor substrate 220 preferably made of single-crystal silicon carbide is provided, from which the single-crystal silicon carbide surface layer is formed. With reference to Figure 5A, as shown by the arrows, an implantation of ionic species, such as hydrogen and/or helium, is performed so as to form an embrittlement area 21 in the donor substrate 220. Said embrittlement area 21 defines a layer 20 of single-crystal silicon carbide to be transferred.

With reference to Figure 5B, the donor substrate 220 thus implanted is bonded to a base substrate 11. The donor substrate may be bonded directly to the base substrate as shown in Figure 5B, or via one or more intermediate layers which may be applied to the donor substrate and/or the base substrate prior to bonding (not shown).

With reference to Figure 5C, the donor substrate 220 is then detached along the embrittlement area 21, which results in transfer of the single-crystal silicon carbide layer onto the base substrate 11, thus forming the support substrate 10 as represented in Figure 2. The detached portion 221 of the donor substrate may be reused for transferring other single-crystal silicon carbide layers onto other base substrates.

A process for treating the substrate 10 is then performed, successively comprising a step of stabilizing the surface by forming a protective vitreous carbon layer, high-temperature annealing intended to heal the defects created in the single-crystal silicon carbide layer during implantation of the ionic species, and subsequent removal of the protective carbon layer.

The process comprising the formation of the carbon layer and the heat treatment is performed in the same furnace. Thus, transferring the substrate from a deposition chamber dedicated to depositing the protective layer to an annealing furnace is avoided, and thus a simpler, faster process is obtained, minimizing the risk of substrate contamination.

Figure 6A shows a temperature profile for one embodiment of such a process as a function of time. Three main sequences of the process may be distinguished, corresponding to the formation of a protective carbon layer (S1), annealing at high temperature (S2), i.e. above the temperature at which terrace formation begins, and a step of removing the protective layer (S3).

The gas injected at the top of the furnace is discharged in a stream of carrier gas via the bottom of the furnace throughout all the process sequences.

The first sequence S1 starts at time t0. The substrate is at room temperature, which is typically about 20°C, or at a temperature below the terrace formation temperature. The substrate is introduced into the deposition chamber. The substrate is heated to a deposition

temperature T1 for the vitreous carbon layer. The deposition temperature T1 is greater than 700°C and strictly less than 1000°C. T1 is thus lower than the temperature at which terraces begin to form, which is about 1300°C at a pressure of 101 kPa (1 atm), or even about 1200 or 1100°C at lower pressures. The temperature T1 is also lower than the temperature of about 1000°C which can cause an increase in surface roughness.

From a time t1, a gas stream comprising a carbon-based gas and a carrier gas is injected into the furnace.

Deposition of the carbon layer begins at time t1. The duration of formation of the carbon layer is typically between two seconds and two hours up to time t2. During this time, the deposition temperature T1 is kept constant. The pressure in the furnace is maintained between 0.1 and 100 kPa (between 1 mbar and 1 bar).

The flow rate of the injected gases depends on the volume of the chamber and is controlled to obtain a partial pressure of the carbon-based gas of between 0.1 and 1 kPa (between 1 mbar and 10 mbar). The deposition temperature T1 and the carbon-based gas flow rate may be adjusted to obtain a carbon layer with a desired thickness and homogeneity suitable for optimum protection during the next sequence, and in a sufficiently short time to optimize the process in terms of time and cost.

The carbon-based gas feed is stopped at the end of sequence S1. The carbon-based gas residues are evacuated under the carrier gas stream.

When deposition of the carbon layer is complete at a time t2, the second sequence S2 is performed. The second sequence S2 involves heating from the deposition temperature T1 to an annealing temperature T2 and a temperature plateau lasting, for example, between 30 and 120 minutes. The annealing temperature T2 and the duration of the treatment are chosen as a function of the state of the substrate prior to the current process, and of the crystalline structure of the substrate envisaged. Typically, annealing is performed at a temperature T2 above 1500°C, for example between 1600°C and 1900°C.

The heat treatment in the second sequence is performed in the same furnace as the formation of the carbon layer in the first sequence.

At the end of sequence S2, the substrate is cooled to conserve the crystalline properties obtained during annealing. At a time t3, the substrate reaches a third temperature T3 of 900°C.

In certain embodiments, with reference to Figure 6A, a third sequence S3 is performed directly, during which the protective carbon layer is removed by oxidation, as described previously. During this step, oxygen may be injected into the furnace to create a reactive plasma.

During this step, the temperature T3 = 900°C is kept constant. The removal time is typically between 10 and 120 s at a stripping rate of about 100 nm per minute. The total duration of sequence S3 also includes stabilization of the furnace and is typically between five

minutes and one hour. When, at time t4, the carbon layer is totally removed, the furnace is cooled in order to take out the substrate.

Figure 6B illustrates a temperature profile for one embodiment in which the step of removing the carbon layer is performed outside the furnace. Sequences S1 and S2 are performed as described above. At the end of sequence S2, the substrate is cooled to a temperature close to room temperature, allowing the furnace to be opened and the substrate to be removed. Removal of the carbon layer is performed during sequence S3' outside the furnace. In this case, a step of transferring from the annealing furnace to a chamber for removing the protective layer or to a polishing device is performed at time t3. When the substrate treatment process comprises a transfer step, the various sequences may be performed separately over time. Depending on the technique used to ablate the vitreous carbon layer, sequence S3 may involve heating to a temperature below the terrace formation temperature or may be performed at room temperature.

Effect of the protective layer on the formation of terraces

Figures 7A and 7B are atomic force microscopy (AFM) images over a 30x30 μm^2 area of two respective substrates each having a single-crystal silicon carbide surface.

Figure 7A is an AFM image of a substrate that has been heat-treated at 1500°C without the application of a carbon layer. Terraces have formed on the surface of the substrate, visible in the form of vertical lines in the AFM image. The root mean square (RMS) value of the surface roughness induced by the terraces is about 16 nm.

Figure 7B is an AFM image showing the surface roughness of a substrate of the same type, which has also been heat-treated at 1500°C. The substrate in Figure 7B was protected with a layer of vitreous carbon formed at a temperature of 900°C and a pressure of less than 5 kPa (50 mbar) for 10 minutes prior to the heat treatment. The carbon layer was formed in an atmosphere comprising argon as the carrier gas and propane as the carbon-based gas. The propane content in the mixture was less than 30%.

The image of the protected substrate shows no parallel line structure indicating the presence of terraces. The root mean square value of the surface roughness is about 0.2 nm. The roughness of the substrate protected with the carbon layer is therefore considerably less than the roughness of the substrate without the protective layer.

Effect of temperature during formation of the carbon layer

Figures 8A and 8B are AFM images over a 5x5 μm^2 area of two respective substrates having a single-crystal silicon carbide surface. Each substrate includes a protective carbon layer. The carbon layers were deposited at different temperatures. Each respective substrate underwent heat treatment at 1500°C under identical conditions.

The substrate in Figure 8A is protected with a carbon layer deposited for 10 minutes at a temperature of 900°C, in accordance with a preferred embodiment of the invention. The

curve below the AFM image shows the height profile of the magnified portion of the image over a length l of 100 nm. In this area, the largest particles on the surface have a height h of about 1.5 nm.

The substrate in Figure 8B is protected with a layer of carbon deposited for 10 minutes at a temperature of 1000°C, i.e. under conditions not covered by the invention. This image has a more granular structure than the image in Figure 8A, indicating greater surface roughness. A height profile over a length l of 500 nm of this surface is represented below the AFM image. This profile shows larger grains, up to a height h of about 15 nm.

The carbon layer formed at 900°C thus has considerably lower roughness than the layer formed at 1000°C. Due to the fact that the roughness increases with the temperature at which the carbon layer is formed, it is necessary to form the carbon layer at a temperature strictly below 1000°C.

Presentation of the furnace

In order to make a process for treating a plurality of substrates fast and efficient, an annealing furnace which can treat a maximum number of substrates simultaneously under identical conditions is preferably used. Such a furnace is conventionally referred to as a batch annealing furnace in the microelectronics field.

Figure 9 illustrates a furnace suitable for receiving an amount of between 120 and 150 substrates in an annealing chamber. The substrates 10 are positioned horizontally in the furnace and are superposed vertically so as to treat as many substrates as possible in the same stream 73 of hot gas. A free space is maintained between each substrate 10 and the adjacent substrates 10 to optimize the gas stream and facilitate the formation of the carbon layer. Typically, the vertical distance between two adjacent substrates is between 2 and 20 mm.

Such a furnace uses a “top flow” configuration, i.e. a stream of gas is fed into the furnace from the top 71 and, after passing through the furnace, is discharged through an outlet 79 at the bottom of the furnace. Typically, a carrier gas stream transports the carbon-based gas (typically propane) for formation of the carbon layer. In certain cases, other gases are added to the furnace, for example catalyst-type gases to promote the decomposition of the carbon-based gas.

All the elements of the annealing chamber inside the furnace, i.e. the inner walls 75, the substrate holders for holding the substrates in a horizontal and vertically superposed position, and the gas included in the annealing chamber are at the same temperature during use of the furnace, with the exception of the outer elements such as the outer wall 76 and the ends of the gas inlet pipes. The term “same temperature” means that the difference in temperature between the top end 74 of the furnace and the bottom end 78 of the furnace is

minimal, typically a few degrees Celsius, for example less than 3 degrees for a temperature in the furnace of between 800 and 1200°C.

The substrates are heated mainly by conduction from the walls of the furnace. The gas streams are injected at the same temperature as the temperature inside the furnace.

An annealing furnace is not intended for the deposition of layers but for the application of a heat treatment to the substrates placed in the furnace. These furnaces are thus optimized for high temperature homogeneity of the substrates received therein, but not to allow optimization of a material deposition, notably to ensure homogeneity of the gas stream on the surface of the substrates. The superposed positioning of the substrates notably hinders this homogeneity, since it is more difficult for the gases to reach the centre of the substrates than the edges. However, this type of furnace is nevertheless suitable for depositing carbon layers to protect the surface of a semiconductor material against the formation of terraces, notably because the homogeneity of the thickness of the carbon layer is not a decisive criterion as long as all of the surface to be protected is covered. Temporary use of the carbon layer does not require increased homogeneity of this layer. However, it is necessary to control the thickness so as to obtain a sufficient thickness over the entire surface of all the substrates contained in the furnace. The use of graphite elements inside the furnace is compatible with the deposition of the carbon layer due to the fact that it is the same material and that the thickness of the deposited layer is small relative to the dimensions of said elements.

Unlike an epitaxy chamber, such a furnace allows a large number of substrates to be treated simultaneously by virtue of the vertical overlapping arrangement. Furthermore, such a furnace allows the carbon layer deposition and annealing steps to be performed in the same chamber, thus avoiding the risk of contamination during transfer between two different chambers. Steps for transferring between a chamber for deposition of the carbon layer and an annealing furnace are avoided, thus avoiding cooling between the respective steps, the need for manpower for the transfer and thus a loss of time and efficiency.

REFERENCES

R. Zhang et al. “Growth of large Domains of Epitaxial Graphene on the C-face of SiC”, J. of App. Phys. 2012, 112 (10); doi: 10.1063/1.4765666

J. Bao et al. “Sequential Control of Step-Bunching During Graphene Growth on SiC (0001)”, App. Phys. Lett. 2016, 109(8); doi: 10.1063/1.4961630

CLAIMS

1. Process for treating a substrate having a free surface made of a semiconductor material, notably a single-crystal semiconductor material, comprising a process for stabilizing said surface against the formation of terraces and/or beads, said process involving

- the formation of a layer of vitreous carbon (30) by a carbon reaction in the gaseous phase on said surface at a temperature (T1) above 700°C, preferably above 800°C, and strictly below 1000°C, preferably below 950°, and more preferably below 900°C, and
- a heat treatment of said substrate after stabilizing said surface, in which the vitreous carbon layer (30) limits the reorganization of the surface into a semiconductor material in the form of terraces,

the deposition of the carbon layer (30) and the heat treatment being performed in the same furnace.

2. Treatment process according to the preceding claim, in which the formation of the vitreous carbon layer (30) is performed under a gas pressure of between 0.1 and 100 kPa (between 1 mbar and 1 bar).

3. Treatment process according to either of the preceding claims, in which the formation of the carbon layer is performed in a gas stream comprising a carbon-based gas and a carrier gas, the carrier gas preferably being argon.

4. Treatment process according to Claim 3, in which the carbon-based gas is propane.

5. Treatment process according to either of claims 3 and 4, in combination with Claim 2, in which the formation of the vitreous carbon layer (30) is performed at a partial pressure of the carbon-based gas of between 0.1 and 1 kPa (between 1 mbar and 10 mbar).

6. Treatment process according to any one of the preceding claims, in which the semiconductor material is silicon carbide.

7. Treatment process according to any one of the preceding claims, in which the carbon layer (30) has a thickness of less than or equal to 100 nm.

8. Treatment process according to any one of the preceding claims, in which the furnace (70) comprises inner walls (75) and support elements configured to hold at least one substrate (10), said inner walls (75), said supports and the gas inside the furnace (70) having the same temperature.

9. Treatment process according to any one of the preceding claims, in which the furnace (70) has at least one inner wall (75) made of carbon.

10. Treatment process according to any one of the preceding claims, in which the furnace (70) contains a plurality of substrates comprising a surface of said semiconductor material, said substrates being vertically superposed, a vertical space being provided between two adjacent substrates, a carbon layer (30) being formed on the surface of the semiconductor material of each of said substrates.

11. Treatment process according to any one of the preceding claims, in which at least part of the heat treatment is performed at a temperature above 1500°C.

12. Treatment process according to any one of the preceding claims, also comprising, after the heat treatment, a step of removing the carbon layer (30) by chemical-mechanical polishing (CMP) and/or by reactive ion etching and/or by plasma etching.

13. Process for manufacturing a semiconductor structure, comprising the following steps:

- forming an embrittlement area (21) by implanting ionic species in a donor substrate (220) made of a semiconductor material, notably a single-crystal semiconductor material,
- bonding said donor substrate (220) to a support substrate (11),
- detaching the donor substrate (220) along the embrittlement area (21) so as to transfer a layer (20) of semiconductor material onto the support substrate (11),
- a treatment process according to one of Claims 1 to 12, so as to heal the defects created in the layer of semiconductor material (20) during implantation of the ionic species, in which the carbon layer (30) is formed on

the free surface (200) of the layer (20) of semiconductor material transferred onto the support substrate.