WHAT IS CLAIMED IS:

1. A field effect transistor, comprising:

a gate contact and gate metal forming a vertical structure, such vertical structure having sides and a top surrounded by an air gap formed between a source electrode and a drain electrode of the field effect transistor;

a vertical stack comprising:

a portion of a III-N buffer layer, a portion of a III-N channel layer, and a portion of a III-V buffer layer; and

a uniformly thick, horizontally extending doped GaN layer disposed on the III-N buffer layer, the uniformly thick, horizontally extending doped GaN layer having an aperture extending vertically there through, the aperture having vertically extending sidewalls terminating at horizontally extending upper surface portions of the III-N buffer layer,

wherein the vertical stack extends vertically upwardly into the aperture and between the vertically extending sidewalls of the aperture, and

wherein the vertical structure is disposed on the vertical stack.

2. The field effect transistor recited in claim 1 wherein the source electrode and the drain electrode are damascene structures.

3. The field effect transistor recited in claim 2 wherein the vertical structure having sides and the top surrounded by the air gap extending vertically to a level parallel to a top of the damascene structures.

4. The field effect transistor recited in claim 3 wherein the gate contact is comprised of a plurality of stacked damascene metal layers.

5. The field effect transistor recited in claim 4 wherein the gate contact is comprised of the plurality of stacked damascene metal layers extending vertically to a level parallel to tops of the damascene structures.

6. The field effect transistor recited in claim 5 wherein the field effect transistor is a mesa structure, wherein the vertical structure having the sides and the top surrounded by

the air gap formed between the source and drain electrodes and between edges of the mesa structure are perpendicular to the direction of the gate.

7. A field effect transistor structure, comprising:

an III-N buffer layer;

an III-N channel layer of disposed over III-N buffer layer;

a III-V barrier layer disposed on the III-N channel layer;

wherein a 2DEG is formed in the channel layer;

a uniformly thick, horizontally extending doped GaN layer disposed on the III-N buffer layer, such uniformly thick, horizontally extending doped GaN layer having an aperture extending vertically there through, such aperture having vertically extending sidewalls terminating at horizontally extending upper surface portions of the III-N buffer layer;

a gate electrode;

a vertical stack comprising:

a portion of the III-N buffer layer, a portion of the III-N channel layer, and a portion of the III-V buffer layer,

wherein the vertical stack extends vertically upwardly into the aperture and between the vertically extending sidewalls of the aperture; and

a gate metal disposed on the vertical stack; and

source and drain contacts in Ohmic contact with an upper surface portion of the uniformly thick, horizontally extending doped GaN layer;

wherein the gate electrode is disposed between the source and drain contacts.

8. The field effect transistor structure recited in claim 7 including:

a gate contact disposed on the gate metal, and wherein the source and drain contacts have a lower portion; and wherein the gate contact and the lower portion of the source and drain contacts have upper surfaces disposed in a common plane.

9. The field effect transistor structure recited in claim 8 wherein the source and drain contacts are damascene structures.

10. The field effect transistor structure recited in claim 9 wherein the gate contact and gate metal form a vertical structure, such vertical structure having sides and a top surrounded by an air gap extending vertically to a level parallel to tops of the damascene structures.

11. The field effect transistor structure recited in claim 8 wherein the gate contact and gate metal form a vertical structure, such vertical structure having sides and a top surrounded by an air gap.

12. The field effect transistor structure recited in claim 10 wherein the gate contact is comprised of a plurality of stacked damascene metal layers.

13. The field effect transistor structure recited in claim 12 wherein the gate contact is comprised of a plurality of stacked damascene metal layers extending vertically to a level parallel to a top of the damascene structures.