SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority under 35 U.S.C. § 119(a) to Korean patent application number 10-2021-0020127 filed on February 15, 2021, in the Korean Intellectual Property Office, the entire disclosure of which is incorporated by reference herein.

BACKGROUND

1. Technical Field

[0002] The present disclosure generally relates to an electronic device, and more particularly, to a semiconductor device and a manufacturing method of a semiconductor device.

2. Related Art

[0003] A degree of integration of a semiconductor device is mainly determined by an area occupied by a unit memory cell. As the improvement of the degree of integration of semiconductor devices in which memory cells are formed in the form of a single layer over a substrate reaches the limit, there has recently been proposed a three-dimensional semiconductor device in which memory cells are stacked over a substrate. Various structures and manufacturing methods have been developed so as to improve the operational reliability of the three-

dimensional semiconductor device.

SUMMARY

[0004] Embodiments relate to a semiconductor device having a stable structure and improved characteristics, and a manufacturing method of the semiconductor device.

[0005] In accordance with an aspect of the present disclosure, there is provided a semiconductor device including: a first electrode including a carbon layer; a second electrode; a variable resistance layer interposed between the first electrode and the second electrode; and a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including nitrogen and carbon, wherein a concentration of the nitrogen in the barrier layer is equal to or higher than that of the carbon in the barrier layer.

[0006] In accordance with another aspect of the present disclosure, there is provided a method of manufacturing a semiconductor device, the method including: forming a first electrode including a carbon layer; forming, on the first electrode, a barrier layer including carbon nitride in which a concentration of nitrogen is equal to or higher than that of carbon; forming a variable resistance layer on the barrier layer; and forming a second electrode on the variable resistance layer.

[0007] In accordance with an aspect of the present disclosure, there is provided a semiconductor device including: a first electrode including a first element; a second electrode; a variable resistance layer interposed

between the first electrode and the second electrode; and a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including the first element and a second element, wherein a concentration of the second element in the barrier layer is equal to or higher than that of the first element in the barrier layer, and the barrier layer is in an amorphous state.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the example embodiments to those skilled in the art.

[0009] In the drawing figures, dimensions may be exaggerated for clarity of illustration. It will be understood that when an element is referred to as being "between" two elements, it can be the only element between the two elements, or one or more intervening elements may also be present. Like reference numerals refer to like elements throughout.

[0010] FIG. 1 is a view illustrating a structure of a semiconductor device in accordance with an embodiment of the present disclosure.

[0011] FIG. 2 is a view illustrating a structure of a semiconductor device in accordance with an embodiment of the present disclosure.

[0012] FIGS. 3A and 3B are views each illustrating a structure of a semiconductor device in accordance with an embodiment of the present disclosure.

[0013] FIG. 4 is a view illustrating a structure of a semiconductor device in accordance with an embodiment of the present disclosure.

[0014] FIGS. 5A and 5B are views illustrating a manufacturing method of a semiconductor device in accordance with an embodiment of the present disclosure.

[0015] FIG. 6 is an example of a configuration view of a microprocessor implementing a memory device in accordance with an embodiment of the present disclosure.

[0016] FIG. 7 is an example of a configuration view of a processor implementing a memory device in accordance with an embodiment of the present disclosure.

[0017] FIG. 8 is an example of a configuration view of a system implementing a memory device in accordance with an embodiment of the present disclosure.

[0018] FIG. 9 is an example of a configuration view of a memory system implementing a memory device in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0019] The specific structural or functional description disclosed herein is merely illustrative for the purpose of describing embodiments according to

the concept of the present disclosure. These embodiments according to the concept of the present disclosure can be implemented in various forms, and cannot be construed as being limited to the embodiments set forth herein.

[0020] FIG. 1 is a view illustrating a structure of a semiconductor device in accordance with an embodiment of the present disclosure.

[0021] Referring to FIG. 1, the semiconductor device in accordance with the embodiment of the present disclosure may include a first electrode 11, a second electrode 12, a barrier layer 13, and a variable resistance layer 14. The semiconductor device may include a memory cell MC, and the first electrode 11, the second electrode 12, the barrier layer 13, and the variable resistance layer 14 may constitute the memory cell MC.

[0022] The first electrode 11 may be a portion of a word line or a bit line, or be electrically connected to the word line or the bit line. The first electrode 11 may include a conductive material such as poly-silicon or metal. In an embodiment, the first electrode 11 may include poly-silicon, tungsten (W), tungsten nitride (WNx), tungsten silicide (WSix), titanium (Ti), titanium nitride (TiNx), titanium silicon nitride (TiSiN), titanium aluminum nitride (TiAlN), tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tantalum aluminum nitride (TaAlN), carbon (C), carbon nitride (CNx) silicon carbide (SiC), silicon carbon nitride (SiCN), copper (Cu), zinc (Zn), nickel (Ni), cobalt (Co), lead (Pd), platinum (Pt), molybdenum (Mo), ruthenium (Ru), or the like, or include a combination thereof.

[0023] The second electrode 12 may be a portion of a bit line or a word line, or be electrically connected to the bit line or the word line. When the first electrode 11 is electrically connected to the word line, the second electrode 12 may be electrically connected to the bit line. The first electrode 11 may include a conductive material such as poly-silicon or metal. In an embodiment, the second electrode 12 may include poly-silicon, tungsten (W), tungsten nitride (WNx), tungsten silicide (WSix), titanium (Ti), titanium nitride (TiNx), titanium silicon nitride (TiSiN), titanium aluminum nitride (TiAlN), tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tantalum aluminum nitride (TaAlN), carbon (C), carbon nitride (CNx) silicon carbide (SiC), silicon carbon nitride (SiCN), copper (Cu), zinc (Zn), nickel (Ni), cobalt (Co), lead (Pd), platinum (Pt), molybdenum (Mo), ruthenium (Ru), or the like, or include a combination thereof. In an embodiment, the second electrode 12 may include a carbon layer.

[0024] The variable resistance layer 14 may be located between the first electrode 11 and the second electrode 12. The variable resistance layer 14 may include a resistive material, and have a characteristic of reversibly changing between different resistance states according to an applied voltage or current.

[0025] In an embodiment, the variable resistance layer 14 may include a transition metal oxide or include a metal oxide such as a perovskite-based material. Thus, an electrical path is generated or eliminated in the variable resistance layer 14, so that data can be stored in the memory cell.

[0026] In an embodiment, the variable resistance layer 14 may have an MTJ (Magnetic Tunnel Junction) structure, and include a magnetization fixed layer, a magnetization free layer, and a tunnel barrier layer interposed therebetween. For example, the magnetization fixed layer and the magnetization free layer may include a magnetic material, and the tunnel barrier layer may include oxide such as magnesium (Mg), aluminum (Al), zinc (Zn), or titanium (Ti). The magnetization direction of the magnetization free layer may be changed by spin torque of electrons in an applied current. Therefore, data may be stored in the memory cell according to a change in the magnetization direction of the magnetization free layer with respect to the magnetization direction of the magnetization fixed layer.

[0027] In an embodiment, the variable resistance layer 14 may include a phase change material, and include chalcogenide-based material. The variable resistance layer 14 may include chalcogenide glass, a chalcogenide alloy, etc. The variable resistance layer 14 may include silicon (Si), germanium (Ge), antimony (Sb), tellurium (Te), bismuth (Bi), indium (In), tin (Sn), selenium (Se), or the like, or include a combination thereof. In an embodiment, the variable resistance layer 14 may be Ge-Sb-Te (GST), and be $Ge_2Sb_2Te_5$, $Ge_2Sb_2Te_7$, $Ge_1Sb_2Te_4$, $Ge_1Sb_4Te_7$, or the like. The variable resistance layer 14 may be phase-changed depending on a program operation. In an embodiment, the variable resistance layer 14 may have a low-resistance crystalline state due to a set operation. In an embodiment, the variable resistance layer 14 may have a high-

resistance amorphous state due to a reset operation. Therefore, data may be stored in the memory cell by using a resistance difference caused by a phase change of the variable resistance layer 14.

[0028] In an embodiment, the variable resistance layer 14 may include a variable resistance material of which resistance is changed without any phase change, and include a chalcogenide-based material. The variable resistance layer 14 may include germanium (Ge), antimony (Sb), tellurium (Te), arsenic (As), selenium (Se), silicon (Si), indium (In), tin (Sn), sulfur (S), gallium (Ga), or the like, or include a combination thereof. The variable resistance layer 14 may include a chalcogenide-based material which maintains an amorphous state in a program operation. The variable resistance layer 14 has an amorphous state, and may not be changed to a crystalline state in the program operation. Therefore, the threshold voltage of the memory cell may be changed according to a program voltage applied to the memory cell, and the memory cell may be programmed to at least two states. In an embodiment, when a negative program voltage is applied to the memory cell, the memory cell may have a relatively high threshold voltage. In an embodiment, when a positive program voltage is applied to the memory cell, the memory cell may have a relatively low threshold voltage. Therefore, data may be stored in the memory cell by using a threshold voltage difference of the memory cell.

[0029] The barrier layer 13 may be interposed between the first electrode 11 and the variable resistance layer 14, or between the second electrode 12 and the variable resistance layer 14, or both. The barrier layer 13

may have an amorphous state. For example, the barrier layer 13 may include one or more elements (e.g., carbon) included in the first electrode 11, or the second electrode 12, or both. The barrier layer 13 may include nitrogen and carbon. In an embodiment, the barrier layer 13 may include carbon nitride. The barrier layer 13 may include CxNy, and x and y may be integers of 1 or more. In the barrier layer 13, a concentration of the nitrogen may be equal to that of the carbon or be higher than that of the carbon. When the concentration of the nitrogen increases, specific resistance may increase. The barrier layer 13 may be a non-conductor in which current does not flow or hardly flows. In an embodiment, the barrier layer 13 may include C_3N_4.

[0030] The barrier layer 13 may have a relatively small volume as compared with the first electrode 11. The barrier layer 13 may be formed with a relatively thin thickness on a surface of the first electrode 11. In an embodiment, the volume of the barrier layer 13 may be 1% to 10% of that of the first electrode 11. In an embodiment, the thickness of the barrier layer 13 may be 1 Å to 10 Å. When the volume or thickness of the barrier layer 13 is relatively large, a firing voltage for activating the memory cell increases, and hence the variable resistance layer 14 may be damaged. Also, when the volume or thickness of the barrier layer 13 is relatively large, current may not flow. For example, when the volume of the barrier layer 13 exceeds 10% of the volume of the first electrode 11, the firing voltage for activating the memory cell may become excessively high to damage the variable resistance layer 14

and a current may not flow through the barrier layer 13 even when a program voltage is applied to the memory cell. When the volume of the barrier layer 13 is less than 1% of the volume of the first electrode 11, the barrier layer 13 may not sufficiently increase a read window margin of the memory cell MC. Thus, in accordance with the embodiment of the present disclosure, the barrier layer 13 is formed to have a small volume or thickness as compared with the first electrode 11, so that the damage of the variable resistance layer 14 can be substantially prevented. Further, current can flow through the barrier layer 13 in the program operation.

[0031] According to the structure described above, the first electrode 11, the second electrode 12, the barrier layer 13, and the variable resistance layer 14 may constitute the memory cell MC. In an embodiment, the memory cell MC may serve as a selection element while being a memory element. Alternatively, the memory cell MC may separately include a selection element or a memory element. Also, the memory cell MC includes the barrier layer 13, so that a read window margin of the memory cell MC can be increased.

[0032] FIG. 2 is a view illustrating a structure of a semiconductor device in accordance with an embodiment of the present disclosure.

[0033] Referring to FIG. 2, the semiconductor device may include word lines WL, bit lines BL, and memory cells MC. The word lines WL may extend in a first direction I. The bit lines BL may extend in a second direction II intersecting the first direction I.

[0034] The memory cells MC may be located in intersection regions of the word lines WL and the bit lines BL. In an embodiment, each of the memory cells MC may include a barrier layer 23 and a variable resistance layer 24. The barrier layer 23 may be located between the word line WL and the variable resistance layer 24, or be located between the bit line BL and the variable resistance layer 24, or both. The variable resistance layer 24 and the barrier layer 23 may be stacked in a third direction III. The third direction III may be a direction protruding from a plane defined by the first direction I and the second direction II, and protrude vertically from the plane.

[0035] The memory cells MC may further include a first electrode interposed between the word line WL and the barrier layer 23, or include a second electrode interposed between the bit line BL and the variable resistance layer 24, or both. Alternatively, a portion of the word line WL may be the first electrode, or a portion of the bit line BL may be the second electrode.

[0036] Meanwhile, although FIG. 2 illustrates a structure in which the memory cells MC are arranged in the first direction I and the second direction II, the memory cells MC may be stacked in the third direction III. The bit lines BL and the word lines WL may be alternately stacked, and the memory cells MC may be located between the bit lines BL and the word lines WL, which are stacked.

[0037] FIGS. 3A and 3B are views each illustrating a structure of a semiconductor device in accordance with an embodiment of the present

disclosure. Hereinafter, descriptions of portions overlapping with those described above may be omitted for the interest of brevity.

[0038] Referring to FIGS. 3A and 3B, the semiconductor device may include a stack structure ST, a barrier layer 33, a variable resistance layer 34, and a second conductive layer 32. The semiconductor device may further include a gap fill layer 37.

[0039] The stack structure ST may include first conductive layers 31 and insulating layers 36, which are alternately stacked. The first conductive layers 31 may include a conductive material such as poly-silicon or metal. In an embodiment, the first conductive layers 31 may include poly-silicon, tungsten (W), tungsten nitride (WNx), tungsten silicide (WSix), titanium (Ti), titanium nitride (TiNx), titanium silicon nitride (TiSiN), titanium aluminum nitride (TiAlN), tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tantalum aluminum nitride (TaAlN), carbon (C), carbon nitride (CNx) silicon carbide (SiC), silicon carbon nitride (SiCN), copper (Cu), zinc (Zn), nickel (Ni), cobalt (Co), lead (Pd), platinum (Pt), molybdenum (Mo), ruthenium (Ru), or the like, or include a combination thereof. In an embodiment, the first conductive layers 31 may include a carbon layer. The first conductive layers 31 may be word lines or bit lines. The insulating layers 36 are used to insulate the first conductive layers 31 from each other, and may include an insulating material such as oxide or nitride.

[0040] The second conductive layer 32 may penetrate the stack structure ST. Referring to FIG. 3A, the second conductive layer 32 may have a

structure of which a central region is opened. The gap fill layer 37 may be filled in the second conductive layer 32. Referring to FIG. 3B, the second conductive layer 32 may have a structure in which the second conductive layer 32 is filled up to the central region thereof. The gap fill layer 37 may not be formed in the second conductive layer 32.

[0041] The second conductive layer 32 may include poly-silicon, tungsten (W), tungsten nitride (WNx), tungsten silicide (WSix), titanium (Ti), titanium nitride (TiNx), titanium silicon nitride (TiSiN), titanium aluminum nitride (TiAlN), tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tantalum aluminum nitride (TaAlN), carbon (C), carbon nitride (CNx) silicon carbide (SiC), silicon carbon nitride (SiCN), copper (Cu), zinc (Zn), nickel (Ni), cobalt (Co), lead (Pd), platinum (Pt), molybdenum (Mo), ruthenium (Ru), or the like, or include a combination thereof. In an embodiment, the second conductive layer 32 may include a carbon layer. The second conductive layer 32 may be a bit line or a word line. When the first conductive layers 31 are word lines, the second conductive layer 32 may be a bit line.

[0042] The variable resistance layer 34 may be interposed between the first conductive layers 31 and the second conductive layer 32. In an embodiment, the variable resistance layer 34 may be formed to surround a sidewall of the second conductive layer 32.

[0043] The barrier layer 33 may be interposed between the variable resistance layer 34 and the first conductive layers 31, or between the variable resistance layer 34 and the second conductive layer 32, or both.

In an embodiment, the barrier layer 33 may be formed to surround a sidewall of the variable resistance layer 34.

[0044] According to the structure described above, memory cells may be located in intersection regions of the first conductive layers 31 and the second conductive layer 32. The stacked memory cells may share the barrier layer 33, the variable resistance layer 34, and the second conductive layer 32.

[0045] FIG. 4 is a view illustrating a structure of a semiconductor device in accordance with an embodiment of the present disclosure. Hereinafter, descriptions of portions overlapping with those described above may be omitted for the interest of brevity.

[0046] Referring to FIG. 4, the semiconductor device may include a stack structure ST, barrier layers 43, variable resistance layers 44, and a second conductive layer 42. The semiconductor device may further include a gap fill layer 47.

[0047] The stack structure ST may include first conductive layers 41 and insulating layers 46. The second conductive layer 42 may penetrate the stack structure ST. The second conductive layer 42 may have a structure of which a central region is opened, or have a structure in which the second conductive layer 42 is filled up to the central region thereof.

[0048] Each of the barrier layers 43 may be interposed between the first conductive layers 41 and the second conductive layer 42, and extend between the insulating layers 46 and the first conductive layer 41. The barrier layers 43 may respectively surround the variable resistance layers

44. Each of the barrier layers 43 may have a C-shaped section.

[0049] Each of the variable resistance layers 44 may be interposed between the first conductive layers 41 and the second conductive layer 42, and extend between the insulating layers 46 and the first conductive layers 41. The variable resistance layers 44 may be respectively interposed between the barrier layers 43 and the first conductive layers 41. The variable resistance layers 44 may respectively surround the first conductive layers 41. Each of the variable resistance layers 44 may have a C-shaped section.

[0050] According to the structure described above, memory cells may be located in intersection regions of the first conductive layers 41 and the second conductive layer 42. The barrier layers 43 and the variable resistance layers 44 of the stacked memory cells may be isolated from each other. The stacked memory cells may share the second conductive layer 42.

[0051] FIGS. 5A and 5B are views illustrating a manufacturing method of a semiconductor device in accordance with an embodiment of the present disclosure. Hereinafter, descriptions of portions overlapping with those described above may be omitted for the interest of brevity.

[0052] Referring to FIG. 5A, a first electrode 51 is formed. In an embodiment, the first electrode 51 may include a carbon layer. Subsequently, a barrier layer 53 is formed on the first electrode 51. The barrier layer 53 may include nitrogen and carbon. The barrier layer 53 may include carbon nitride in which a concentration of the nitrogen is

equal to that of the carbon or is higher than that of the carbon. In an embodiment, the barrier layer 53 may include C_3N_4.

[0053] The barrier layer 53 may be formed through a deposition process. The deposition process of the barrier layer 53 may be performed in-situ with that of the first electrode 51. The barrier layer 53 may be deposited through a Physical Vapor Deposition (PVD) process. In the deposition, a nitrogen gas having a relatively large amount may be used with relatively low power, thereby forming the barrier layer 53 in an amorphous state. In an embodiment, the barrier layer 53 may be deposited by using a nitrogen gas having an amount of 15 sccm to 30 sccm with power of 50 W to 1000 W. Accordingly, carbon nitride having the amorphous state may be formed.

[0054] The barrier layer 53 may be a non-conductor in which current does not flow or hardly flows. Therefore, the barrier layer 53 may be formed to have a relatively small volume or a relatively thin thickness as compared with the first electrode 51 such that current can flow through the barrier layer 53 in a program operation. In an embodiment, the barrier layer 53 (e.g., carbon nitride layer) is formed to have a volume which is 1% to 10% of that of the first electrode 51. In an embodiment, the carbon nitride layer 53 is formed to have a thickness of 1 Å to 10 Å.

[0055] Subsequently, a variable resistance layer 54 is formed on the barrier layer 53. Subsequently, a second electrode 52 is formed on the variable resistance layer 54. In an embodiment, the second electrode 52 may include a carbon layer.

[0056] According to the manufacturing method described above, the barrier layer 53 can be formed between the first electrode 51 and the variable resistance layer 54. Thus, a read window margin of a memory cell can be ensured. Further, since the barrier layer 53 is formed before the variable resistance layer 54 is formed, the variable resistance layer 54 can be prevented from being nitrified even when the barrier layer 53 is formed by using a relatively large amount of nitrogen gas, thereby preventing a firing voltage from being excessively increased.

[0057] The memory circuit or the semiconductor device of the above-described embodiments can be used in various devices or systems. FIGS. 6 to 9 illustrate some examples of a device or system, which can implement the memory circuit or the semiconductor device of the above-described embodiments.

[0058] FIG. 6 is an example of a configuration view of a microprocessor implementing a memory device in accordance with an embodiment of the present disclosure.

[0059] Referring to FIG. 6, the microprocessor 1000 may perform tasks for controlling and tuning a series of processes of receiving data from various external devices, processing the data, and outputting processing results to external devices. The microprocessor 1000 may include a memory 1010, an operating component 1020, a controller 1030, and the like. The microprocessor 1000 may be various data processing units such as a central processing unit (CPU), a graphic processing unit (GPU), a digital signal processor (DSP), and an application processor (AP).

[0060] The memory 1010 is a part which stores data in the microprocessor 1000, as a processor register, register or the like. The memory 1010 may include various registers such as a data register, an address register, and a floating point register. The memory 1010 may perform the function of temporarily storing data for which operations are to be performed by the operating component 1020, result data of performing the operations and addresses where data for performing of the operations are stored.

[0061] The memory 1010 may include one or more of the above-described embodiments of the semiconductor device. For example, the memory 1010 may include at least one memory element, and the memory element may include: a first electrode including a carbon layer; a second electrode; a variable resistance layer interposed between the first electrode and the second electrode; and a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including nitrogen and carbon, wherein a concentration of the nitrogen is equal to or higher than that of the carbon. Accordingly, the reliability of the memory 1010 can be enhanced, and a manufacturing process can be improved. Consequently, operation characteristics of the microprocessor 1000 can be improved.

[0062] The operating component 1020 may perform several arithmetical operations or logical operations according to results that the controller 1030 decodes commands. The operating component 1020 may include at least one arithmetic logic unit (ALU) and the like.

[0063] The controller 1030 may receive signals from the memory 1010, the operating component 1020 and an external device of the microprocessor 1000, perform extraction, decoding of commands, and controlling input and output of signals of the microprocessor 1000, and execute processing represented by programs.

[0064] The microprocessor 1000 in accordance with this embodiment may additionally include a cache memory 1040 which can temporarily store data to be inputted from an external device or to be outputted to an external device, other than the memory 1010. The cache memory 1040 may exchange data with the memory 1010, the operating component 1020 and the controller 1030 through a bus interface 1050.

[0065] FIG. 7 is an example of a configuration view of a processor implementing a memory device in accordance with an embodiment of the present disclosure.

[0066] Referring to FIG. 7, the processor 1100 may improve performance and realize multi-functionality by including various functions other than those of the above-described microprocessor 1000. The processor 1100 may include a core 1110 which serves as the microprocessor, a cache memory 1120 which serves to storing data temporarily, and a bus interface 1130 for transferring data between internal and external devices. The processor 1100 may include various system-on-chips (SoCs) such as a multi-core processor, a graphic processing unit (GPU), and an application processor (AP).

[0067] The core 1110 of this embodiment is a part which performs

arithmetic logic operations for data inputted from an external device, and may include a memory 1111, an operating component 1112 and a controller 1113. The memory 1111, the operating component 1112, and the controller 1113 may be substantially identical to the memory 1010, the operating component 1020, and the controller 1030, which are described above.

[0068] The cache memory 1120 is a part which temporarily stores data to compensate for a difference in data processing speed between the core 1110 operating at a high speed and an external device operating at a low speed. The cache memory 1120 may include a primary storage section 1121, a secondary storage section 1122, and include a tertiary storage section 1123 in the case where high storage capacity is required. As the occasion demands, the cache memory 1120 may include an increased number of storage sections. That is, the number of storage sections which are included in the cache memory 1120 may be changed according to a design. The speeds at which the primary, secondary and tertiary storage sections 1121, 1122 and 1123 store and discriminate data may be the same or different. In the case where the speeds of the respective storage sections 1121, 1122 and 1123 are different, the speed of the primary storage section 1121 may be largest. At least one storage section of the primary storage section 1121, the secondary storage section 1122 and the tertiary storage section 1123 of the cache memory 1120 may include one or more of the above-described embodiments of the memory device. For example, the cache memory 1120 may include

at least one memory element, and the memory element may include: a first electrode including a carbon layer; a second electrode; a variable resistance layer interposed between the first electrode and the second electrode; and a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including nitrogen and carbon, wherein a concentration of the nitrogen is equal to or higher than that of the carbon. Accordingly, the reliability of the cache memory 1120 can be enhanced, and a manufacturing process can be improved. Consequently, operation characteristics of the processor 1100 can be improved.

[0069] Although a case where all the primary, secondary and tertiary storage sections 1121, 1122 and 1123 are configured inside the cache memory 1120 is illustrated in this embodiment, some or all of the primary, secondary and tertiary storage sections 1121, 1122 and 1123 of the cache memory 1120 may be configured inside the core 1110 and may compensate for a difference in data processing speed between the core 1110 and the external device.

[0070] The bus interface 1130 is a part which connects the core 1110, the cache memory 1120 and external device and allows data to be efficiently transmitted.

[0071] The processor 1100 in accordance with this embodiment may include a plurality of cores 1110, and the plurality of cores 1110 may share the cache memory 1120. The plurality of cores 1110 and the cache memory 1120 may be directly connected or be connected through

the bus interface 1130. The plurality of cores 1110 may be configured in the same way as the above-described configuration of the core 1110. The storage section in each of the plurality of cores 1110 may be configured outside the core 1110 in such a way as to be shared through the bus interface 1130.

[0072] The processor 1100 in accordance with this embodiment may further include an embedded memory 1140 which stores data, a communication module 1150 which can transmit and receive data to and from an external device in a wired or wireless manner, a memory controller 1160 which drives an external memory device, and a media processor 1170 which processes the data processed in the processor 1100 or the data inputted from an external input device and outputs the processed data to an external interface device, and the like. Besides, the processor 1100 may include a plurality of various modules and devices. The plurality of modules which are added may exchange data with the cores 1110 and the cache memory 1120 and with one another, through the bus interface 1130.

[0073] The embedded memory 1140 may include not only a volatile memory but also a nonvolatile memory. The volatile memory may include a DRAM (dynamic random access memory), a mobile DRAM, an SRAM (static random access memory), and a memory with similar functions to above mentioned memories, and the like. The nonvolatile memory may include a ROM (read only memory), a NOR flash memory, a NAND flash memory, a phase change random access memory (PRAM), a

resistive random access memory (RRAM), a spin transfer torque random access memory (STTRAM), a magnetic random access memory (MRAM), a memory with similar functions.

[0074] The communication module 1150 may include a module capable of being connected with a wired network, a module capable of being connected with a wireless network and both of them. The wired network module may include a local area network (LAN), a universal serial bus (USB), an Ethernet, power line communication (PLC) such as various devices which send and receive data through transmit lines, and the like. The wireless network module may include Infrared Data Association (IrDA), code division multiple access (CDMA), time division multiple access (TDMA), frequency division multiple access (FDMA), a wireless LAN, Zigbee, a ubiquitous sensor network (USN), Bluetooth, radio frequency identification (RFID), long term evolution (LTE), near field communication (NFC), a wireless broadband Internet (Wibro), high speed downlink packet access (HSDPA), wideband CDMA (WCDMA), ultra wideband (UWB) such as various devices which send and receive data without transmit lines, and the like.

[0075] The memory controller 1160 is to administrate and process data transmitted between the processor 1100 and an external storage device operating according to a different communication standard. The memory controller 1160 may include various memory controllers, for example, devices which may control IDE (Integrated Device Electronics), SATA (Serial Advanced Technology Attachment), SCSI (Small Computer System

Interface), RAID (Redundant Array of Independent Disks), an SSD (solid state disk), eSATA (External SATA), PCMCIA (Personal Computer Memory Card International Association), a USB (universal serial bus), a secure digital (SD) card, a mini secure digital (mSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and the like.

[0076] The media processor 1170 may process the data processed in the processor 1100 or the data inputted in the forms of image, voice and others from the external input device and output the data to the external interface device. The media processor 1170 may include a graphic processing unit (GPU), a digital signal processor (DSP), a high definition audio device (HD audio), a high definition multimedia interface (HDMI) controller, and the like.

[0077] FIG. 8 is an example of a configuration view of a system implementing a memory device in accordance with an embodiment of the present disclosure.

[0078] Referring to FIG. 8, the system 1200 as an apparatus for processing data may perform input, processing, output, communication, storage, etc. to conduct a series of manipulations for data. The system 1200 may include a processor 1210, a main memory device 1220, an auxiliary memory device 1230, an interface device 1240, and the like. The system 1200 of this embodiment may be various electronic systems which operate using processors, such as a computer, a server, a PDA

(personal digital assistant), a portable computer, a web tablet, a wireless phone, a mobile phone, a smart phone, a digital music player, a PMP (portable multimedia player), a camera, a global positioning system (GPS), a video camera, a voice recorder, a telematics, an audio visual (AV) system, a smart television, and the like.

[0079] The processor 1210 may decode inputted commands and processes operation, comparison, etc. for the data stored in the system 1200, and controls these operations. The processor 1210 may be substantially identical to the above-described microprocessor 1000 or the above-described processor 1100.

[0080] The main memory device 1220 is a storage which can temporarily store, call and execute program codes or data from the auxiliary memory device 1230 when programs are executed and can conserve memorized contents even when power supply is cut off.

[0081] The auxiliary memory device 1230 is a memory device for storing program codes or data. While the speed of the auxiliary memory device 1230 is slower than the main memory device 1220, the auxiliary memory device 1230 can store a larger amount of data. The main memory device 1220 or the auxiliary memory device 1230 may include one or more of the above-described embodiments of the semiconductor device. For example, the main memory device 1220 or the auxiliary memory device 1230 may include at least one memory element, and the memory element may include: a first electrode including a carbon layer; a second electrode; a variable resistance layer interposed between the first

electrode and the second electrode; and a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including nitrogen and carbon, wherein a concentration of the nitrogen is equal to or higher than that of the carbon. Accordingly, the reliability of the main memory device 1220 or the auxiliary memory device 1230 can be enhanced, and a manufacturing process can be improved. Consequently, operation characteristics of the system 1200 can be improved.

[0082] The main memory device 1220 or the auxiliary memory device 1230 may include a memory system 1300 as shown in FIG. 9, in addition to the semiconductor memory of the above-described embodiment or without including the semiconductor memory of the above-described embodiment.

[0083] The interface device 1240 may be to perform exchange of commands and data between the system 1200 of this embodiment and an external device. The interface device 1240 may be a keypad, a keyboard, a mouse, a speaker, a mike, a display, various human interface devices (HIDs), a communication device, and the like. The communication device may be substantially identical to the above-described communication module 1150.

[0084] FIG. 9 is an example of a configuration view of a memory system implementing a memory device in accordance with an embodiment of the present disclosure.

[0085] Referring to FIG. 9, the memory system 1300 may include a

memory 1310 which has a nonvolatile characteristic as a component for storing data, a controller 1320 which controls the memory 1310, an interface 1330 for connection with an external device, and a buffer memory 1340 which temporarily stores data so as to efficiently transfer an input/output of data between the interface 1330 and the memory 1310. The memory system 1300 may mean a memory which simply stores data. Further, the memory system 1300 may mean a data storage device which conserves stored data in the long term. The memory system 1300 may be a card type such as a solid state disk (SSD), a USB memory (universal serial bus memory), a secure digital (SD) card, a mini secure digital (mSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and the like.

[0086] The memory 1310 or the buffer memory 1340 may include one or more of the above-described embodiments of the semiconductor device. For example, the memory 1310 or the buffer memory 1340 may include at least one memory element, and the memory element may include: a first electrode including a carbon layer; a second electrode; a variable resistance layer interposed between the first electrode and the second electrode; and a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including nitrogen and carbon, wherein a concentration of the nitrogen is equal to or higher than that of the carbon. Accordingly, the reliability of the memory 1310 or the

buffer memory 1340 can be enhanced, and a manufacturing process can be improved. Consequently, operation characteristics of the memory system 1300 can be improved.

[0087] The memory 1310 or the buffer memory 1340 may include various volatile or nonvolatile memories, in addition to the semiconductor memory of the above-described embodiment or without including the semiconductor memory of the above-described embodiment.

[0088] The controller 1320 may control exchange of data between the memory 1310 and the interface 1330. To this end, the controller 1320 may include a processor 1321 for performing an operation for processing commands inputted through the interface 1330 from an outside of the memory system 1300.

[0089] The interface 1330 is to perform exchange of commands and data between the memory system 1300 and the external device. When the memory system 1300 is of a card type or a disk type, the interface 1330 may be compatible with interfaces which are used in the card-type or disk-type devices, or be compatible with interfaces which are used in devices similar to the above mentioned devices. The interface 130 may be compatible with one or more interfaces having a different type from each other.

[0090] In accordance with embodiments of the present disclosure, the degree of integration of the semiconductor device can be improved. Further, the semiconductor device can have a stable structure and improved reliability.

[0091] Some embodiments have been described in the drawings and specification of the present disclosure. Although specific terminologies are used here, those are only to explain the embodiments of the present disclosure. Therefore, embodiments of the present disclosure are not restricted to the above-described embodiments and many variations are possible within the spirit and scope of the present disclosure. It should be apparent to those skilled in the art that various modifications can be made on the basis of the technological scope of the present disclosure in addition to the embodiments disclosed herein.

[0092] So far as not being differently defined, all terms used herein including technical or scientific terminologies have meanings that they are commonly understood by those skilled in the art to which the present disclosure pertains. The terms having the definitions as defined in the dictionary should be understood such that they have meanings consistent with the context of the related technique. So far as not being clearly defined in this application, terms should not be understood in an ideally or excessively formal way.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first electrode including a carbon layer;

a second electrode;

a variable resistance layer interposed between the first electrode and the second electrode; and

a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including nitrogen and carbon,

wherein a concentration of the nitrogen in the barrier layer is equal to or higher than that of the carbon in the barrier layer.

2. The semiconductor device of claim 1, wherein the barrier layer is in an amorphous state.

3. The semiconductor device of claim 1, wherein the barrier layer is a non-conductor.

4. The semiconductor device of claim 1, wherein a volume of the barrier layer is 1% to 10% of that of the first electrode.

5. The semiconductor device of claim 1, wherein the variable resistance layer maintains an amorphous state in a program operation.

6. A method of manufacturing a semiconductor device, the

method comprising:

forming a first electrode including a carbon layer;

forming, on the first electrode, a barrier layer including carbon nitride in which a concentration of nitrogen is equal to or higher than that of carbon;

forming a variable resistance layer on the barrier layer; and

forming a second electrode on the variable resistance layer.

7. The method of claim 6, wherein, in the forming of the barrier layer, the carbon nitride having an amorphous state is formed.

8. The method of claim 6, wherein, in the forming of the barrier layer, the barrier layer as a non-conductor is formed.

9. The method of claim 6, wherein, in the forming of the barrier layer, the barrier layer is formed to have a volume which is 1% to 10% of that of the first electrode.

10. The method of claim 6, wherein, in the forming of the barrier layer, the barrier layer is deposited through a Physical Vapor Deposition (PVD) process by using a nitrogen gas having an amount of 15 sccm to 30 sccm with power of 50 W to 1000 W.

11. The method of claim 6, wherein the variable resistance layer

maintains an amorphous state in a program operation.

12. A semiconductor device comprising:

a first electrode including a first element;

a second electrode;

a variable resistance layer interposed between the first electrode and the second electrode; and

a barrier layer interposed between the first electrode and the variable resistance layer, the barrier layer including the first element and a second element,

wherein a concentration of the second element in the barrier layer is equal to or higher than that of the first element in the barrier layer, and the barrier layer is in an amorphous state.

13. The device of clam 12, wherein the first element is carbon, and the second element is nitrogen.

14. The device of claim 12, wherein a volume of the barrier layer is 1% to 10% of that of the first electrode.

15. The device of claim 12, wherein a thickness of the barrier layer is 1 Å to 10 Å.