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# METHOD OF FORMING PID PROTECTION DIODE FOR SOI WAFER

**by**

## BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a semiconductor integrated microelectronic circuit device having a silicon-on-insulator (SOI) structure.

Description of the Related Art

SOI (silicon-on-insulator) technology is the fabrication of integrated semiconductor microelectronics circuitry on a three-layer substrate consisting of an upper layer of monocrystalline silicon, a layer of insulating material, usually an oxide of silicon, and an underlying layer of monocrystalline silicon. Although there are several methods for forming the SOI structure, wafer bonding or the SIMOX (separation by implanted oxygen) technique, which forms a buried oxide layer by driving oxygen ions into the silicon substrate, is commonly used. The circuitry is then primarily fabricated in the upper silicon layer, wherein it is substantially electrically isolated from the underlying silicon layer. SOI technology has become important precisely because it has the virtue of providing such degrees of isolation between circuit elements.

The very isolation of the thin upper silicon layer from the more substantial lower layer presents the possibility of unwanted surge currents in signal input lines, such as those caused by electrostatic discharges and the like, damaging circuit elements. One accepted way of ameliorating the effects of such currents is to provide the input line with a protective diode circuit to channel current surges away from the affected regions. Tsuruta et al. (U. S. Patent No. 5,567,968) teach the formation of a protective diode structure that allows the passage of high currents in MOSFET circuitry fabricated in SOI layers. They teach a particular diode structure wherein a p-type semiconductor layer and an n-type semiconductor layer are electrically connected by a buried semiconductor layer to form a vertically disposed pn-junction. The diode so formed is then itself connected electrically to an adjacent MOSFET and thereby functions as an electrostatic discharge protection element. Suzuki et al. (U. S. Patent No. 5,751,041) teach a method of protecting a CMOS inverter circuit formed in an SOI substrate by use of an np-diode connected between the signal input line and ground. They teach the formation of a second diffusion layer of a conductivity type that is the same as but of a higher concentration than that of the substrate, so as to circumscribe the extent of the depletion region and eliminate unwanted leakage currents. Fukumoto et al. (U. S. Patent No. 5,786,616) teach the formation of a diode type circuit that protects against two types of surges: a surge between the signal input terminal and a ground terminal, and a surge between a signal input terminal and a power supply terminal, with the latter surge protection being the novel element of the invention. According to the method taught by Fukumoto et al., the power supply to signal input surges are protected against by a

parasitic diode element formed between a resistor diffusion region and the underlying semiconductor substrate.

As can be seen from the above, the use of diode circuitry of one form or another to protect integrated SOI microelectronic circuits is an accepted part of the present art of fabricating such circuitry. Such protection, however, is not only needed when the SOI circuits are in actual use, it is also needed to protect the SOI circuitry from hazards that arise during its fabrication. In particular, the extensive use of plasmas in such fabrication processes as plasma assisted film depositions and etching causes the accumulation of charge deposits on conductive surfaces. If these charge excesses were not removed, they would produce potential differences across gate oxides which would be sufficient to cause their breakdown and damage or destroy transistors.

Another cause of circuit damage during SOI microelectronics fabrications as well as loss of circuit reliability is excessive heat buildup due to poor heat conduction and dissipation. The reduced size of modern microelectronic circuitry requires the use of low-k (low dielectric constant) materials to serve as interlayer dielectrics and insulating layers. Low-k materials, such as CORAL, manufactured by Novellus Corp., Black Diamond, manufactured by Applied Materials Corp., organic films from the Schumacher Corp. and various carbon-containing films, allow the formation of closely packed circuit elements without the attendant inter-element parasitic capacitances that would be associated with other dielectric materials. Unfortunately, such low-k dielectric materials also have low thermal conductivities, typically 0.24-0.37 W/k.m vs. 1.2 W/k.m for $SiO_2$, which allows localized heat buildup in the fabrication. None of the methods discussed above address the problem of heat buildup or its reduction. The present invention

addresses the heat dissipation problem simultaneously with the excess charge reduction problem by teaching a method of forming a PID protective diode that produces a structure capable of eliminating or significantly reducing both problems and does so efficiently, cost-effectively and in a manner that smoothly integrates its formation into the overall circuit fabrication scheme.

## SUMMARY OF THE INVENTION

It is an object of the present invention to teach a method of forming a "plasma-induced -damage" (PID) diode protective circuit for an SOI integrated microelectronic fabrication, such as a fabrication containing an arbitrary array of conductively interconnected nMOS and pMOS transistors disposed in single or multiple levels of integration.

It is yet another object of the present invention to teach a method of fabricating a PID diode protective circuit for an SOI integrated microelectronics fabrication that enhances the dissipation of heat produced during fabrication processes.

It is yet a further object of the present invention to teach a PID protective diode circuit fabrication method that is accomplished efficiently, cost-effectively and in a manner that smoothly integrates the diode formation into the overall fabrication scheme.

The objects of the present invention are achieved by a novel PID protective diode structure that conducts excess charge away from active portions of circuitry formed in the upper silicon layer of the SOI substrate, through a low resistance diode circuit, to the

lowest silicon layer of the SOI substrate and, at the same time, conducts excess heat away from said portions of the circuitry, similarly conveying such heat to the lower silicon layer of the SOI substrate wherein it can be dissipated without damage to the fabricated circuitry. This is achieved by conductively connecting said diode to metal layers and structures, formed in various shapes over the various levels containing active portions of the circuitry, said layers and structures serving both as charge collectors and heat sinks and, thereby, conveying both charge and heat, through inter-level vias, directly to the lowest silicon layer of the SOI substrate.

The objects of the present invention are further achieved efficiently and cost-effectively by making use of an alignment opening formed during the fabrication process through which to form the diode in the lowest silicon layer of the SOI substrate.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1-10 show, in schematic fashion, a sequence of processes leading to the fabrication of a typical microelectronics integrated circuit on an SOI substrate, incorporating a PID protective diode that eliminates excess charge and dissipates heat.

Fig. 1 shows a schematic cross-sectional view of a lightly doped p-type SOI substrate on which a photoresist film has been patterned for the production of shallow trench isolation (STI) regions that will separate active elements of the circuitry.

Fig. 2 shows a schematic cross sectional view of the SOI substrate of Fig. 1 subsequent to the formation of the STI regions and the removal of the photoresist film.

Fig. 3 shows a schematic cross-sectional view of the SOI substrate of Fig. 2 on which a second photoresist film has been deposited and patterned for the formation of an alignment opening.

Fig. 4 shows a schematic cross-sectional view of the SOI substrate of Fig. 3 subsequent to the etching back of the previously patterned alignment opening.

Fig. 5 shows a schematic cross-sectional view of the SOI substrate of Fig. 4 on which a third photoresist film has been patterned to allow the implantation of n type impurities into the upper silicon layer and into the portion of the lower silicon substrate exposed by the previous etching process depicted in Fig. 4, producing therein an n- well structure that will form the PID protective diode.

Fig. 6 shows a schematic cross-sectional view of the SOI substrate of Fig. 5 subsequent to the formation of gate electrodes and polysilicon spacers. The detailed structure of the electrodes is not critical to the present invention and is not shown herein.

Fig. 7 shows a schematic cross-sectional view of the SOI substrate of Fig. 6 subsequent to the deposition and patterning of a fourth photoresist film to allow implantation of n+ source/drain regions in the pMOS structures and to form an n+ well within the already implanted n- well of the PID protective diode formed in the underlying silicon substrate as shown in Fig. 5.

Fig. 8 shows a schematic cross-sectional view of the SOI substrate of Fig. 7 subsequent to the implantation of a high density of p-type impurities to form p+ source/drain regions for the nMOS structures and to selectively form salicide contact regions. The resulting SOI fabrication is then covered with an interlayer dielectric (ILD).

Fig. 9 shows a schematic cross-sectional view of the SOI substrate showing the formation of contacts to the salicides and the PID protection diode through the ILD.

Fig's. 10 A, B, C and D show a common side view (10A) and two different top views (B and C) of the fabrication of Fig. 9, on which has now been formed a layer of metal to act as both a heat sink and charge collector. The figures also show a top view of the conducting contacts that arise from a typical transistor in the SOI substrate beneath the ILD and are separated from the metal layer that connects to the PID protective diode. Fig's 10 B and C differ only in the shape of this metal layer, said shapes being only two among the many that could be formed as appropriate to the nature of the underlying circuitry. Fig. 10 D Shows a top view of a slightly different circuit configuration, wherein an entire transistor array would be located beneath an appropriately shaped opening in the metal layer.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

The fabrication method by which a protective PID diode circuit is incorporated into an SOI microelectronics integrated circuit will now be described with reference to the above figures. Referring first to Fig. 1, there is shown a schematic cross-sectional diagram of a three-layered SOI (silicon- on-insulator) substrate, comprising an upper monocrystalline silicon layer (10), an insulating layer (12), which can be a layer of silicon oxide, and a lower silicon layer (14). The upper and lower silicon layers are lightly doped with p-type conduction impurities in this particular example. The SOI substrate may be formed by wafer bonding, the SIMOX method or by other methods

known to practitioners of the art. The upper surface of the upper silicon layer (10) is shown covered with a first layer of photoresist (16) that has been patterned for the formation of shallow trench isolation (STI) regions. Although methods of forming STI regions are known to practitioners of the art, the method of the present invention etches the upper silicon layer (10) through the mask, fills the trenches so produced with silicon oxide or silicon oxynitride (18) and then planarizes the resulting formation.

Referring next to Fig. 2, there is shown the SOI substrate of Fig. 1 subsequent to the formation of the shallow trench isolation (STI) regions (18), the removal of the first photoresist layer and the planarization of the fabrication so produced.

Referring next to Fig. 3, there is shown the SOI substrate of Fig. 2 with the formation thereon of a second photoresist layer (20), patterned at (21) to allow the formation of an opening through the STI oxide (18) and the SOI oxide layer (12) (eg. by a $C_4F_8$ etch) to expose the lower silicon layer (14). The PID protection diode will ultimately be formed in the lower silicon layer (14), which layer does not contain the integrated microelectronics circuitry and, therefore, allows the formation of a larger diode appropriate to the magnitude of the discharges to be protected against.

Referring next to Fig. 4, there is shown the SOI substrate of Fig. 3 subsequent to the etching back of the STI (18) and SOI (12) oxides to produce an opening (22) to the lower silicon layer (14). The opening (22) serves both as an alignment opening for mask alignment and repair and as entry to the lower silicon layer (14) for the subsequent PID diode formation. The second photoresist layer ((20) in Fig. 3) has been removed.

Referring next to Fig. 5, there is shown the fabrication of Fig. 4 with the addition of a third photoresist layer (23) which has been patterned to allow the formation of an n-type well in the silicon substrate at (24), which will be the PID protection diode.

Referring next to Fig. 6, there is shown the fabrication of Fig. 5 subsequent to the removal of the third photoresist layer and the n-type doping that has now produced the substrate well (28) of the PID diode and other n-type doped regions (shown crosshatched). A succession of additional process steps (not shown) has also formed gate stacks (30) and sidewall spacers (32) on the upper silicon layer.

Referring next to Fig. 7, there is shown the fabrication of Fig. 6, subsequent to the patterning of a fourth photoresist layer (33) to allow the implant of a higher density of n-type ions so as to form an n+ region in the low density n-type substrate well (34) and to form n+ source and drain regions in selected MOS structures (36) of the microelectronics fabrication (shown heavily crosshatched). The n+ doping of the PID diode well allows a low-resistance contact to be subsequently formed on the PID diode.

Referring next to Fig. 8, there is shown the fabrication of Fig. 7 with the additional formation of silicided p+ implanted source/drain regions that have been formed, either on all S/D regions or selectively, by the salicide process (40) (shown oppositely crosshatched to the n-regions). The entire fabrication has then been covered by an interlayer dielectric (ILD) (42), which can be formed of sub-atmospheric BPSG (SABPSG), high density plasma deposited USG or FSG, carbon doped films or oxides, all deposited to a thickness of between 6,000 and 20,000 angstroms.

Referring, now, to Fig. 9, there is shown the fabrication of Fig. 8 with the additional formation of contacts (44) through the ILD, to selected circuit elements and to the PID diode, thereby allowing the PID diode to perform its protective role.

Fig's 10, A, B, C and D, show the formation of a metal layer over the fabrication of Fig. 9, said metal layer being conductively connected to the PID protective diode beneath it. Fig. 10A is a side view of the fabrication of Fig. 9, showing the metal layer (50). The PID diode is connected to this layer by its contact (44a) at (52). The emerging contacts (44b) from an exemplar circuit element beneath the ILD are connected to metal pieces, such as tungsten pieces, that do not touch the metal layer, but are separated from it by a distance that depends on the width of those pieces.

Fig. 10B is a schematic top view of the fabrication of Fig. 10A. The metal pieces (53) connected to the circuit element are shown separated from the metal layer (50) by at least an amount "X," said amount depending on the width of the metal pieces and being generally equal to or greater than the width of the metal pieces (53). As an example:

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|---|---|---|---|
| Metal Width (microns): | 0.19 | 0.24 | 0.36 |
| Spacing (microns): | >0.20 | >0.24 | >0.38 |

Additional metal layers may be formed over additional levels of circuit integration, passing conducting leads to the PID protective diode through vias formed in the appropriate ILD layers.

Fig. 10C shows a metal layer of a different shape (54), still serving the same purpose as the layer in Fig. 10B. In this particular shape, part of the layer has an antenna-like formation, allow better heat dissipation as might be appropriate to the particular

fabrication steps or circuitry formed below. The spacing, X, between the layer and the metal pieces still obeys the same rules.

Fig. 10D shows a metal layer shaped to accommodate a transistor array, SRAM or DRAM beneath it. The shapes of the layer depicted in B, C and D are by no means exhaustive.

As is understood by a person skilled in the art, the preferred embodiment of the present invention is illustrative of the present invention rather than being limiting of the present invention. Revisions and modifications may be made to methods, processes, materials, structures, and dimensions through which is formed a PID protective diode for an SOI wafer, while still providing a PID protective diode for an SOI wafer formed in accord with the present invention as defined by the appended claims.

What is claimed is:

1. A method of forming a heat-dissipating PID protective diode for an integrated semiconductor microelectronics circuit on an SOI substrate, comprising:

providing an SOI substrate;

forming and patterning a first photoresist layer on said SOI substrate;

forming a plurality of shallow trench isolation (STI) regions through said photoresist layer by means of a first etch process and STI oxide deposition, then removing said photoresist layer and planarizing the substrate;

forming and patterning a second photoresist layer on said SOI substrate;

removing a portion of STI and SOI oxide layer and exposing the lower silicon layer by a second etch process through said second photoresist layer and then removing said photoresist layer;

forming and patterning a third photoresist layer on said SOI substrate and implanting a certain low density of dopant ions into the exposed portion of the lower silicon layer through said third photoresist layer, forming thereby a PID protective np-diode structure and then removing said photoresist layer;

patterning and etching a plurality of gate electrodes and sidewall spacers over selected portions of the upper silicon layer of the SOI substrate, forming thereby a portion of a microelectronics fabrication in the upper silicon layer;

forming and patterning a fourth photoresist layer on said SOI substrate and implanting a certain high density of dopant ions through said photoresist layer into the exposed low density doped region of the PID protective diode in the lower silicon layer, forming thereby a region of higher dopant density and improved conductive contact

properties within the region of lower dopant density and also implanting said high density of dopant ions into selected regions of the upper silicon layer to form, thereby, source and drain regions for a plurality of transistors in the microelectronics fabrication and then removing said photoresist layer;

implanting a certain high density of dopant ions into selected regions of the upper silicon layer of the SOI substrate to form, thereby, silicided implanted source and drain regions for a plurality of transistors;

forming silicide contacts on the source, drain and gate regions of the transistors by a salicide process;

forming an interlayer dielectric (ILD) over the fabrication;

forming conducting contacts to the silicided regions of selected transistors of the microelectronics fabrication or to other selected circuit elements and to the implanted high dopant density region of the PID protective diode formed in the lower silicon layer of the SOI substrate, completing, thereby, a PID protective diode structure for the entire fabrication;

forming a metal layer over the ILD layer, said metal layer being in electrical contact with the contact from the PID diode, but not being in electrical contact with the contacts of the selected transistors or circuit elements;

forming, if required, additional levels of microelectronic integration over the fabrication;

forming, over each such additional level, a metal layer connected, through vias, to the PID protective diode.

2. The method of claim 1 wherein the SOI substrate is formed by the SIMOX method or by a method of wafer bonding.

3. The method of claim 1, wherein the upper and lower silicon layers of the SOI substrate are doped with a low density of p-type ions.

4. The method of claim 1, wherein the first etch process is an etch by a chemical etchant chosen from among the group consisting of $Cl_2$, HBr and $SF_6$.

5. The method of claim 3, wherein the low density of ions implanted through the third photoresist layer are n-type ions such as As or P ions, and they are implanted to a density of between 5E13 and 1E15 ions per cubic centimeter.

6. The method of claim 5, wherein the high density ions implanted through the fourth photoresist layer are n-type ions such as As or P ions and they are implanted to a density of between 1E15 and 5E15 ions per cubic centimeter.

7. The method of claim 1, wherein the high density of ions implanted into selected regions of the upper silicon layer to form source and drain regions are p-type ions, such as B or $BF_2$ ions and they are implanted to a density of between 5E13 and 1E15 ions per cubic centimeter.

8. The method of claim 1, wherein the ILD is formed of a layer of dielectric material chosen from among the group consisting of BPSG, FSG, USG or various oxides, with a thickness of between 6000 angstroms and 20,000 angstroms.

9. The method of claim1, wherein the contacts through the ILD to the PID diode and silicided regions of the MOS devices are formed of tungsten.

10. The method of claim 1, wherein the metal layer covering the ILD is shaped such that it optimally collects excess charges and dissipates heat generated by subsequent fabrication processes, such shapes consisting of, but not limited to, perimeter pieces, fingers and antenna shaped projections, formed so as to maintain a certain minimum distance from any nearby conductive contacts to the circuitry below.

11. The method of claim 10, wherein the spacing between the metal layer and any nearby conductive contacts is at least the width of those conductive contacts.