CLAIMS

What is claimed is:

1. An apparatus for implementing signed numerical values, the apparatus comprising:

an optical detector comprising a first terminal and a second terminal;

a first switch coupling the first terminal of the optical detector to either a node or a reference voltage;

a second switch coupling the second terminal of the optical detector to either the node or to a voltage rail; and

control circuitry configured to:

produce a positively-signed numerical value output at least in part by setting the first switch to couple the first terminal to the reference voltage and setting the second switch to couple the second terminal to the node; and

produce a negatively-signed numerical value output at least in part by setting the first switch to couple the first terminal to the node and setting the second switch to couple the second terminal to the voltage rail.

2. The apparatus of claim 1, wherein the optical detector comprises a photodiode;

the first terminal comprises an anode; and

the second terminal comprises a cathode.

3. The apparatus of claim 1, wherein the first switch and the second switch each comprise a transistor switch.

4. The apparatus of claim 1, wherein the reference voltage is ground.

5. The apparatus of claim 1, wherein the control circuitry comprises logical gate configured to output a sign orientation bit, wherein the sign orientation bit comprises information indicative of whether the numerical value output comprises a positively-signed or negatively-signed numerical value.

6. The apparatus of claim 5, wherein the logical gate comprises an XOR gate.

7. The apparatus of claim 5, wherein the logical gate is configured to compare a sign of a value of an input vector element and a sign of a value of an input matrix element.

8. An optical processing system, comprising:

a first plurality of optical modulators, each configured to receive an input optical signal, modulate the input optical signal, and output a first optical signal representing an element of a vector;

a second plurality of optical modulators, each optically coupled to an optical modulator of the first plurality of optical modulators and configured to receive the first optical signal, modulate the first optical signal, and output a second optical signal representing a portion of a matrix-vector multiplication between the vector and a matrix;

a plurality of optical detectors each optically coupled to optical modulators of the second plurality of optical modulators and configured to convert the second optical signal into an electrical signal representing the portion of the matrix-vector multiplication, wherein each optical detector of the plurality of optical detectors comprises a first terminal and a second terminal;

a first switch coupling the first terminal of a first optical detector to either an output node or a reference voltage;

a second switch coupling the second terminal of the first optical detector to either the output node or to a voltage rail; and

control circuitry configured to:

produce a positively-signed numerical value output at least in part by setting the first switch to couple the first terminal of the first optical detector to the reference voltage and setting the second switch to couple the second terminal of the first optical detector to the output node; and

produce a negatively-signed numerical value output at least in part by setting the first switch of the first optical detector to couple the first terminal to the output node and setting the second switch of the first optical detector to couple the second terminal to the voltage rail.

9. The optical processing system of claim 8, wherein the optical detector comprises a photodiode;

the first terminal comprises an anode; and

the second terminal comprises a cathode.

10. The optical processing system of claim 9, wherein the first switch and the second switch each comprise a transistor switch.

11. The optical processing system of claim 9, wherein the reference voltage is grounded.

12. The optical processing system of claim 9, further comprising a plurality of electrical summing circuits, wherein:

a first electrical summing circuit of the plurality is coupled to two or more output nodes, each output node of the two or more output nodes being coupled to an optical detector through the first switch or the second switch; and

the first electrical summing circuit is configured to output an electrical signal representing a sum of the portions of the matrix-vector operation output by the optical detectors coupled to the two or more output nodes.

13. The optical processing system of claim 8, wherein the control circuitry comprises logical gate configured to output a sign orientation bit, wherein the sign orientation bit comprises information indicative of whether the numerical value output comprises a positively-signed or negatively-signed numerical value.

14. The optical processing system of claim 13, wherein the logical gate comprises an XOR gate.

15. The optical processing system of claim 13, wherein the logical gate is configured to compare a sign of a value of an input vector element and a sign of a value of an input matrix element.

16. A method for implementing signed numerical values output by optical detectors of an optical processor, the method comprising:

converting, using an optical detector comprising a first terminal and a second terminal, an output optical signal into a first electrical signal, the output optical signal being output by a portion of the optical processor;

determining, using an at least one conventional processor coupled to the optical processor, whether the first electrical signal represents a positively-signed numerical value or a negatively-signed numerical value;

arranging, using control circuitry of the optical processor, settings of a first switch coupled to the first terminal and settings of a second switch coupled to the second terminal in response to determining whether the first electrical signal represents the positively-signed

numerical value or the negatively-signed numerical value, wherein the control circuitry is configured to:

produce a positively-signed numerical value output at least in part by setting the first switch to couple the first terminal to a reference voltage and setting the second switch to couple the second terminal to a node; and

produce a negatively-signed numerical value output at least in part by setting the first switch to couple the first terminal to the node and setting the second switch to couple the second terminal to a voltage rail; and

outputting, from the optical detector, the first electrical signal so that the first electrical signal passes through either the first switch or the second switch based on the determination of whether the first electrical signal represents a positively-signed numerical value or a negatively-signed numerical value.

17. The method of claim 16, wherein arranging settings of the first switch and the second switch comprises sending, from the control circuitry, one or more electrical signals to the first switch and the second switch, wherein the first switch and the second switch each comprise a transistor switch.

18. The method of claim 16, further comprising:

modulating an input optical signal using a first optical modulator to optically represent an element of a vector in a first optical signal;

modulating the first optical signal using a second optical modulator to optically represent a summand in the output optical signal, wherein the summand, when summed with other summands, represents a product between the vector and a matrix row; and

detecting the output optical signal using the optical detector.

19. The method of claim 16, wherein arranging settings of a first switch and settings of a second switch further comprises using a logical gate to generate a sign orientation bit, wherein the sign orientation bit comprises information indicative of whether the first electrical signal comprises a positively-signed or negatively-signed numerical value.

20. The method of claim 19, wherein using the logical gate comprises using an XOR gate.

~~21. An optical processor for implementing a matrix-vector multiplication operation, the optical processor comprising:~~

~~a first plurality of optical modulators, each configured to receive an input optical signal, modulate the input optical signal, and output a first optical signal representing an element of a vector;~~

~~a second plurality of optical modulators, each optically coupled to an optical modulator of the first plurality of optical modulators and configured to receive the first optical signal, modulate the first optical signal, and output a second optical signal representing a portion of a matrix-vector multiplication between the vector and a matrix;~~

~~a plurality of optical detectors each coupled to optical modulators of the second plurality of optical modulators and configured to convert the second optical signal into an electrical signal representing the portion of the matrix-vector multiplication; and~~

~~a plurality of switches configured to implement a value of zero in the matrix-vector multiplication operation by preventing transmission of an optical or electrical signal when a value of the vector and/or matrix comprises a zero, wherein a switch of the plurality of switches is coupled to an output of each of the first plurality of optical modulators or each of the plurality of optical detectors.~~

~~22. The optical processor of claim 21, wherein a switch of the plurality of switches comprises an electrical switch and is coupled to an output of one of the first plurality of optical detectors.~~

~~23. The optical processor of claim 22, wherein the switch is configured to prevent transmission of an electrical signal when a corresponding value of an element of the matrix is zero.~~

~~24. The optical processor of claim 21, wherein a switch of the plurality of switches comprises an optical switch and is coupled to an output of one of the second plurality of optical modulators.~~

~~25. The optical processor of claim 24, wherein the switch is configured to prevent transmission of an optical signal when a corresponding value of an element of the vector is zero.~~

~~26. The optical processor of claim 21, further comprising a plurality of electrical summing units, each coupled to an output of two or more optical detectors of the plurality of optical detectors and configured to output an electrical signal representing a sum of the portions of the matrix-vector operation output by the two or more optical detectors.~~

27. The optical processor of claim 26, further comprising another plurality of switches coupled to outputs of the plurality of electrical summing units, the switches of the another plurality of switches configured to prevent transmission of the electrical signal representing the sum when all values of elements of a row of the matrix are equal to zero.

28. A method of performing a matrix-vector row multiplication operation using an optical processor, the method comprising:

modulating an input optical signal using a first optical modulator to optically represent an element of a vector in a first optical signal;

modulating the first optical signal using second optical modulators to optically represent summands in a second plurality of optical signals, wherein the summands, when summed, represent a product between the element of the vector and a matrix row;

converting the second plurality of optical signals into a plurality of summand electrical signals using optical detectors; and

cause a switch coupled to an output of the first optical modulator to prevent transmission of the first optical signal to the second optical modulators when a value of the element of the vector is equal to zero and/or cause one or more switches coupled to outputs of the optical detectors to prevent transmission of the summand electrical signals when a value of one or more elements of the matrix row is equal to zero.

29. The method of claim 28, further comprising:

summing, using an electrical summing unit, the summand electricals signals to obtain a product electrical signal; and

outputting the product electrical signal.

30. The method of claim 29, further comprising:

causing a switch coupled to an output of the electrical summing unit to prevent transmission of the product electrical signal when values of all elements of the matrix row are equal to zero.

31. The method of claim 28, wherein causing the switch coupled to the first optical modulator to prevent transmission of the first optical signal to the second optical modulators when the value of the element of the vector is equal to zero comprises opening an optical switch.

32. The method of claim 28, wherein causing the one or more switches coupled to outputs of the optical detectors to prevent transmission of the summand electrical signals when the value of one or more elements of the matrix row is equal to zero comprises opening an electrical switch.

33. The method of claim 28, wherein modulating the input optical signal using the first optical modulator comprises modulating an amplitude of the input optical signal.

34. At least one non-transitory computer-readable medium comprising instructions, which, when executed by an at least one optical processor, cause the optical processor to perform a method of:

modulating an input optical signal using a first optical modulator to optically represent an element of a vector in a first optical signal;

modulating the first optical signal using second optical modulators to optically represent summands in a second plurality of optical signals, wherein the summands, when summed, represent a product between the vector and a matrix row;

converting the second plurality of optical signals into a plurality of summand electrical signals using optical detectors; and

cause a switch coupled to an output of the first optical modulator to prevent transmission of the first optical signal to the second optical modulators when a value of the element of the vector is equal to zero and/or cause one or more switches coupled to outputs of the optical detectors to prevent transmission of the summand electrical signals when a value of one or more elements of the matrix row is equal to zero.

35. The at least one non-transitory computer-readable medium of claim 34, wherein the method further comprises:

summing, using an electrical summing unit, the summand electricals signals to obtain a product electrical signal; and

outputting the product electrical signal.

36. The at least one non-transitory computer-readable medium of claim 35, wherein the method further comprises:

causing a switch coupled to an output of the electrical summing unit to prevent transmission of the product electrical signal when values of all elements of the matrix row are equal to zero.

37. The at least one non-transitory computer-readable medium of claim 34, wherein causing the switch coupled to the first optical modulator to prevent transmission of the first optical signal to the second optical modulators when the value of the element of the vector is equal to zero comprises opening an optical switch.

38. The at least one non-transitory computer-readable medium of claim 34, wherein causing the one or more switches coupled to outputs of the optical detectors to prevent transmission of the summand electrical signals when the value of one or more elements of the matrix row is equal to zero comprises opening an electrical switch.

39. The at least one non-transitory computer-readable medium of claim 34, wherein modulating the input optical signal using the first optical modulator comprises modulating an amplitude of the input optical signal.

40. A method of performing matrix-matrix operations using an optical processor, the method comprising:

programming a first matrix into a first optical sub-processor;

programming a second matrix into a second optical sub-processor, the second optical sub-processor comprising inputs that are coupled to outputs of the first optical sub-processor;

inputting, as optical signals, a plurality of one-hot vectors into the first optical sub-processor; and

outputting, from the second optical sub-processor, an output vector representing a portion of a multiplication of the first and second matrices.

41. The method of claim 40, further comprising:

outputting, from the first optical sub-processor, a plurality of electrical signals representing a multiplication between the one-hot vector and the first matrix.

42. The method of claim 41, further comprising:

receiving, at the second optical sub-processor, the plurality of electrical signals from the first optical sub-processor; and

modulating, using optical modulators of the second optical sub-processor, input optical signals using the plurality of electrical signals received from the first optical sub-processor.

43. The method of claim 41, further comprising:

after outputting the plurality of electrical signals representing a multiplication between the one-hot vector and the first matrix, amplifying the plurality of electrical signals using one or more amplifiers.

44. An optical processor configured to perform matrix-matrix operations, the optical processor comprising:

a first optical sub-processor configured to optically perform a matrix-vector multiplication of a one-hot vector and a first matrix to obtain a first vector; and

a second optical sub-processor configured to receive output signals from the first optical sub-processor and to optically perform a matrix-vector multiplication of the first vector and a second matrix.

45. An optical processor configured to perform matrix-matrix operations, the optical processor comprising:

a first optical sub-processor, comprising:

a first plurality of optical modulators, each configured to receive an input optical signal, modulate the input optical signal, and output a first optical signal representing an element of a one-hot vector;

a second plurality of optical modulators, each optically coupled to an optical modulator of the first plurality of optical modulators and configured to receive the first optical signal, modulate the first optical signal, and output a second optical signal representing a portion of a matrix-vector multiplication between the one-hot vector and a first matrix;

a first plurality of optical detectors, each coupled to an optical modulator of the second plurality of optical modulators and configured to convert the second optical signal into an electrical signal representing the portion of the matrix-vector multiplication; and

a first plurality of electrical summing units, each coupled to an output of two or more optical detectors of the first plurality of optical detectors and configured to output an electrical signal representing an element of a vector resulting from a summation of portions of the matrix-vector multiplication; and

a second optical sub-processor, comprising:

a third plurality of optical modulators, each receiving an output electrical signal from an electrical summing unit of the plurality of electrical summing units of the first optical sub-processor, and wherein each is configured to receive an input optical signal,

modulate the input optical signal according to the received output electrical signal, and output a third optical signal representing the element of the vector;

a fourth plurality of optical modulators, each optically coupled to an optical modulator of the third plurality of optical modulators and configured to receive the third optical signal representing an element of the vector, modulate the third optical signal, and output a fourth optical signal representing portion of a matrix-matrix multiplication between the first matrix and a second matrix;

a second plurality of optical detectors, each coupled to an optical modulator of the third plurality of optical modulators and configured to convert the third optical signal into an electrical signal representing a portion of the matrix-matrix multiplication; and

a second plurality of electrical summing units, each coupled to an output of two or more optical detectors of the second plurality of optical detectors and configured to output an electrical signal representing an element of a matrix resulting from a summation of portions of the matrix-matrix multiplication.