

# PATENT SPECIFICATION

1,014,735

DRAWINGS ATTACHED.

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## COMPLETE SPECIFICATION.

### Encapsulated PN Junction Semiconductor Device.

We, TEXAS INSTRUMENTS INCORPORATED, a corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to encapsulated semiconductor devices.

The present invention is an encapsulated P-N junction semiconductor device comprising a substrate having a substantially flat surface, a semiconductor wafer on said flat surface, said semiconductor wafer having a plurality of P-N junctions therein all of which are in the vicinity of one major wafer face and spaced from the opposite major wafer face, an enclosure including said substrate surrounding said semiconductor wafer, electrical connections exterior of said enclosure and extending into the interior of said enclosure to connect ohmically to various semiconductor zones of said semiconductor wafer, and said electrical connections including a plurality of spaced coplanar flat conductors on said substantially flat surface, a respective plurality of spaced coplanar elongated flat conductors, essentially the entire opposite major wafer face ohmically resting on one of said spaced coplanar flat conductors and wires ohmically connected between the semiconductor zones on said one major wafer face and the other ones of said spaced coplanar flat conductors.

The novel features believed characteristic of this invention are set forth in the appended claims. The invention itself, however, may best be understood from the following description of an illustrative embodiment,

when read in conjunction with the accompanying drawing, in which:

Figure 1 is the top view of the mounting frame and transistor assembly in an intermediate stage of fabrication;

Figure 2 is an enlarged pictorial view of the transistor assembly of Figure 1;

Figure 3 is a greatly enlarged pictorial view in section of the semiconductor wafer of Figure 1; and

Figure 4 is a pictorial view of the completed assembly.

With reference to Figure 1, a transistor is fabricated according to this invention by first assembling the component parts on a mounting ring 10. This mounting ring is merely used in fabrication to hold the parts together, and so the specific form is immaterial. The ring 10 will have three inwardly extending leads 11, 12 and 13 attached thereto by welding, for example, while the end of each of these leads will be bent downwardly as best seen in Figure 2. These leads may be composed of nickel clad on the top surface with about 1 mil thickness of silver. The dimensions of the leads are about  $3 \times 20$  mil in cross section. A semiconductor wafer 14, having appropriate regions and junctions therein to form a planar silicon transistor, has been previously secured to the end of the lead 12. The wafer 14 may be bonded to the lead 12 by placing the lead on a strip heater and bringing it up to a temperature of close to  $830^{\circ}\text{C}$ , the silver-silicon eutectic temperature, and then placing the wafer on the end of the lead. The lower, undiffused portion 15 of the wafer 14 forms the collector region of the transistor so that the lead 12 provides the collector contact. A pair of diffused regions 16 and 17 have been formed in the wafer, as seen in Figure 3, and a silicon oxide layer 18 covers the top surface

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to protect the exposed edges of the junctions. Emitter and base contacts 19 and 20 have been provided by evaporating a conductive material such as aluminium onto the surface of the silicon wafer in areas where the oxide layer 18 has been selectively removed by etching. Although a planar type structure is illustrated wherein the exposed junctions are protected by an oxide coating, it is of course understood that other configurations can be used, and that the junctions could be protected by a surface treatment other than an oxide coating.

As seen in Figure 1, a small wire 21 is attached at one end to the emitter contact 19 by a technique such as ball bonding and attached at the other end to the lead 11 by spot welding, for example. In a like manner a small wire 22 is connected between the base contact 20 and the lead 13, the latter forming the base contact. The wires 21 and 22 are preferably silver, platinum or palladium with a diameter of about 1 mil.

The ring 10 including the transistor components is placed around a glass can or shell 24 which has been previously formed by pressing, extruding, or other suitable means. The ends of the leads 11, 12 and 13, which have been bent downwardly, are now seen to extend down into the shell. Depressions or notches around the edges of the shell 24 may be provided to accommodate the leads 11, 12 and 13. The shell 24 is composed of a hard glass material which is selected to have a temperature expansion coefficient matched with that of the solder glass potting material which is subsequently introduced. For example, a potash soda lead glass which is commercially available under the trade designation "Corning Type 0120" may be used to form the shell 24. "Corning" is a registered Trade Mark. This glass has a thermal expansion coefficient of  $89 \times 10^{-7}/^{\circ}\text{C}$  and a softening point of  $630^{\circ}\text{C}$ .

The device is now encapsulated by filling the shell 24 with a slurry prepared from finely ground solder glass, a solvent and perhaps a binder. The glass material must have a relatively low melting point, less than that of the shell 24 and less than that which would damage the semiconductor wafer, and may be of the type generally known as solder glass. Solder glasses are various combinations of inorganic materials including  $\text{SiO}_2$ ,  $\text{PbO}$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{B}_2\text{O}_3$ ,  $\text{ZnO}$  and others. A material of this general type is commercially available under the trade designation of Corning Pyroceram, which incidentally, includes traces of a material such as gold to aid in crystal formation upon fusing. Specifically, a glass matched with that suggested above would be high lead glass. Corning Type 7570, which softens at  $440^{\circ}\text{C}$  and has a thermal expansion

coefficient of  $84 \times 10^{-7}/^{\circ}\text{C}$ . It is of course understood that any two types of glass could be used for the shell 24 and the casing, provided that the thermal expansion coefficients were matched with each other and that the softening points were adequately separated. The finely ground solder glass is mixed with a suitable amount of liquid solvent such as amylacetate to form a slurry of the proper viscosity so that the mixture will flow into the shell and surround the transistor wafer and leads. The solvent may also include a small amount of binder such as nitro-cellulose. The assembly is then allowed to stand in air for a time so that the solvent in the slurry may evaporate. The binder, if used, would aid in holding the powdered glass in place at this point. The powdered solder glass must then be fused to form a hard, impervious casing for the transistor device. If the solder glass has a softening point of about  $440^{\circ}\text{C}$ , as suggested above, then the device would be fired at a temperature of a few degrees above this point, or perhaps  $450^{\circ}$  to  $500^{\circ}\text{C}$ . During this firing, the nitrocellulose is burned out, if used, leaving only the glass. The time necessary to perform this firing step would vary, depending upon the materials used, but it has been found that about 30 minutes is adequate at  $450^{\circ}\text{C}$ .

The device is then removed from the ring 10 by clipping the leads 11, 12 and 13 at the positions indicated in Figure 1 by dotted lines. The completed transistor assembly will appear as in Figure 4, wherein the open side of the shell 24 is seen to be closed off by a casing 25 of hardened solder glass. The leads 11, 12 and 13 form the emitter, collector and base leads, respectively.

It should be emphasized that gold leads and contacts would not be very well adapted for use in the present transistor assemblies since gold and silicon form a eutectic at  $377^{\circ}\text{C}$ , well below the softening point of most solder glasses. The region wherein the gold-silicon eutectic formed might travel through the thin semiconductor wafer and destroy the junctions. Silver is well suited for use as the contact and lead material since a eutectic of silver and silicon forms at a relatively high temperature of  $830^{\circ}\text{C}$ . Likewise, platinum would be excellent lead material since a eutectic also forms between metallic compounds of platinum and silicon at  $830^{\circ}\text{C}$ . Palladium is also suitable for the leads since a eutectic of palladium and silicon compounds forms at  $720^{\circ}\text{C}$ .

It is, of course, understood that various configurations of the transistor assembly of this invention may be used in addition to the illustrative embodiment above. For

degrees



example, instead of a three element transistor device a multielement semiconductor network could be employed in place of the wafer 14. In this case, the number of leads or tabs utilized would correspond to the number of contacts necessary for the semiconductor device. Also, two transistors could be encapsulated in the same glass shell, in which case six tabs or leads would be arranged in a suitable configuration to extend into the shell and form base, emitter and collector contacts for both transistors. The shell could, of course, be of rectangular or any other suitable configuration.

The present Application was divided out from Patent Application No. 39642/62 (Serial No. 1,014,734).

#### WHAT WE CLAIM IS:—

1. An encapsulated P-N junction semiconductor device comprising a substrate having a substantially flat surface, a semiconductor wafer on said flat surface, said semiconductor wafer having a plurality of P-N junctions therein all of which are in the vicinity of one major wafer face and spaced from the opposite major wafer face, an enclosure including said substrate surrounding said semiconductor wafer, electrical connections exterior of said enclosure and extending into the interior of said en-

closure to connect ohmically to various semiconductor zones of said semiconductor wafer, and said electrical connections including a plurality of spaced coplanar flat conductors on said substantially flat surface, a respective plurality of spaced coplanar elongated flat conductors, essentially the entire opposite major wafer face ohmically resting on one of said spaced coplanar flat conductors and wires ohmically connected between the semiconductor zones on said one major wafer face and the other ones of said spaced coplanar flat conductors.

2. A device according to claim 1, wherein said spaced coplanar elongated flat conductors are located in a different but substantially parallel plane with respect to the plane of said spaced coplanar flat conductors.

3. A device according to claim 1 or 2, wherein said one major wafer face is a plane surface and said P-N junctions terminate thereat.

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3

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