CLAIMS

1. A method of calibrating a component, the method comprising: receiving previous calibration parameters for an external component at a secondary SoC from a primary SoC, wherein the secondary SoC is coupled to the external component and configured to calibrate the external component; determining validity of the previous calibration parameters by the secondary SoC; and operating the external component by the secondary SoC based on the determined validity of the previous calibration parameters.

2. The method of claim 1, further comprising: controlling boot of the secondary SoC by the primary SoC; determining new calibration parameters for the external component by the secondary SoC based on determining the previous calibration parameters are invalid; transmitting the new calibration parameters from the secondary SoC to the primary SoC; and operating the external component using the new calibration parameters.

3. The method of claim 2, wherein the previous calibration parameters are determined based on previous one or more datasets for determining calibration parameters, and further comprising receiving one or more new datasets for determining calibration parameters as an update to the previous one or more datasets for determining calibration parameters, wherein the new calibration parameters are determined based on the one or more new datasets for determining calibration parameters.

4. The method of claim 3, wherein the one or more new datasets comprise one or more of a frequency matrix, a voltage configuration, a training algorithm, or double data rate dynamic random access memory parameters.

5. The method of claim 2, wherein the previous calibration parameters comprise dummy data.

6. The method of claim 2, further comprising storing the new calibration parameters in a storage of the primary SoC.

7. The method of claim 6, wherein the secondary SoC does not directly interface with any storage that is configured to store the new calibration parameters or the previous calibration parameters.

8. The method of claim 1, further comprising: receiving a previous checksum corresponding to the previous calibration parameters at the secondary SoC from the primary SoC; and calculating a new checksum at the secondary SoC based on previous calibration parameters, at least one of one or more datasets for determining calibration parameters by the secondary SoC, and an identifier of the secondary SoC, wherein determining the validity of the previous calibration parameters comprises comparing the previous checksum to the new checksum.

9. The method of claim 1, further comprising: receiving a previous authentication tag corresponding to the previous calibration parameters at the secondary SoC from the primary SoC; and calculating, based on an authentication algorithm, a new authentication tag at the secondary SoC based on previous calibration parameters, at least one of one or more datasets for determining calibration parameters by the secondary SoC, and a key based on an identifier of the secondary SoC, wherein the key is calculated by the secondary SoC and unavailable to the primary SoC, wherein the authentication algorithm is unavailable to the primary SoC, and wherein determining the validity of the previous calibration parameters comprises comparing the previous authentication tag to the new authentication tag.

10. The method of claim 1, wherein the external component is one of stacked with the secondary SoC, configured as a package on package design with the secondary SoC, or on a different package than the secondary SoC.

11. The method of claim 1, wherein receiving the previous calibration parameters is performed over a transport layer.

12. The method of claim 1, further comprising operating the external component using the previous calibration parameters based on determining the previous calibration parameters are valid.

13. The method of claim 1, wherein the external component comprises an external memory.

14. A circuit comprising: a primary SoC comprising: a first bus; a first processor coupled to the first bus; a storage controller coupled to the first bus; and a first chip to chip interface coupled to the first bus; a secondary SoC comprising: a second bus; a second processor coupled to the second bus; a component interface coupled to the second bus, wherein the component interface is configured to interface with an external component; and a second chip to chip interface coupled to the second bus, wherein the second chip to chip interface is configured to interface with the first chip to chip interface to provide communication between the primary SoC and the

secondary SoC; wherein the second processor is configured to: receive previous calibration parameters for the external component from the first processor, wherein the first processor is configured to retrieve the previous calibration parameters from a storage coupled to the storage controller; determine validity of the previous calibration parameters; and operate the external component based on the determined validity of the previous calibration parameters.

15. The circuit of claim 14, wherein the primary SoC is configured to control boot of the secondary SoC, wherein the secondary SoC is configured to determine new calibration parameters for the external component based on determining the previous calibration parameters are invalid, wherein the secondary SoC is configured to transmit the new calibration parameters to the primary SoC, and wherein the secondary SoC is configured to operate the external component using the new calibration parameters.

16. The circuit of claim 15, wherein the previous calibration parameters are determined based on previous one or more datasets for determining calibration parameters, and wherein the secondary SoC is further configured to receive one or more new datasets for determining calibration parameters as an update to the previous one or more datasets for determining calibration parameters, wherein the new calibration parameters are determined based on the one or more new datasets for determining calibration parameters.

17. The circuit of claim 16, wherein the one or more new datasets comprise one or more of a frequency matrix, a voltage configuration, a training algorithm, or double data rate dynamic random access memory parameters.

18. The circuit of claim 15, wherein the previous calibration parameters comprise dummy data.

19. The circuit of claim 15, wherein the primary SoC is further configured to store the new calibration parameters in a storage of the primary SoC.

20. The circuit of claim 19, wherein the secondary SoC does not directly interface with any storage that is configured to store the new calibration parameters or the previous calibration parameters.

21. The circuit of claim 14, wherein the secondary SoC is further configured to: receive a previous checksum corresponding to the previous calibration parameters from the primary SoC; and calculate a new checksum based on previous calibration parameters, at least one of one or

more datasets for determining calibration parameters by the secondary SoC, and an identifier of the secondary SoC, wherein determining the validity of the previous calibration parameters comprises comparing the previous checksum to the new checksum.

22. The circuit of claim 14, wherein the secondary SoC is further configured to: receive a previous authentication tag corresponding to the previous calibration parameters from the primary SoC; and calculate, based on an authentication algorithm, a new authentication tag based on previous calibration parameters, at least one of one or more datasets for determining calibration parameters by the secondary SoC, and a key based on an identifier of the secondary SoC, wherein the key is calculated by the secondary SoC and unavailable to the primary SoC, wherein the authentication algorithm is unavailable to the primary SoC, and wherein determining the validity of the previous calibration parameters comprises comparing the previous authentication tag to the new authentication tag.

23. The circuit of claim 14, wherein the external component is one of stacked with the secondary SoC, configured as a package on package design with the secondary SoC, or on a different package than the secondary SoC.

24. The circuit of claim 14, wherein receiving the previous calibration parameters is performed over a transport layer.

25. The circuit of claim 14, wherein the secondary SoC is configured to operate the external component using the previous calibration parameters based on determining the previous calibration parameters are valid.

26. The circuit of claim 14, wherein the external component comprises an external memory.

27. A circuit comprising: means for receiving previous calibration parameters for an external component at a secondary SoC from a primary SoC, wherein the secondary SoC is coupled to the external component and configured to calibrate the external component; means for determining validity of the previous calibration parameters by the secondary SoC; and means for operating the external component by the secondary SoC based on the determined validity of the previous calibration parameters.

28. The circuit of claim 27, further comprising: means for controlling boot of the secondary SoC by the primary SoC; means for determining new calibration parameters for the external

component by the secondary SoC based on determining the previous calibration parameters are invalid; means for transmitting the new calibration parameters from the secondary SoC to the primary SoC; and means for operating the external component using the new calibration parameters.

29. A non-transitory computer readable medium having instructions stored thereon for causing a circuit to perform a method of calibrating a component, the method comprising: receiving previous calibration parameters for an external component at a secondary SoC from a primary SoC, wherein the secondary SoC is coupled to the external component and configured to calibrate the external component; determining validity of the previous calibration parameters by the secondary SoC; and operating the external component by the secondary SoC based on the determined validity of the previous calibration parameters.

30. The non-transitory computer readable medium of claim 29, wherein the method further comprises: controlling boot of the secondary SoC by the primary SoC; determining new calibration parameters for the external component by the secondary SoC based on determining the previous calibration parameters are invalid; transmitting the new calibration parameters from the secondary SoC to the primary SoC; and operating the external component using the new calibration parameters.