

CLAIMS

What is claimed is:

1. A method of testing a semiconductor device, the method comprising:
contacting a pad of the semiconductor device with a plurality of probe needles, the plurality of probe needles comprising a plurality of first needles and at least one second needle;
supplying current through the plurality of first needles, wherein supplying current comprises regulating the current through the plurality of first needles to a predetermined relationship; and
measuring a voltage at the at least one second needle.
2. The method of claim 1, wherein:
regulating the current comprises, in a current splitter, generating a current supplied through each of the plurality of first needles.
3. The method of claim 2, wherein:
generating, in a current splitter, a current supplied through each of the plurality of first needles comprises generating a control voltage to each of a plurality of circuits.
- ~~4. The method of claim 2, wherein:
generating a current supplied through each of the plurality of first needles comprises:
supplying a current through each of the plurality of needles in the range of 0 Amps to 7 Amps; and
supplying an aggregate current through the plurality of needles in the range of 40 Amps to 60 Amps.~~
45. The method of claim 1, further comprising:
computing an ON resistance of the semiconductor device based on the measured voltage.

56. A method of manufacturing a semiconductor device incorporating the method of testing a claim 5, the method of manufacturing comprising:

testing the semiconductor device according to the method of claim 1; and
selecting at least one subsequent step in the manufacturing based on the computed ON resistance.

67. The method of claim 1, further comprising:
sensing contact resistance between needles of the plurality of first needles and the semiconductor device; and
generating an alarm when a sensed contact resistance exceeds a threshold.

~~8. The method of claim 1, wherein:
the ON resistance is less than 5 milliOhm.~~

~~9. The method of claim 1, wherein:
the semiconductor device is a power FET.~~

710. The method of claim 1, wherein:
the at least one second needle comprises a plurality of second needles; and
a tip of each of the plurality of second needles is positioned adjacent a tip of a needle of the plurality of first needles.

811. The method of claim 710, wherein:
measuring voltage comprises measuring a composite voltage at a node to which the plurality of second needles are connected.

912. The method of claim 1, wherein:
the semiconductor device is a semiconductor device on a wafer;

the wafer is attached to a chuck; and

supplying current comprises inducing a current between the first needles and the chuck.

1013. The method of claim 1, wherein:

regulating the current further comprises, equalizing the current supplied through each of the plurality of first needles.

~~14. The method of claim 13, wherein:~~

~~equalizing the current further comprises, dividing the current to generate the current supplied through each of the plurality of first needles.~~

1145. The method of 1, further comprising:

sensing a total current flow, wherein the sensed total current flow is used to adjust control signals to a plurality of current regulators based on a sensed total current.

1246. A device interface board configured to connect to a test system for testing a high current device, the device interface board comprising:

a plurality connection points positioned to connect to a probe card, the plurality of connection points comprising a plurality of first connection points and at least one second connection point;

a current regulator, the current regulator comprising a plurality of outputs coupled to the plurality of first connection points, the current regulator configured to regulate current flow through each of the plurality of first connection points; and

a conducting path positioned to couple the at least one second connection point to a measurement point on a test system.

1347. The device interface board of claim 1246, further comprising:

alarm circuitry that outputs an alarm when a contact resistance of a probe needle coupled to a connection point of the plurality of first connection points exceeds a threshold.

1448. The device interface board of claim 1216, wherein:

the at least one second connection point comprises a plurality of second connection points; and

the device interface board comprises conductive elements connecting the plurality of second connection points.

~~19. — The device interface board of claim 16, wherein:~~

~~the current regulator is configured to regulate current through each of the plurality of first connection points with a tolerance of $\pm 1\%$.~~

~~20. — The device interface board of claim 19, wherein:~~

~~the current regulator is configured to regulate current through each of the plurality of first connection points within a range of 0 Amps to 7 Amps.~~

1524. The device interface board of claim 1216, further comprising:

a current control loop, wherein the control loop is configured to regulate the current proportionally through each of the plurality of first connection points in response to comparing a total current to an indication of a desired total current.

1622. A test system for testing a semiconductor device, the semiconductor device comprising a pad, the test system comprising:

a probe card comprising:

a plurality of needles comprising tips positioned to contact the pad, the plurality of needles comprising a plurality of first needles and at least one second needle;
at least one current regulator coupled to the plurality of first needles, the at least one current regulator configured to equalize current through the plurality of first needles; and
at least one voltage sense circuit coupled to the at least one second needle.

~~23. The test system of claim 22, further comprising:~~

~~a chuck; and~~

~~a processor coupled to receive a value indicative of voltage sensed by the at least one voltage sense circuit and to compute, based on the voltage sensed, an ON resistance of the semiconductor device, wherein the voltage is sensed between the pad and the chuck.~~

~~24. The test system of claim 23, wherein the chuck is configured to position a wafer comprising the semiconductor device in contact with the plurality of needles, wherein the chuck comprises a surface for receiving the wafer and the surface comprises gold plating.~~

~~25. The test system of claim 22, wherein the at least one current regulator is configured to generate an aggregate current through the plurality of first needles in excess of 10 Amps.~~

~~26. The test system of claim 25, wherein the at least one current regulator is configured to generate a current through each of the plurality of first needles that differs by less than +/- 2%.~~

~~1727.~~ The test system of claim ~~1622~~, wherein:

the first plurality of needles comprise force needles and the at least one second needle comprises a sense needle.

~~1828.~~ The test system of claim ~~1622~~, wherein:

the at least one second needle comprises a plurality of second needles; and

the plurality of second needles are connected to a single voltage sense circuit of the at least one voltage sense circuit.

~~1929.~~ The test system of claim ~~1622~~, wherein:

the plurality of first needles are positioned with tips that are equi-resistant from a nearest tip of a needle of the at least one second needle.