What is claimed is:

CLAIMS

1. A method for forming a semiconductor package comprising:

providing a wafer having first and second major surfaces, wherein the wafer is prepared with a plurality of dies and a plurality of external electrical contacts disposed on the first major surface of the wafer; and

processing the wafer, wherein processing the wafer comprises

performing a first singulation process which comprises a full cut to separate the wafer into the plurality of individual dies, wherein an individual die comprises first and second major surfaces and first and second sidewalls, and the external electrical contacts are formed on the first major surface of the die, and wherein the individual dies are provided on a support unit and adjacent individual dies are separated by a gap on the support unit,

expanding the support unit along radius of the support unit to increase the gap between adjacent individual dies prior to forming an encapsulant material, wherein the gap is increased to a predetermined distance which is sufficiently wide to accommodate at least an encapsulant material, and wherein the individual dies with increased gap distance are processed together in a wafer format on the support unit, and

forming an encapsulant material, wherein the encapsulant material covers at least a portion of the first and second sidewalls of the die.

2. The method of claim 1 wherein:

forming the encapsulant material comprises providing encapsulant material which at least fills and covers the gap between adjacent dies; and

processing the wafer further comprises performing a second singulation process through the encapsulant material which fills the gaps such that the encapsulant material covers at least a portion of the first and second sidewalls of the die.

3. The method of claim 2 wherein processing the wafer comprises forming a backside protective layer, wherein the backside protective layer is formed over the second major surface of the dies.

4. The method of claim 2 wherein processing the wafer comprises:

providing a temporary support having top and bottom surfaces;

providing an adhesive layer over the top surface of the temporary support; and

attaching the individual dies to the adhesive layer, wherein the external electrical contacts are at least partially embedded in the adhesive layer.

5. The method of claim 4 wherein processing the wafer comprises removing at least a portion of the encapsulant material over the second major surface of the dies.

6. The method of claim 2 wherein forming the encapsulant material comprises:

providing a stencil over the first surface of the dies, wherein the stencil covers the first major surface of the dies and comprises openings which expose the gap between adjacent dies; and

the encapsulant material is provided by dispensing the encapsulant material to fill and cover the gap.

7. The method of claim 1 wherein forming the encapsulant material comprises jetting or spraying the encapsulant along edges of the dies, wherein the encapsulant material conforms to sidewalls of the dies.

8. The method of claim 1 wherein processing the wafer comprises:

providing an encapsulant layer over one of the first or second major surface of the wafer;

performing the first singulation process after providing the encapsulant layer to separate the wafer into the plurality of individual dies having the encapsulant layer over one of the first or second major surface of the dies; and

performing a treatment process to transform the encapsulant layer into liquid phase to form the encapsulant material which covers at least a portion of the first and second sidewalls of the die and the first or second major surface of the die, wherein the encapsulant material comprises non-uniform thickness at least across the first or second major surface of the die, and wherein the encapsulant material over the first or second major surface of the die comprises a convex profile.

9. A method for forming a semiconductor package comprising:

providing a wafer having first and second major surfaces, wherein the wafer is prepared with a plurality of dies and a plurality of external electrical contacts disposed on the first major surface of the wafer; and

processing the wafer, wherein processing the wafer comprises

providing at least a first encapsulant layer having an encapsulant material which covers at least the first major surface of the wafer and partially covers the external electrical contacts,

performing a first singulation process after providing the first encapsulant layer to separate the wafer into the plurality of individual dies, wherein an individual die comprises first and second major surfaces and first and second sidewalls, and the external electrical contacts are formed on the first major surface of the die, and wherein the plurality of individual dies have the first encapsulant layer at least over the first major surface of the dies, wherein adjacent dies are separated by a gap, and

performing a second singulation process through the gap such that the encapsulant material is formed to cover at least a portion of the first and second sidewalls of the die.

10. The method of claim 9 wherein processing the wafer comprises:

performing a treatment process to transform the first encapsulant layer into liquid phase to at least fills the gaps between adjacent dies.

11. The method of claim 9 wherein processing the wafer comprises:

forming grooves through first major surface of the wafer, wherein the grooves extend from the first major surface of the wafer and partially into the wafer; and wherein

the first and second sidewalls of the dies comprise a step profile after performing the first singulation process.

12. The method of claim 11 wherein processing the wafer comprises:

providing a second encapsulant layer which covers the first encapsulant layer and fills gaps between adjacent dies; and wherein

the second singulation process is performed after providing the second encapsulant layer such that the encapsulant material is formed by the first and second encapsulant layers which cover at least a portion of the first and second sidewalls of the die.

13. A method for forming a semiconductor package comprising:

providing a semiconductor die, wherein the die comprises first and second major surfaces and first and second sidewalls, and external electrical contacts formed on the first major surface of the die;

forming an encapsulant material, wherein the encapsulant material covers and in direct contact with the first and second sidewalls of the die without covering and without contacting the external electrical contacts of the die; wherein the first and second sidewalls include vertical sidewall profile and the encapsulant material fully covers the first and second sidewalls of the die; and wherein the encapsulant material is a single encapsulant layer that fully covers the first and second sidewalls and the second major surface of the die.

14. The method of claim 13, wherein the single encapsulant layer comprises non-uniform thickness at least across the second major surface of the die, wherein the encapsulant material over the second major surface of the die comprises a convex profile.

15. The method of claim 13 comprising forming a backside protective layer over the second major surface of the die, wherein the encapsulant material also covers side surfaces of the backside protective layer.

16. The method of claim 13 comprising forming a backside protective layer over the second major surface of the die, wherein the backside protective layer also covers surfaces of the encapsulant material which are substantially coplanar with the second major surface of the die.

17. The method of claim 13 wherein the encapsulant material which fully covers the first and second sidewalls of the die comprises a substantially arc shape profile nearer to the external electrical contacts.

18. The method of claim 13 wherein the encapsulant material comprises a vertical portion and first and second lateral extended portions, wherein the vertical portion is disposed over the sidewall of the die, the first lateral extended portion extends to peripheral portion of the die towards the external electrical contacts and the second lateral extended portion extends outward and away from the die and has a top surface which is substantially coplanar with the second major surface of the die.

19. The method of claim 18 wherein forming the encapsulant material comprises jetting or spraying the encapsulant material along edges of the die, wherein the encapsulant material conforms to sidewalls of the die.

20. The method of claim 13 wherein the first and second sidewalls include a step profile and the encapsulant material covers only portion of the first and second sidewalls of the die.

21. The method of claim 13 comprising:

providing a wafer having first and second major surfaces, wherein the wafer is prepared with a plurality of semiconductor dies and a plurality of external electrical contacts disposed on the first major surface of the wafer; and

processing the wafer to provide the semiconductor die, wherein processing the wafer comprises

performing a first singulation process which comprises a full cut to separate the wafer into the plurality of individual semiconductor dies, wherein adjacent semiconductor dies are separated by a gap, and

providing an encapsulant layer which covers the external electrical contacts and the first surface of the semiconductor dies and fills gaps between adjacent dies, and

patterning the encapsulant layer to form the encapsulant material such that the encapsulant material covers and in direct contact with at least a portion of the first and second sidewalls of the semiconductor die without covering and without contacting at least the first major surface of the semiconductor die.

22. The method of claim 13 comprising:

providing a wafer having first and second major surfaces, wherein the wafer is prepared with a plurality of semiconductor dies and a plurality of external electrical contacts disposed on the first major surface of the wafer; and

processing the wafer to provide the semiconductor die, wherein processing the wafer comprises

forming first type grooves through the first major surface of the wafer, wherein the first type grooves extend from the first major surface of the wafer and partially into the wafer having a first depth,

providing an encapsulant layer which covers the external electrical contacts and the first major surface of the dies and fills the first type grooves, and

patterning the encapsulant layer to form the encapsulant material such that the encapsulant material covers and in direct contact with at least a portion of the first and

second sidewalls of the semiconductor die without covering and without contacting at least the first major surface of the semiconductor die, and

performing a first singulation process which comprises a full cut to separate the wafer to provide the semiconductor die, wherein the first and second sidewalls of the semiconductor die comprise a step profile after performing the first singulation process.

23. A method for forming a semiconductor package comprising:

providing at least one semiconductor die, wherein the die comprises first and second major surfaces and first and second sidewalls, and external electrical contacts formed on the first major surface of the die;

providing a support structure, wherein the support structure comprises at least one recess defined in the support structure, wherein the recess is sufficiently large to accommodate the semiconductor die;

placing the at least one semiconductor die into the at least one recess;

forming an encapsulant material, wherein forming the encapsulant material comprises filling the at least one recess of the support structure with the encapsulant material, wherein the encapsulant material covers and in direct contact with at least a portion of the first and second sidewalls of the semiconductor die; and wherein the at least one recess of the support structure is filled with the encapsulant material prior to placing the at least one semiconductor die into the at least one recess.

24. A method for forming a semiconductor package comprising:

providing at least one semiconductor die, wherein the die comprises first and second major surfaces and first and second sidewalls, and external electrical contacts formed on the first major surface of the die; and

forming an encapsulant material which covers at least a portion of the first and second sidewalls of the die, wherein the encapsulant material comprises

a first encapsulant material that covers and in direct contact with at least the first major surface of the die, and

a second encapsulant material that covers and in direct contact with at least the first encapsulant material, wherein total thickness of the first and second encapsulant materials over the first major surface of the die is less than height of the external electrical contacts.

25. The method of claim 24 wherein the second encapsulant material fully covers and in direct contact with the first and second sidewalls of the die.

26. The method of claim 24 wherein the first encapsulant material fully covers and in direct contact with the first and second sidewalls of the die and wherein the second encapsulant material fully covers and in direct contact with portion of the first encapsulant material that is in direct contact with the first and second sidewalls of the die.

27. The method of claim 24 wherein the first and second sidewalls of the dies comprise a step profile.

28. The method of claim 24 comprising:

providing a wafer having first and second major surfaces, wherein the wafer is prepared with a plurality of semiconductor dies and a plurality of external electrical contacts disposed on the first major surface of the wafer; and

processing the wafer to provide the at least one semiconductor die, wherein processing the wafer comprises

forming grooves through the first major surface of the wafer, wherein the grooves extend from the first major surface of the wafer and partially into the wafer,

providing a first encapsulant layer over the first major surface of the wafer,

providing a second encapsulant layer which covers the first encapsulant layer and fills the grooves, and

performing a first singulation process which comprises a full cut to separate the wafer to provide the at least one semiconductor die.

29. The method of claim 24 comprising:

providing a wafer having first and second major surfaces, wherein the wafer is prepared with a plurality of semiconductor dies and a plurality of external electrical contacts disposed on the first major surface of the wafer; and

processing the wafer to provide the at least one semiconductor die, wherein processing the wafer comprises

forming grooves through the first major surface of the wafer, wherein the grooves extend from the first major surface of the wafer and partially into the wafer,

providing a first encapsulant layer over the first major surface of the wafer, and

performing a first singulation process which comprises a full cut to separate the wafer to provide the at least one semiconductor die.

30. A method for forming a semiconductor package comprising:

providing a wafer having first and second major surfaces, wherein the wafer is prepared with a plurality of dies and a plurality of external electrical contacts disposed on the first major surface of the wafer; and

processing the wafer, wherein processing the wafer comprises

forming first type grooves through the first major surface of the wafer wherein the first type grooves extend from the first major surface of the wafer and partially into the wafer having a first depth,

providing an encapsulant material which covers at least the first major surface of the wafer and at least partially covers the external electrical contacts and fills the first type grooves,

removing a portion of the wafer from the second major surface of the wafer,

performing a singulation process after removing a portion of the wafer, wherein the singulation process comprises a full cut to separate the wafer into the plurality of individual dies, wherein an individual die comprises first and second major surfaces and first and second sidewalls with a step profile, and wherein the encapsulant material covers and in direct contact with only the first major surface of the die and portion of the first and second sidewalls of the die above the step of the step profile while the second major surface of the die is devoid of encapsulant material.

31. The method of claim 30 wherein processing the wafer comprises:

forming second type grooves through the first type grooves filled with the encapsulant material, wherein the second type grooves comprise a second depth deeper than the first depth of the first type grooves with reference to the first major surface of the wafer; and wherein

removing a portion of the wafer from the second major surface of the wafer is performed after forming the second type grooves.