FLEXIBLE ARCHITECTURE AND INSTRUCTION FOR ADVANCED ENCRYPTION STANDARD (AES)

FIELD

This disclosure relates to cryptographic algorithms and in particular to the advanced encryption standard (AES) algorithm.

BACKGROUND

Cryptology is a tool that relies on an algorithm and a key to protect information. The algorithm is a complex mathematical algorithm and the key is a string of bits. There are two basic types of cryptology systems: secret key systems and public key systems. A secret key system also referred to as a symmetric system has a single key ("secret key") that is shared by two or more parties. The single key is used to both encrypt and decrypt information.

The Advanced Encryption Standard (AES), published by the National Institute of Standards and Technology (NIST) as Federal Information Processing Standard (FIPS) 197 is a secret key system. AES is a symmetric block cipher that can encrypt and decrypt information.

Encryption (cipher) performs a series of transformations using the secret key (cipher key) to transforms intelligible data referred to as "plaintext" into an unintelligible form referred to as "cipher text". The transformations in the cipher include: (1) Adding a round key (value derived from the cipher key) to the state (a two dimensional array of bytes) using a Exclusive OR (XOR) operation; (2) Processing the state using a non-linear byte substitution table (S-Box) (3) Cyclically shifting the last three rows of the state by different offsets; and (4) Taking all of the columns of the state and mixing their data (independently of one another) to produce new columns.

Decryption (inverse cipher) performs a series of transformations using the cipher key to transform the "cipher text" blocks into "plaintext" blocks of the same size. The transformations in the inverse cipher are the inverse of the transformations in the cipher.

The Rijindael algorithm is specified in the AES standard to process data blocks of 128 bits, using cipher keys with lengths of 128, 192 and 256 bits. The different key lengths are typically referred to as AES-128, AES-192 and AES-256.

The AES algorithm transforms the plaintext into cipher text or cipher text into plaintext in 10, 12, or 14 consecutive rounds, with the number of rounds dependent on the length of the key.

BRIEF DESCRIPTION OF THE DRAWINGS

Features of embodiments of the claimed subject matter will become apparent as the following detailed description proceeds, and upon reference to the drawings, in which like numerals depict like parts, and in which:

Fig. 1 is a block diagram of a system that includes an embodiment of a flexible architecture and instruction for performing AES encryption and decryption in a general purpose processor according to the principles of the present invention;

Fig. 2 is a block diagram of an embodiment of the processor shown in Fig. 1;

Fig. 3 is a block diagram that includes an embodiment of the execution unit shown in Fig. 2 for performing AES encryption and decryption according to the principles of the present invention;

Fig. 4 is a flow graph illustrating the flow of an aes encrypt round instruction through the execution unit shown in Fig. 3;

Fig. 5 is a flow graph illustrating the flow of an aes encrypt last round instruction through the execution unit shown in Fig. 3;

Fig. 6 is a flow graph illustrating the flow of an aes decrypt round instruction through the execution unit shown in Fig. 3;

Fig. 7 is a flow graph illustrating the flow of an aes decrypt last round instruction through the execution unit shown in Fig. 3; and

Fig. 8 illustrates an embodiment of an aes round instruction with immediate byte that may be used to generate round keys and perform encryption and decryption.

Although the following Detailed Description will proceed with reference being made to illustrative embodiments of the claimed subject matter, many alternatives, modifications, and variations thereof will be apparent to those skilled in the art. Accordingly, it is intended that the claimed subject matter be viewed broadly, and be defined only as set forth in the accompanying claims.

DETAILED DESCRIPTION

The Advanced Encryption Standard (AES) algorithm is a compute intensive algorithm that is typically performed in software or in a special purpose processor. Thus, encryption is typically only used for encrypting a subset of the information stored in computers, for example, information that may be classified as "top secret". However, there is a need to encrypt more of the information that is stored on computers. For example, if all information stored on a mobile computer was encrypted, this information would be protected in the event that the mobile computer was stolen.

AES is a block cipher that operates on a 128-bit block of bits with a key size of 128, 192 or 256 bits. A sequence of operations is iterated for a number of rounds (10, 12 or 14) based on the key size.

The generation of the keys for each round may be performed on the fly (that is, just prior to each round) using implicit 128-bit registers to store the round key. However, the use of implicit registers may reduce the performance of x86 register-based processors due to dependency on a result of a previous instruction.

There are some applications, for example, an application that processes network packets that may have different keys per flow that benefit from on-the-fly key generation. There may be other applications where greater performance is required with the single key, for example, a single key that is used for encrypting/decrypting contents of a disk drive. Thus, there arises a need for flexibility of key generation. An embodiment of the invention provides a flexible architecture and instruction for performing AES encryption and decryption in a general purpose processor.

Fig. 1 is a block diagram of a system 100 that includes an embodiment of a flexible architecture and instruction for performing AES encryption and decryption in a general purpose processor according to the principles of the present invention. The system 100 includes a processor 101, a Memory Controller Hub (MCH) or (Graphics Memory Controller Hub (GMCH)) 102 and an Input/Output (I/O) Controller Hub (ICH) 104. The MCH 102 includes a memory controller 106 that controls communication between the processor 101 and memory 108. The processor 101 and MCH 102 communicate over a system bus 116.

The processor 101 may be any one of a plurality of processors such as a single core Intel® Pentium IV ® processor, a single core Intel Celeron processor, an Intel® XScale processor or a multi-core processor such as Intel® Pentium D, Intel® Xeon® processor, or Intel® Core® Duo processor or any other type of processor.

The memory 108 may be Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Synchronized Dynamic Random Access Memory (SDRAM), Double Data Rate 2 (DDR2) RAM or Rambus Dynamic Random Access Memory (RDRAM) or any other type of memory.

The ICH 104 may be coupled to the MCH 102 using a high speed chip-to-chip interconnect 114 such as Direct Media Interface (DMI). DMI supports 2 Gigabit/second concurrent transfer rates via two unidirectional lanes.

The ICH 104 may include a storage I/O controller 110 for controlling communication with at least one storage device 112 coupled to the ICH 104. The storage device may be, for example, a disk drive, Digital Video Disk (DVD) drive, Compact Disk (CD) drive, Redundant Array of Independent Disks (RAID), tape drive or other storage device. The ICH 104 may communicate with the storage device 112 over a storage protocol interconnect 118 using a serial storage protocol such as, Serial Attached Small Computer System Interface (SAS) or Serial Advanced Technology Attachment (SATA).

The processor 101 includes an AES function 103 to perform aes encryption and decryption operations. The AES function 103 may be used to encrypt or decrypt information stored in memory 108 and/or stored in the storage device 112.

Fig. 2 is a block diagram of an embodiment of the processor 101 shown in Fig. 1. Processor 101 includes a fetch and decode unit 206 for decoding processor instructions received from Level 1 (L1) instruction cache 202. Data to be used for executing the instruction may be stored in register file 208. In one embodiment, the register file 208 includes a plurality of 128-bit registers, which are used by an aes instruction to store data for use by the aes instruction.

In one embodiment, the register file is a group of 128-bit registers similar to the 128-bit MMX registers provided in Intel Pentium MMX Processors that have a Streaming (Single Instruction Multiple Data (SIMD)) Extension (SSE) Instruction set. In a SIMD processor, data is processed in 128-bit blocks with one 128-bit block loaded at one time.

The fetch and decode unit 202 fetches macroinstructions from L1 instruction cache 202, decodes the macroinstructions and breaks them into simple operations called micro operations (μops) that may be stored in microcode Read Only Memory (ROM) 214. The execution unit 210 schedules and executes the micro operations. In the embodiment shown, the aes function 103 in the execution unit 210 includes micro operations for an aes instruction set. The retirement unit 212 writes the results of the executed instructions to

registers or memory. A round key 214 used by the aes instruction may be stored in L1 data cache 204 and loaded into the execution unit 210 for use by the micro operations to execute an aes instruction in the aes instruction set. Storing the round key 214 in the data cache 204 protects the round key from side channel attacks, for example, attempts to obtain the round key in order to get access to encrypted information stored in the system 100.

Fig. 3 is a block diagram that illustrates an embodiment of the execution unit 210 shown in Fig. 2 for performing AES encryption and decryption according to the principles of the present invention. Fig. 3 will be described in conjunction with Fig. 2.

After an aes instruction has been decoded by the fetch and decode unit 206, the execution of an aes instruction by the execution unit 210 involves performing the micro operations associated with the aes instruction that may be stored in the microcode ROM 214.

A flexible AES instruction set according to an embodiment of the present invention allows a programmer to make performance tradeoffs with respect to the amount of data to be processed, and memory bandwidth and capacity.

Some applications may continuously use the same key. In applications in which performance is very important, a tradeoff can be made in terms of pre-computing a key schedule for the key (that is, a round key per round) once and storing it in memory. Other applications may want to minimize the amount of memory used to store the key schedule while still achieving good performance on multi-block operations. For such applications the key schedule may be pre-computed for multiple blocks before being processed. The memory footprint may be further minimized by only storing the cipher key or the inverse cipher key, and then deriving the other as necessary at the expense of some performance.

In an x86 –type processor, the area and the number of execution ports that are available for AES round key operations and AES scheduling operations constrain the performance of an AES instruction. In a system in which key expansion is required for every block encryption, performance may be improved by placing the AES scheduling operations and the AES round key operations on separate execution ports. However, separate execution ports and the additional area for controlling the separate ports may not be available in an x86-type processor.

In an embodiment, an aes instruction set is provided that includes separate aes instructions for performing an encryption round, a decryption round, an encryption last

round, a decryption last round and for computing an encryption round key or a decryption round key. In one embodiment there are six aes instructions in the aes instruction set. Each aes round instruction has a unique operation code (opcode). The aes round instructions in the aes instruction set for one embodiment for a fixed width round key (for example, 128-bits) are shown below in Table 1.

AESENCRYPTRound xmmsrcdst xmm	
Input:	data (=destination), round key
Output:	data after transformation through the AES round using the round key
AESENCRYPTLastRound xmmsrcdst xmm	
Input:	data (=destination), round key
Output:	data after transformation through the AES last round using the round key
AESDECRYPTRound xmmsrcdst xmm	
Input:	data (=destination), round key
Output:	data after transformation through the AES round using the round key
AESDECRYPTLastRound xmmsrcdst xmm	
Input:	data (=destination), round key
Output:	data after transformation through the AES last round using the round key
AESNextRoundKey xmmsrc1,2 xmm dst (immediate)	
Input:	low 128 bits of key, high 128 bits of key, indicator for round number.
Output:	next round key derived from the input
AESPreviousRoundKey xmmsrc1,2 xmm dst (immediate)	
Input:	low 128 bits of key, high 128 bits of key, indicator for round number
Output:	previous round key derived from the input

Table 1

The aes instruction set includes four aes round instructions (encrypt, decrypt, encrypt last round, decrypt last round) and two aes round key instructions (next round key and previous round key). The aes round instructions in the aes instruction set include single round operations to perform encryption and decryption round operations that are to be used for all rounds but the last round. For example, in the AESENCRYPTRound single round instruction in Table 1, the input data is stored in a 128-bit register (xmmsrcdst) and the round key stored in another 128-bit register (xmm). This instruction performs an aes round operation on input data (source) that is stored in the 128-bit xmmsrcdst register and overwrites the input data stored in the 128-bit xmmsrcdst register with the result of the execution of the round operation. Thus xmmsrcdst first stores the input data and later stores the result of the aes round operation.

The aes instruction set also includes an aes decryption instruction for a last decryption round and an aes encryption instruction for a last encryption round. For example, in the 'AESENCRYPTLastRound single round instruction in Table 1, the input data is stored in a 128-bit register (xmmsrcdst) and the round key stored in another 128-bit register (xmm). This instruction performs an aes round operation on input data (source) that is stored in the xmmsrcdst register and overwrites the input data stored in the xmmsrcdst register with the result of the execution of the round operation. Thus xmmsrcdst first stores the input data and later stores the result of the round operation. The xmm register stores the round key for the round operation.

In another embodiment, the round and last round instructions, for example, 'AESENCRYPTRound and AESENCRYPTLastRound may take the input from memory (m/128) instead of from the register file 304, for example, the aes round instruction may be AESENCRYPTRound xmmsrcdst m/128.

The other two aes instructions in the aes instruction set generate a round key for an aes round dependent on the size of the key, that is, 128-bits, 192-bits or 256-bits. One of the aes round key instructions generates a round key for use in an encryption operation and the other aes round key instruction generates a round key for use in a decryption operation. The immediate field in the AESNextRoundKey and the AESPreviousRoundKey instructions specify the size of the key {128, 192, 256}.

In yet another embodiment, instead of an immediate field, the different key sizes may be implemented as separate instructions each having a unique operation code. In this embodiment, the number of aes round key instructions includes three separate instructions

for each round key operation, for example, AESNextRoundKey_128 AESNextRoundKey_192 and AESNextRoundKey_256 and there would be a similar set of three instructions for AESPreviousRoundKey. In this embodiment, the total number of instructions in the instruction set is 10 instead of 6 in the previously discussed embodiment.

The register file 304 has a plurality of 128-bit registers which may be used by the aes instructions in the aes instruction set. The 128-bit registers may store source operand(s), round keys and the result of the aes instruction. For the first round, the aes instruction receives a source operand that may be 128-bit of plaintext to be encrypted or 128-bits of cipher text to be decrypted. A key for generating a key schedule for a 128-bit, 192-bit or 256-bit key may be stored in any of the 128-bit registers 308 in the register file 304. The round keys may also be stored in any of the 128-bit registers 308 in the register file. All of the instructions use registers in the register file and may also take input directly from memory as discussed earlier.

An example of source code that uses an embodiment of the aes instruction set shown in Table 1 is shown in Table 2 below. In the example, performance is optimized in an application for performing encryption that uses the same key for many blocks. One such application is the use of a single key for encrypting contents of a disk in which the same key is used for encrypting all of the data prior to being stored on the disk. In the example, AES-128 encryption is performed.

The size of the key may be 128-bits, 192-bits or 256-bits. The number of rounds to be performed (n) may be 1, 10, 12 or 14 dependent on the size of the key with each round key being a fixed size (128-bits). With a number of rounds value of 10, 12, 14, the aes micro operations may perform standard aes encryption and decryption for key sizes of 128-bits, 192-bits or 256-bits.

When the same key is used for many blocks, the round key for each round (key schedule) may be pre-computed and stored in memory (for example, level 1 data cache 204) so that the same key schedule does not have to be recomputed prior to an encryption/decryption operation on each block.

RK[0] = Input Key

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For i = 1..10
  RK [i] = AESNextRoundKey (RK[i-1])
End

STATE = Input Block
STATE = STATE xor RK[0]

For i = 1..9
  STATE  = AESENCRYPTRound (STATE, RK[i])
End
STATE  = AESENCRYPTLastRound (STATE, RK[10])
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Table 2

An array (RK) having 10 elements is used to store the key schedule for the key. The input key for AES-128 encryption is stored in RK[0] and the 9 round keys RK[0] – RK[1] are pre-computed through a call to the AESNextRoundKey instruction from the aes instruction set. The AESNextRoundKey instruction computes the next round based on the current round key. The pre-computed round keys for the key schedule may be stored in round key 214 in level 1 data cache 204.

In this example, as the portion of the key schedule (expanded key), that is the round key for the round is input directly from the register file 304, an exclusive OR (XOR)operation is performed on the state and key prior to entering the loop for performing the aes rounds. For each round 1 through 9, the AESENCRYPTRound instruction from the aes instruction set is called to perform the aes round operation for one round. For the last round (round 10) the AESNECYRPTLastRound instruction from the aes instruction set is called to perform the aes round operation for the last round.

Information to be encrypted or decrypted by the aes instruction is loaded into a source/destination register 306 in the register file 304 prior to issuing the first aes instruction to start an encrypt or decrypt operation. The key to be used to encrypt/decrypt the information in the source register 306 is stored in one or more other registers 308 in the register file 308. In the case of a 128-bit key, the entire 128-bits of the key are stored in any one of the other 128-bit registers in the register file 304. For key sizes greater than 128 bits, the most significant bits (greater than 128 bits) are stored in another one of the 128-bit registers.

In the example shown in Table 2, the round key for each round is pre-computed based on the key and may be stored in level 1 data cache 204 prior to being loaded into any one of the registers 308 in the register file 304. The key for each round may also be stored in one or more registers in the register file 304 or may be stored in round key 214 in level 1 data cache 204.

AES has a fixed block size of 128 bits and a key size of 128, 192 or 256 bits and operates on a 4×4 array of bytes (that is, 16 bytes (128-bit fixed block size)), which is referred to as the 'state'. The AES algorithm transforms a 128-bit plaintext block into a 128-bit block of cipher text (encrypts) or a 128-bit block of cipher text into a 128-bit block of plaintext (decrypts) in 10, 12, or 14 consecutive rounds, with the number of rounds dependent on the key size (128, 192 or 256-bits).

Prior to performing the per round encryption or decryption operation, the execution unit 210 retrieves the state and the key which are stored in the register file 304. Each encryption/decryption round operation is performed using the micro operations for the aes instruction stored in the key scheduler 302 in the Read Only Memory (ROM) 214. In the embodiment shown, the state (128-bit block state) is stored in register 306 and the key is stored in one or more of the other registers 308 in the register file 304. After the execution of the aes instruction is complete, the resulting state is stored in register 306 in the register file 304. The state may be an intermediate round date to be used by a next aes round or the final result of the AES encryption or decryption operation.

In the embodiment shown, a key scheduler 302 generates the round key to be used in an aes round. The key scheduler 302 may be implemented as microcode operations and may include microcode operations to perform the sequence of operations for generating round keys for 128-bit, 196-bit and 256-bit keys as defined by FIPS Publication 197.

In another embodiment, the key scheduler may be implemented as a hardware state machine sequence in the execution unit 210. In yet another embodiment, some portion of the key scheduler may be implemented as microcode operations stored in the microcode ROM 214 and the remainder of the key scheduler may be implemented as a hardware state machine sequence in the execution unit 210.

The key scheduler 302 expands the n-bytes of a key into b-bytes of an expanded key (key schedule) with the first n-bytes of the expanded key being the original key. For example, for a 128-bit key, the 128-bit key is expanded into a 176-bytes expanded key, that is, 11 x 16-bytes (128-bits), with the first 16-bytes being the original 128-bit key, and thus the number of rounds is 10. The 24 bytes of a 192-bit key are expanded into 208 bytes (13 x 16 bytes) to provide 12 "round keys" one for each of the 12 rounds and the 32 bytes of a 256-bit key are expanded into 240 bytes (15 x 16 bytes) to provide 14 "round keys" one for each of the 14 rounds.

Upon decoding the operation code (opcode) in an aes instruction, a number of parameters to be used to control the flow in the aes instruction for one aes round are stored in control logic 322. The parameters include the type of operation (encryption or decryption) and whether it is a last round.

Aes round logic 324 may include micro operations for the following stages: block state 314, s-box/inverse S-box 316, shift rows 316 and mix inverse, mix columns or null (referred to as "mix columns") 320 and add round key 326.

In block state 314, the 128-bit input (state) to the aes round logic 324 is added with a key (128-bit portion of the expanded key associated with the round) using bitwise XOR to produce a 128-bit intermediate value (state).

In the S-box/inverse S-box 316, each byte of this 128-bit intermediate value is substituted with another byte value that may be stored and retrieved from a lookup table also referred to as a substitution box or "S-Box". The S-box takes some number of input bits, m, and transforms them into some number of output bits, n and is typically implemented as a lookup table. A fixed lookup table is typically used. This operation provides non-linearity through the use of the inverse function over Galois Field (GF)(2^8). For example, the n-bit output may be found by selecting a row in the lookup table using the outer two bits of the m-bit input, and selecting a column using the inner bits of the m-bit input.

In Shift Rows 318, the results from S-box/inverse S-box 316 passes through a bit-linear transform in which bytes in each row of the 4 x 4 array (128-bit (16 bytes) state) received from the Sub Bytes stage are shifted cyclically to the left. The number of places each byte is shifted differs for each row in the 4 x 4 array.

In Mix Columns 320, the results from Shift Rows 320 passes through a bit-linear transform in which each column of the 4 x 4 array (state) is treated as a polynomial over a binary Galois Field (GF)(2^8) and is then multiplied modulo $x^4 + 1$ with a fixed polynomial $c(x) = 3x^3 + x^2 + x + 2$. A last aes round differs from the other aes rounds in that it omits Mix Columns 320.

Add Round Key 324 after the Mix Columns stage 320 performs an exclusive OR function on the round key from the expanded key and the result of Shift Rows 318 or Mix Columns 320 for the aes round.

For example, the following aes instruction may be issued to perform one round of aes decryption:

AESDECRYPTRound xmmsrcdst xmm

This example performs a 128-bit AES encrypt round operation with a key whose expanded key is represented as {RK[1], RK[2], ... RK[10]}. The round key may be generated by issuing a AESPreviousRoundKey xmmsrc1, 2 xmm dst (immediate) instruction prior to issuing the AESDECRYPTRound instruction. The round key may be loaded directly into the block state 314 from Level 1 data cache 204 or may first be stored in a register (xmm) in the register file 304 and then loaded into the block state 314 from the register.

When a different key is used to encrypt/decrypt each block, for example, in the case of a network interface controller (NIC) that is encypting/decrypting data packets, the round key may computed on-the-fly prior to performing encryption/decryption for each round as shown in the pseudo code below in Table 3 for AES-128 encryption:

RK[0] = Input Key

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STATE = Input Block
STATE = STATE xor RK[0]

For i = 1..9
  RK [i] = AESNextRoundKey (RK[i-1])
  STATE  = AESENCRYPTRound (STATE, RK[i])
End
RK [10] = AESNextRoundKey (RK[9])
STATE  = AESENCRYPTLastRound (STATE, RK[10])
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Table 3

In this example, the round key for the round is generated prior to performing encryption using the round key for each of the 10 rounds in the key schedule (expanded key), that is, rounds 1-9 and round 10 (the last round).

The set of aes instructions that include single aes round instructions and single aes round key generation instructions allows variants of AES with different number of rounds and key schedules, that is, variants of AES not defined by FIPS Publication 197. Thus, the single round aes instructions in the aes instruction set provide flexibility in performing aes encryption and decryption.

As the number of rounds performed by the aes instruction set is not fixed, any numbers of rounds, if required, may be performed. For example, the number of rounds may be varied to support future encryption/decryption standards if new standards for hashing or MAC-ing attacks, or attacks on AES are introduced.

Fig. 4 is a flow graph illustrating the flow of an aes encrypt round instruction through the execution unit 210 shown in Fig. 3.

At block 400, the execution unit 210 waits for an aes encrypt round instruction. If an AES encrypt round instruction has been decoded by the fetch and decode unit 206, processing continues with block 402. If not, processing remains in block 400 waiting for an aes encrypt round instruction.

At block 402, during the instruction decode by the fetch and decode unit 206, an indication that encryption is to be performed is stored in the control logic 322 and the

round key and 128-bit block state (source) for use in performing the encryption round are loaded into the execution unit 210 from the register file 304. Processing continues with block 404.

At block 404, a substitution operation is performed on the 128-bit block state that is, the result from block 406 or 418. Each byte of the 128-bit block state is substituted with another byte value that can be stored and retrieved from a lookup table also referred to as a substitution box or "S-Box". The S-box takes some number of input bits, m, and transforms them into some number of output bits, n and is typically implemented as a lookup table. The result is stored as a 128-bit block state. Processing continues with block 406.

At block 406, the 128-bit block state (4 x 4 array) passes through a bit-linear transform in which bytes in each row of the 4 x 4 array are shifted cyclically to the left. The number of places each byte is shifted differs for each row in the 4 x 4 array. Processing continues with block 408.

At block 408, the 128-bit block state (4 x 4 array) passes through a bit-linear transform in which each column of the 4 x 4 array (state) is treated as a polynomial over $GF(2^8)$ and is then multiplied modulo $x^4 + 1$ with a fixed polynomial $c(x) = 3x^3 + x^2 + x + 2$. Processing continues with block 410.

At block 410, an exclusive OR function is performed on the round key from the expanded key and the result of Shift Rows 318 or Mix Columns 320 for the aes round. Processing continues with block 412.

At block 412, the result of the encryption operation for the round (128-bit block state) is stored in the source/destination register 302 in the register file 304. Processing for the aes encrypt instruction is complete.

Table 4 below shows an example of the result of performing AES-128 encryption using a 128-bit key on a 128-bit block input after execution of the pseudo code shown in Table 3.

128-bit Input:	00112233445566778899aabbccddeeff (Hexadecimal)
128-bit Key:	000102030405060708090a0b0c0d0e0f (Hexadecimal)
128-bit Result:	69c4e0d86a7b0430d8cdb78070b4c55a (Hexadecimal)

Table 4

Fig. 5 is a flow graph illustrating the flow of an aes encrypt last round instruction through the execution unit 210 shown in Fig. 3.

At block 500, the execution waits for an aes encrypt last round instruction. If an AES encrypt last round instruction has been decoded by the fetch and decode unit 206, processing continues with block 502. If not, processing remains in block 500 waiting for an aes instruction.

At block 502, an S-box lookup is performed for the last round in a similar manner to the S-box lookup discussed in conjunction with block 404 (Fig. 4). Processing continues with block 504.

At block 504, a shift rows operation is performed for the last round in a similar manner to that discussed in conjunction with the other rounds in block 406 (Fig. 4). Processing continues with block 506.

At block 506, an exclusive OR function is performed on the round key from the expanded key and the result of Shift Rows 318 or Mix Columns 320 for the aes round. Processing continues with block 508.

At block 508, the result of the encryption last round operation is stored in the source/destination register 306 in the register file 304. Processing for the aes instruction is complete.

Fig. 6 is a flow graph illustrating the flow of an aes decrypt round instruction through the execution unit 210 shown in Fig. 3.

At block 600, the execution waits for an aes decrypt round instruction. If an AES decrypt round instruction has been decoded by the fetch and decode unit 206, processing continues with block 602. If not, processing remains in block 600 waiting for an aes decrypt round instruction.

At block 602, during the instruction decode by the fetch and decode unit 206, an indication that a decrypt round is to be performed is stored in the control logic 322 and the round key and source (128-bit block state) for use in performing the decrypt round are loaded into the execution unit 210 from the register file 304. Processing continues with block 604.

At block 604, the operation to be performed is decryption. A substitution operation is performed on the 128-bit block state by performing an inverse s-box lookup as defined by the AES standard. Processing continues with block 606.

At block 606, an inverse shift rows operation is performed as defined by FIPS publication 197. Processing continues with block 608.

At block 608, an inverse shift rows operation is performed as defined by FIPS publication 197. Processing continues with block 610.

At block 610, an exclusive OR function is performed on the round key from the expanded key and the result of Shift Rows 318 or Mix Columns 320 for the aes round. Processing continues with block 612.

At block 612, the result of the decryption operation for the round (128-bit block state) is stored in the source/destination register 302 in the register file 304. Processing for the aes decrypt round instruction is complete.

Fig. 7 is a flow graph illustrating the flow of an aes decrypt last round instruction through the execution unit 210 shown in Fig. 3.

At block 700, the execution unit 210 waits for an aes decrypt last round instruction. If an AES decrypt last round instruction has been decoded by the fetch and decode unit 206, processing continues with block 702. If not, processing remains in block 700 waiting for an aes decrypt last round instruction.

At block 702, a substitution operation is performed on the 128-bit block state for the last round by performing an inverse s-box lookup as defined by FIPS publication 197. Processing continues with block 704.

At block 704, an inverse shift rows operation is performed for the last round as defined by FIPS publication 197. Processing continues with block 706.

At block 706, an exclusive OR function is performed on the round key from the expanded key and the result of Shift Rows 318 or Mix Columns 320 for the aes round. Processing continues with block 708.

At block 708, the result of the decrypt last round operation is stored in the source/destination register 306 in the register file 304. Processing for the aes decrypt last round instruction is complete.

In one embodiment, the blocks in the flowgraphs of Figs 4-7 may be implemented as a hardware state machine sequence in the execution unit 210. In another embodiment portions of the blocks may be implemented as a micro-program that may be stored in Read Only Memory (ROM) 214. The embodiment in which the blocks are implemented as a hardware state machine sequence may provide higher performance.

Fig. 8 illustrates an embodiment of an aes round instruction with immediate byte that may be used to generate round keys and perform encryption and decryption. Instead of the aes instruction set shown in Table 1, a single aes round instruction is provided to perform the functions of the aes instruction set. The particular function to be performed by the single aes instruction is encoded in bits in the immediate byte (key_select_modifier). The immediate byte allows the aes round instruction to be expanded to add new features instead of creating a plurality of new instructions with each instruction having a unique operation code.

The aes round instruction may be defined symbolically as follows:

dest := aes_key_round (source2, source1), key_select_modifier

The aes_key_round instruction is issued to a particular execution unit 210 based on port number in order to perform an AES encrypt or decrypt operation. In the embodiment shown, port number 4 is the designated execution port for the AES round instruction. The execution unit 210 is divided into many parallel ports (super-scalar). However, not all ports are equal. Some ports have specialized resources such as a large integer multiplier, or floating-point multiplier or divider. Simpler and more common instructions such as addition, subtraction and exclusive OR are supported on multiple ports for maximum performance. Thus for each instruction or micro-operation, issue control logic determines the port to which to issue the micro-operation/instruction. In this embodiment, the aes instruction is always issued to port number 4. However, in other embodiments other port numbers may be used.

Referring to Fig. 8, the dest stores 128 bits of expanded key for round N, source2 stores 128 bits of expanded key for round N-1, and source1 stores 128 bits of expanded key for round N-2. The key_select_modifier is an 8-bit immediate value used to provide current round number (N), direction of operation (encrypt/ decrypt) and AES key size. For AES-128, source1 is not needed and is ignored. The execution unit is AES unit and no flags (integer or floating point) are used.

In one embodiment, the bit encoding of the four least significant bits of the immediate value indicate the round number, for example, a round number from 1 – 10 for AES-128, a round number from 1 – 12 for AES-192 and a round number from 2 -14 for AES 256. For AES-128 and 192 round number 0 is not valid because the first round uses

the unmodified input key. For AES-256 round numbers 0 and 1 are not valid as the unmodified 256-bit input key is used for the first 2 128-bit rounds.

Bit 4 of the immediate byte indicates the direction of operation (encryption or decryption), for example, in one embodiment 0=encrypt, and 1=decrypt and in another embodiment 1=encrypt, and 0=decrypt. Bits 5 and 6 of the immediate byte indicate the AES key size. In one embodiment the AES key size is defined as shown in Table 5 below:

Bits[6:5]	Key Size
00	128
01	192
10	256
11	Reserved

Table 5

In another embodiment, bits [6:5] having a value of 11 is also an indicator for a 128-bit key size. In this embodiment, all values of bits [6:5] are valid and may be parsed.

It will be apparent to those of ordinary skill in the art that methods involved in embodiments of the present invention may be embodied in a computer program product that includes a computer usable medium. For example, such a computer usable medium may consist of a read only memory device, such as a Compact Disk Read Only Memory (CD ROM) disk or conventional ROM devices, or a computer diskette, having a computer readable program code stored thereon.

While embodiments of the invention have been particularly shown and described with references to embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of embodiments of the invention encompassed by the appended claims.

CLAIMS

[Claim 1]

A processor comprising:

a decode unit to receive a first instruction to perform an Advanced Encryption Standard (AES) round of an AES algorithm and a second instruction to generate a round key for the AES round, the first instruction to have a source operand that is to include input data for the AES round, and the first instruction to have a source operand that is to include the round key for the AES round and the second instruction to have a source operand that is to include a previous round key for a previous AES round;

a key scheduler, in response to the second instruction, to generate the round key for the AES round based on the previous round key; and

an execution unit coupled with the decode unit, the execution unit, in response to the first instruction, to store a result in a destination of the first instruction, the result to include the input data transformed by the AES round using the round key.

[Claim 2]

The processor of claim 1, wherein

the first instruction is to perform an AES encryption round.

[Claim 3]

The processor of claim 1, wherein

the first instruction is to perform an AES decryption round.

[Claim 4]

The processor of claim 1, wherein

the source operand that is to include the input data is stored in a register, and wherein

the source operand that is to include the round key is stored in a register.

[Claim 5]

The processor of claim 4, wherein

the registers comprise 128-bit registers.

[Claim 6]

The processor of any one of claims 1 to 5, wherein

the execution unit, in response to the first instruction, is to overwrite the input data with the result.

[Claim 7]

The processor of claim 1, wherein

the execution unit, in response to the first instruction, is to perform operations comprising:

performing an S-Box lookup;

shifting rows;

mixing columns; and

adding round keys.

[Claim 8]

The processor of claim 1, wherein

the second instruction has an immediate, and wherein

the key scheduler is to generate the round key for the AES round based on the previous round key and the immediate, and wherein

the second instruction has a different opcode from the first instruction.

[Claim 9]

The processor of claim 1, wherein:

the decode unit is to receive a third instruction to perform a last AES round of the AES algorithm, the third instruction to have a source operand that is to include input data for the last AES round, and the third instruction to have a source operand that is to include a last round key for the last AES round; and

the execution unit, in response to the third instruction, to store a second result in a destination of the third instruction, the second result to include the input data for the last AES round transformed by the last AES round using the last round key for the last AES round, wherein the third instruction has a different opcode form the first instruction.

[Claim 10]

The processor any one of claims 1 to 9, wherein

the processor comprises a general-purpose processor.

[Claim 11]

A processor comprising:

a plurality of 128-bit registers;

a decode unit to receive a first instruction to perform an Advanced Encryption Standard (AES) encryption round and a second instruction to generate a round key for the AES encryption round, the first instruction to indicate a first 128-bit register of the plurality that is to include information to be encrypted, and the first instruction to indicate a second 128-bit register of the plurality that is to include the round key for the AES encryption round, and the second instruction to have a source operand that is to include a previous round key for a previous AES encryption round;

a key scheduler, in response to the second instruction, to generate the round key for the AES encryption round based on the previous round key; and

an execution unit coupled with the decode unit and the plurality of 128-bit registers, the execution unit, in response to the first instruction, to store a result in a destination of the first instruction, the result to include the information from the first 128-bit register transformed by the AES encryption round using the round key.

[Claim 12]

The processor of claim 11, wherein

the execution unit, in response to the first instruction, is to perform operations comprising:

performing an S-Box lookup;

shifting rows;

mixing columns; and

adding round keys.

[Claim 13]

The processor of claim 11 or 12, wherein

the processor comprises a general-purpose processor.

[Claim 14]

A processor comprising:

a plurality of 128-bit registers;

a decode unit to receive a first instruction to perform an Advanced Encryption Standard (AES) decryption round and a second instruction to generate a round key for the AES decryption round, the first instruction to indicate a first 128-bit register of the plurality that is to include information to be decrypted, and the first instruction to indicate a second 128-bit register of the plurality that is to include the round key for the AES decryption round, and the second instruction to have a source operand that is to include a previous round key for a previous AES decryption round;

a key scheduler, in response to the second instruction, to generate the round key for the AES decryption round based on the previous round key; and

an execution unit coupled with the decode unit and the plurality of 128-bit registers, the execution unit, in response to the first instruction, to store a result in a destination of the first instruction, the result to include the information from the first 128-bit register transformed by the AES decryption round using the round key.

[Claim 15]

The processor of claim 14, wherein

the processor comprises a general-purpose processor.

[Claim 16]

A processor comprising:

a decode unit to receive an instruction to generate a round key for an Advanced Encryption Standard (AES) round, the instruction to have a source operand that is to include a previous round key for a previous AES round; and

a key scheduler coupled with the decode unit, the key scheduler, in response to the instruction, to store the round key for the AES round in a destination of the instruction.

[Claim 17]

The processor of claim 16, wherein

the instruction has an immediate, and wherein the key scheduler is to generate the round key for the AES round based on the immediate, wherein

the destination comprises a 128-bit register.

[Claim 18]

A processor comprising:

a decode unit to receive and decode a plurality of instructions including at least:

a first instruction to generate a first round key for a first given Advanced Encryption Standard (AES) encryption round, the first instruction to have a first instruction source operand that is to include a key to be used to generate the first round key;

a second instruction to perform a second given AES encryption round, the second instruction to have a second instruction first source operand that is to include input data for the second given AES encryption round, and the second instruction to have a second instruction second source operand that is to include a second round key for the second given AES encryption round; and

a third instruction to perform an AES encryption last round, the third instruction to have a third instruction first source operand that is to include input data for the AES encryption last round, and the third instruction to have a third instruction second source operand that is to include a last round key for the AES encryption last round;

a key scheduler, in response to the first instruction, to generate the first round key for the first given AES encryption round based on the key from the first instruction source operand; and

an execution unit, coupled with the decode unit, the execution unit:

in response to the second instruction, to store a result of the second instruction in a destination of the second instruction, the result of the second instruction to include the input data for the second given AES encryption round transformed by the second given AES encryption round using the second round key; and

in response to the third instruction, to store a result of the third instruction in a destination of the third instruction, the result of the third instruction to include the input data for the AES encryption last round transformed by the AES encryption last round using the last round key.

[Claim 19]

The processor of claim 18, wherein

the first instruction has a first opcode, the second instruction has a second opcode different from the first opcode, and the third instruction has a third opcode different from the first and second opcodes.

[Claim 20]

The processor of claim 18, wherein

the first instruction has an immediate, and wherein

the key scheduler is to generate the first round key based on the immediate.

[Claim 21]

The processor of any one of claims 18 to 20, wherein

the processor comprises a general-purpose processor.