

"Improvements in magnetic recording
and playback apparatus"

The present invention relates to magnetic recording and playback apparatus which incorporates a signal.

Variable impedance circuits such as signal
5 transmission circuits, in which the impedance of a signal transmission path is varied by current control, are known from U.S. Patent Specification Nos. 3,761,741 and 4,220,875.

We have made a thorough study of the known
10 variable impedance circuits. From our detailed studies we have noted that the current consumption increases sharply when the impedance is reduced to a small value. In particular, we have found that the current consumption increases in inverse proportion to the impedance.

On the other hand, a switched capacitor filter
15 which is a sampled value filter has been made as a monolithic filter in recent years, as reported in the proceedings of the IEEE Vol. 67 No. 10 at p1403 (October 1979) in an article entitled "Application of CCD and
20 switched capacitor filter technology by Hewes et al.

In a switched capacitor, an impedance is equivalently formed of the capacitance of a capacitor and the frequency of a clock signal applied to switching means.

It is an object of the present invention to provide a signal transmission circuit of low current consumption, for use with magnetic recording and playback apparatus.

5 According to the present invention there is provided a magnetic recording and playback apparatus including:

(a) a playback amplifier which detects a signal recorded on a magnetic tape;

10 (b) a first switched capacitor whose input terminal is connected to an output terminal of said playback amplifier;

(c) a recording amplifier;

(d) a second switched capacitor whose
15 output terminal is connected to an input terminal of said recording amplifier;

(e) an oscillator circuit which generates control signals to be applied to said first and second capacitors; and

20 (f) circuit means for generating an A.C. bias signal for the magnetic tape; wherein a difference between a frequency of the control signals and that of the A.C. bias signal is set at zero or outside an audio-frequency
25 band.

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The present invention will now be described in greater detail by way of examples with reference to the accompanying drawings, wherein:-

5 Figure 1 is a circuit diagram of a first preferred form of a signal transmission circuit for use with magnetic recording and playback apparatus;

10 Figure 2 is a circuit diagram of a second embodiment of a signal transmission circuit;

 Figure 3 is a circuit diagram of a third embodiment of a signal transmission circuit;

15 Figure 4 is a circuit diagram of a fourth embodiment of a signal transmission circuit;

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Figure 5 is a circuit diagram of a fifth embodiment of a signal transmission circuit;

Figure 6 is a circuit diagram of an amplifier circuit which incorporates a sixth embodiment of a signal transmission circuit; and

Figure 7 is a circuit diagram of the principal components of a tape recorder incorporating a seventh embodiment of a signal transmission circuit.

The first embodiment of a variable impedance circuit as a signal transmission circuit to which the present invention is applied will first be described with reference to Figure 1.

An SCF (Switched Capacitor Filter) is incorporated between an input terminal T_1 and the non-inverting input terminal of an operational amplifier 1. The SCF comprises switches S_1 and S_2 and capacitors C_1 and C_2 . The change-over of the switches S_1 and S_2 into their "on" states or "off" states is effected by the output signal ϕ of a voltage-controlled oscillator (hereinafter, abbreviated to "VCO") 2 and the output signal ϕ' of an inverter 3 respectively. A variable voltage V_C is provided to control the output signal ϕ of the VCO 2 to a desired frequency.

Assuming now that the switch S_2 be in the "off" state in accordance with the output signal ϕ ,

the switch S_1 is in the "on" state in accordance with the phase-inverted output signal ϕ' which is provided from the inverter 3. An input signal V_{IN} is transmitted to the capacitor C_1 through the switch S_1 , to charge the capacitor C_1 .

In contrast, when the output signal ϕ has its phase inverted, the switch S_2 is changed-over into the "on" state. Simultaneously therewith, the output signal ϕ' of the inverter 3 has its phase inverted to bring the switch S_1 into the "off" state. In this state, the charging current which has been flowing to the capacitor C_1 through the switch S_1 is cut off. The charge stored in the capacitor C_1 is supplied to the capacitor C_2 through the switch S_2 . Thus, the charge is moved from the capacitor C_1 into the capacitor C_2 . As a result, a voltage which is determined by the charged potential of the capacitor C_2 becomes the input voltage of the operational amplifier 1.

The circuit operation described above is equivalent to the case where the current flow to the capacitor C_2 is supplied through an impedance.

More specifically, at a time $t = n T_C$ where T_C denotes the period of the output signals ϕ and ϕ' originating from the VCO-2, and n denotes an

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arbitrary number, the charges stored in the capacitor C_1 are expressed by $C_1 V_{in} [n T_c]$, assuming the switch S_1 to be "on" and the switch S_2 "off". Since, at this time, the voltage of the capacitor C_2 corresponds to the previous half cycle, the charges stored in the capacitor C_2 are expressed by $C_2 V_{in} [(n - \frac{1}{2}) T_c]$.

Subsequently, when the switch S_1 has changed-over from "on" into "off" and the switch S_2 from "off" into "on", the charge stored in the capacitor C_1 is transferred to the capacitor C_2 . Accordingly, the charge stored in the capacitor C_2 at a time $t = (n + \frac{1}{2}) T_c$ becomes the following equation, in accordance with the law of conservation of charge:-

$$C_2 V_{OUT} [(n + \frac{1}{2}) T_c] = C_2 V_{OUT} [(n - \frac{1}{2}) T_c] - C_1 V_{in} (n T_c) \quad \dots\dots(1)$$

Thus, a transfer function $H_{\frac{1}{2}}(Z)$ in the corresponding half cycle becomes as follows :-

$$H_{\frac{1}{2}}(Z) = - \frac{C_1}{C_2} \frac{Z^{-\frac{1}{2}}}{1 - Z^{-1}} \quad \dots\dots(2)$$

where $Z^{-\frac{1}{2}}$ indicates a delay corresponding to the half cycle.

un. 3.

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In the next half cycle from the time
 $t = (n + \frac{1}{2}) T_c$ to a time $t = (n + 1) T_c$,
 merely a delay corresponding to the half cycle arises
 while the output voltage V_{OUT} is held. Therefore,
 5 the transfer function $H_1(z)$ of the whole cycle becomes
 as follows :

$$H_1(z) = - \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \quad \dots\dots(3)$$

Assuming that a frequency f_c corresponding
 to the period T_c of the output signals ϕ and ϕ'
 10 from the VCO 2 be very high, $z = e^{s T_c} \approx 1 + s T_c$
 holds. Accordingly, Equation (3) becomes as
 follows :

$$H_1(z) \approx - \frac{C_1}{s C_1 T_c} \quad \dots\dots(4)$$

This signifies that the resistance R of the
 15 transfer function $H(s) = 1/(s C R)$ of a CR integrator
 circuit is equivalently formed by the value T_c/C_1
 of the switched capacitor.

Therefore, the variable impedance circuit
 in the present embodiment has the frequency f_c
 20 and period T_c of the output signal ϕ controlled
 by adjusting the voltage level of the control

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voltage V_c . In consequence, the equivalent resistance T_c/C_1 of the signal transmission circuit extending from the input terminal T_1 to the non-inverting input terminal of the operational amplifier 1 is controlled.

Accordingly, the equivalent resistance T_c/C_1 and capacitor C_2 of the switched capacitor determine a frequency characteristic, which can be controlled by the frequency f_c and period T_c of the output signals ϕ and ϕ' from the VCO 2.

Semiconductor switching elements such as MOSFETs can be utilized as the switching means S_1 and S_2 , and the VCO 2 can be replaced with a current-controlled oscillator.

Next, an example of the application of the variable impedance circuit explained as the first embodiment will now be described with reference to the second embodiment shown in Figure 2.

A signal e_1 produced from a signal source is supplied to an amplifier 11 and a level detector 12. The level detector 12 as shown is a rectifying circuit.

The frequency f_c of the output signal ϕ to be provided from the VCO 2 is varied in correspondence with the control voltage V_c derived from the level detector 12. The switches S_1 and S_2 are alternately changed-over into their "on" and "off" states by the output signals ϕ and ϕ' . In relation to a signal e' amplified by the amplifier 11, the switches S_1 , S_2 and the capacitors C_1 , C_2 operate in similar manner to those in the case of the first embodiment. The charged voltage level of the capacitor C_2 becomes an input signal to an amplifier 13, and an output signal V_{out} is provided from a terminal T_2 .

In the second embodiment described above, the resistance of the transmission path of the signal e_1 , in other words, the gain and frequency characteristic thereof is/are varied by the voltage level of the signal e_1 , not by the frequency thereof. The gain of the transmission path can also be varied by the voltage level and the frequency in such a way that a filter circuit 14 of various characteristics is inserted in the control loop as shown in the third embodiment in Figure 3. This is well suited to, for example, the noise reduction system of a tape recorder.

Next, the fourth embodiment will be described with reference to Figure 4.

The switches S_1 and S_2 shown in Figures 1, 2 and 3 can be equivalently expressed by switching means S_{11} as illustrated in Figure 4. That is, the operations of the switches S_1 , S_2 can be so interpreted that the switching means S_{11} is changed-over to the sides of contacts a and b by the signals $\emptyset$ and $\emptyset'$ as indicated in each of the foregoing embodiments.

In this case, a low-pass filter of $\zeta = \emptyset \frac{C_2}{C_1}$ is formed. However, when the switching means S_{11} is held connected to the contact a as illustrated in the figure, in other words, when the switch S_1 is "on" and the switch S_2 is "off" in Figures 1 to 3, the impedance between the contacts a and b becomes infinity, and the contact a is earthed through the capacitor C_1 . Accordingly, the input signal V_{IN} is not transmitted to the capacitor C_2 and an amplifier 31.

When the switching means S_{11} is held connected to the contact b, the switch S_1 is "off" and the switch S_2 is "on", and hence, the input signal is not transmitted to the amplifier 31 also in this case.

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These circuits can be utilized as, for example, the NR (noise reduction) on-off switches of noise reduction systems. In this case, any NR on-off switch need not be separately provided, but merely
5 the clock may be stopped, so that the circuit arrangement is simplified.

Since, in this system, a voltage stored in the capacitor C_2 immediately before the clock is stopped remains immediately after the same, the
10 input signal of the amplifier 31 does not change suddenly.

The fifth embodiment will now be described with reference to Figure 5.

An input terminal T_3 is supplied with a control
15 signal ϕ whose duty ratio is variable. As is well known, the duty ratio of the control signal ϕ signifies the ratio between the period of the high level "H" and that of the low level "L" of the control signal ϕ . A monostable circuit is provided for generating
20 the control signal ϕ of the variable duty ratio, although this circuit is not shown in Figure 5. In this case also, the switches S_1 and S_2 are alternately changed-over into their "on" and "off" states. However, even when the frequency of the
25 signal ϕ is constant, the charging time of the



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capacitor C_1 can be made long and the discharging time thereof short by varying the duty ratio of the signal ϕ . Alternatively, it is possible to make the charging time short and the discharging time long. Accordingly, in the case where a switched capacitor is used as a variable impedance, the frequency or/and the duty ratio of the clock pulses may be controlled.

The sixth embodiment incorporated in an amplified circuit will now be described with reference to Figure 6.

The amplified circuit comprises an amplifier 41 which is constructed in the form of an operational amplifier, and a switched capacitor filter (SCF) 42 which has switches S_1 and S_2 and capacitors C_1 and C_2 as shown in Figure 1. The SCF 42 has either or both of the switches S_1 and S_2 changed-over into their "off" states by control signals ϕ and ϕ' . A control signal generator circuit for generating the control signals ϕ and ϕ' , and a control circuit are provided although these circuits are not shown in Figure 6. When the output signal of the control circuit has become a predetermined level, one of the control signals ϕ and ϕ' to be delivered from the control signal generator circuit is held at its high level, and the other is held at its low

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level, whereby the signal transmitting function of the switched capacitor filter 42 is inhibited. In this case, the SCF 42 is electrically disconnected between the output terminal and inverting input terminal of the amplifier 41. Accordingly, the amplification factor of the amplifier is determined by the ratio between feedback resistances R_s and R_f , and it exhibits a substantially flat frequency characteristic.

10 In contrast, in the case where the SCF 42 operates normally, the circuit between terminals T_1 and T_2 becomes an amplifier circuit which has an amplification factor dependent upon the frequency characteristic of the SCF 42.

15 In this manner, as disclosed in the sixth embodiment, the closed loop amplification factor of the amplifier can be controlled at will by controlling the operation of the SCF incorporated in the feedback loop of the amplifier.

20 The seventh embodiment which is incorporated within a tape recorder, will now be described with reference to Figure 7.

A recorded signal on a magnetic tape 62 is detected by a playback head 63 and is amplified by a playback amplifier 54, whereupon the amplified signal is applied to the first input terminal IN

(S) of an SCF 52. A signal path extending between the first input terminal IN and first output terminal OUT of the SCF 52 functions as an NABB playback equalizer, which attenuates signal components of high frequencies. An output signal from the first output terminal OUT of the SCF 52 is supplied to a speaker through a playback power amplifier.

A signal from, e.g., a microphone is transmitted to the input terminal of a recording amplifier 55 through a signal path which extends between the second input terminal IN' and second output terminal OUT' of the SCF 52. This signal path between the second input terminal IN' and second output terminal OUT' of the SCF 52 functions as a recording equalizer for compensating the high frequency losses of the magnetic tape 62 and heads 61 and 63. An output signal from the recording amplifier 55 is transmitted to the recording head 61 through a resonance circuit which comprises a coil L_1 and a capacitor C_{12} .

20 A crystal oscillator 51 and an inverter 53 are circuits which are provided for generating control signals $\emptyset$ and $\emptyset'$ of opposite phases for application to switching means included within the SCF 52.

When a recording/playback change-over signal R/P is at the high level, the signal path between

the first input terminal IN and first output terminal OUT of the SCF 52 is cut off, while when the recording/playback change-over signal R/P is at the low level, the signal path between the second input terminal IN' and second output terminal OUT' of the SCF 52 is cut off.

A transistor Q_1 and a boosting transformer T_1 are similarly driven by the control signal ϕ of 100 KHz produced from the crystal oscillator 51, whereby an A.C. bias signal of 100 KHz is applied to the magnetic tape 62 in the recording mode.

Meanwhile, in the SCF 52, the control signals ϕ and ϕ' leak to the outputs OUT and OUT' through the stray capacitances of the switching means constituting the SCF. If the difference frequency between the frequency of the control signals ϕ , ϕ' and that of the A.C. bias signal exists within the audio-frequency band, it will form a "beat offensive to the ear" to hamper the playback operation of the tape recorder.

Since, however, both the frequency of the control signals ϕ , ϕ' and that of the A.C. bias signal are 100 KHz in the present embodiment, the difference frequency becomes zero, and the hampering can be avoided. In a modified embodiment, the frequency

of the control signals ϕ , ϕ' to be applied to the SCF 52 is set at $m \times 100$ KHz (m : positive integer), the frequency of the A.C. bias signal is set at $n \times 100$ KHz (n : positive integer), and the difference frequency is accordingly set at $(m - n) \times 100$ KHz outside the audio-frequency band, whereby the audible beat interference can be prevented from arising.

The resonance circuit comprising the coil L_1 and the capacitor C_{12} is a bias trap circuit resonant to 100 KHz, and it inhibits the A.C. bias signal of the booster T_1 from being transmitted to the output of the recording amplifier 55.

In addition, the transistor Q_1 can be controlled into a non-conductive state in the playback mode by turning "on" a switch SW which is arranged across the base and emitter electrodes of the transistor Q_1 . In the playback mode, therefore, the generation of the unnecessary A.C. bias signal can be prevented.

The signal transmission circuits disclosed in the above embodiments are also applicable to magnetic recording and playback apparatus such as tape decks and VTRs, and also to general electronic equipment which employ, at least, a switched capacitor.



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CLAIMS:

1. A magnetic recording and playback apparatus including:

5 (a) a playback amplifier which detects a signal recorded on a magnetic tape;

(b) a first switched capacitor whose input terminal is connected to an output terminal of said playback amplifier;

(c) a recording amplifier;

10 (d) a second switched capacitor whose output terminal is connected to an input terminal of said recording amplifier;

(e) an oscillator circuit which generates control signals to be applied to said first and
15 second switched capacitors; and

(f) circuit means for generating an A.C. bias signal for the magnetic tape; wherein a difference frequency between a frequency of the control signals and that of A.C. bias signal
20 is set at zero or outside an audio-frequency band.

2. Apparatus according to claim 1, wherein each switched capacitor includes a capacitor and switching means.



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3. Apparatus according to claim 1,
wherein the control signals which are supplied
to the first and second switched capacitors
are in antiphase.
- 5 4. Apparatus according to any one of
the preceding claims, wherein said circuit
means for generating an A.C. bias signal combines
a transistor and boosting transformer, which
are driven by one of the control signals.
- 10 5. A magnetic recording and playback
apparatus constructed and arranged to operate
substantially as herein described with reference
to and as illustrated in Fig. 7 of the accompanying
drawings.
- 15 6. Apparatus according to claim 5,
incorporating a switched capacitor circuit
as disclosed in any one of Figs 1 to 6 of
the accompanying drawings.

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7. A signal transmission circuit constructed and arranged to operate substantially as herein described with reference to any one of the figures of the accompanying drawings.
