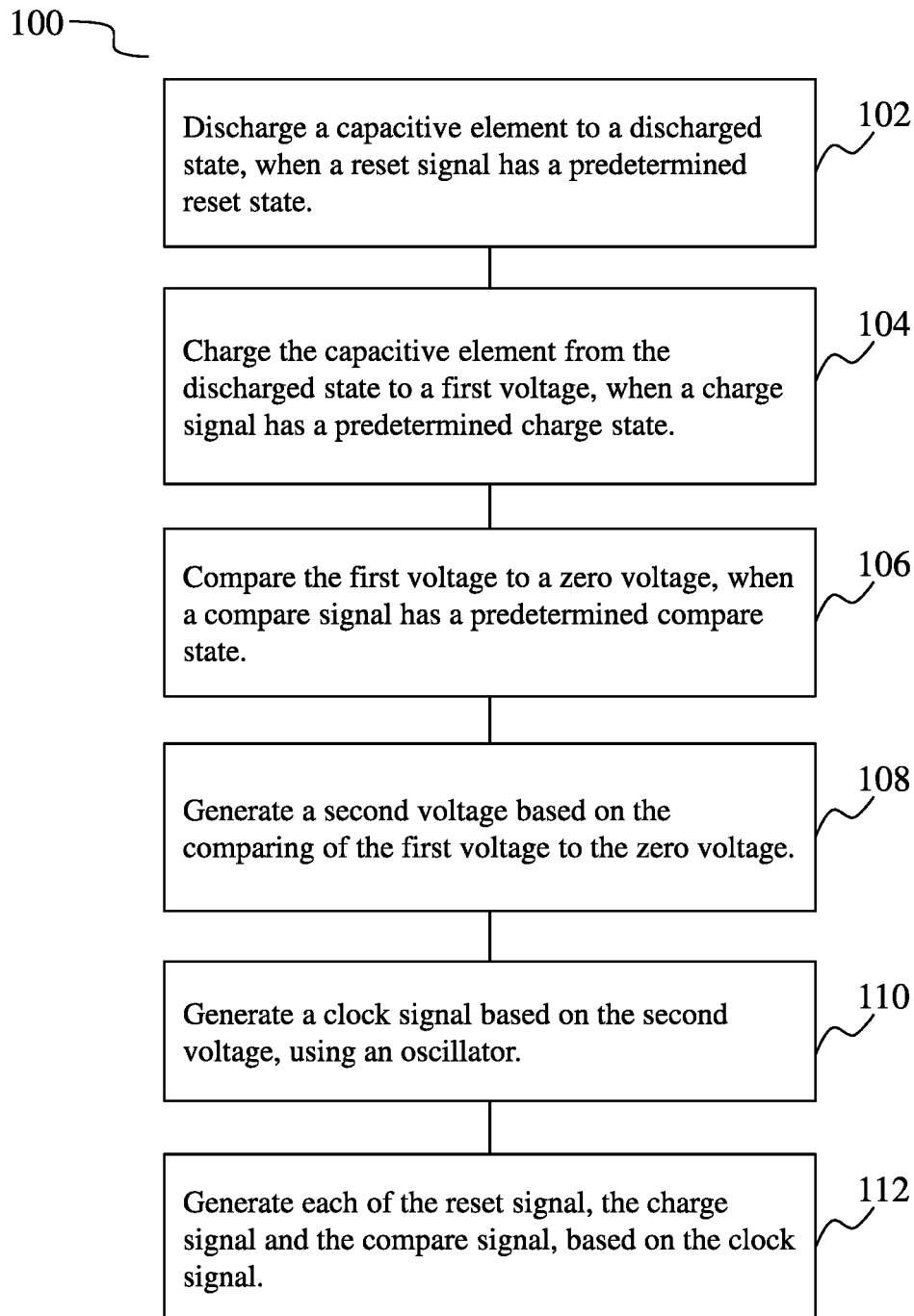
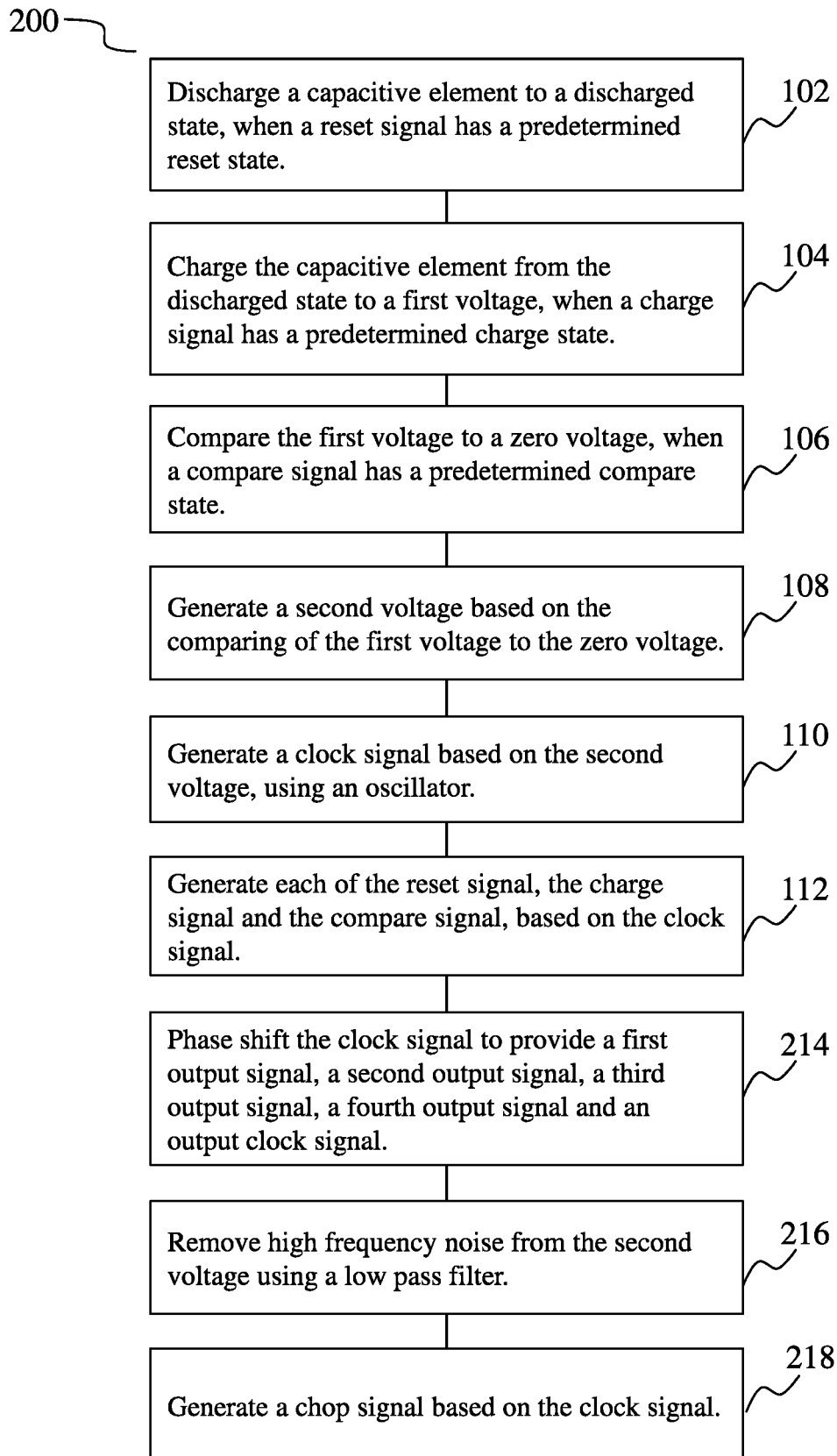
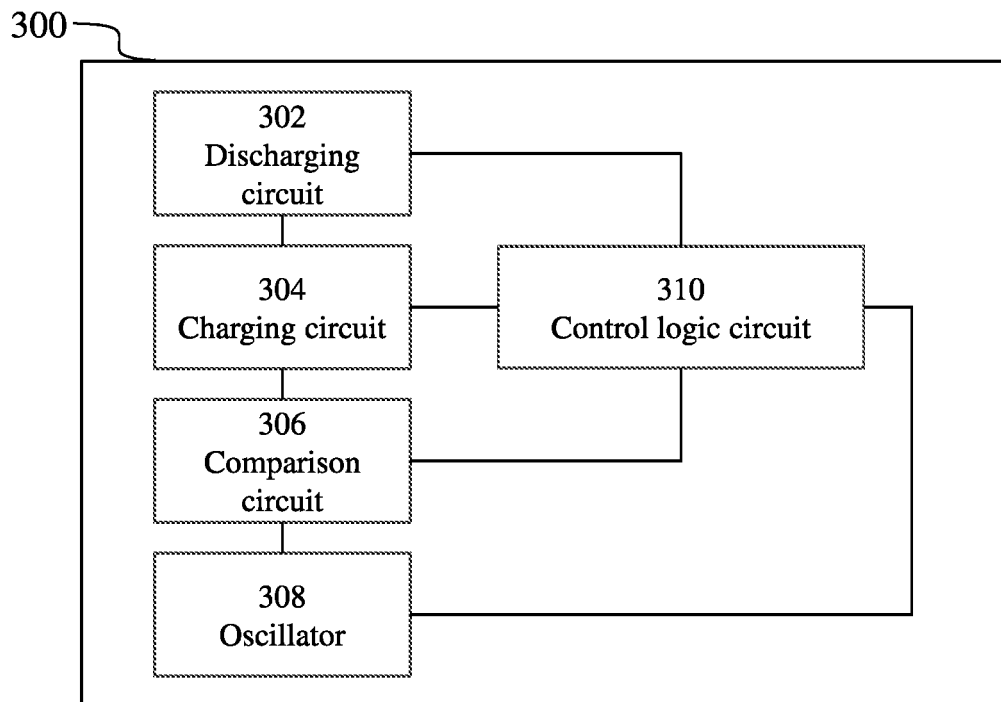
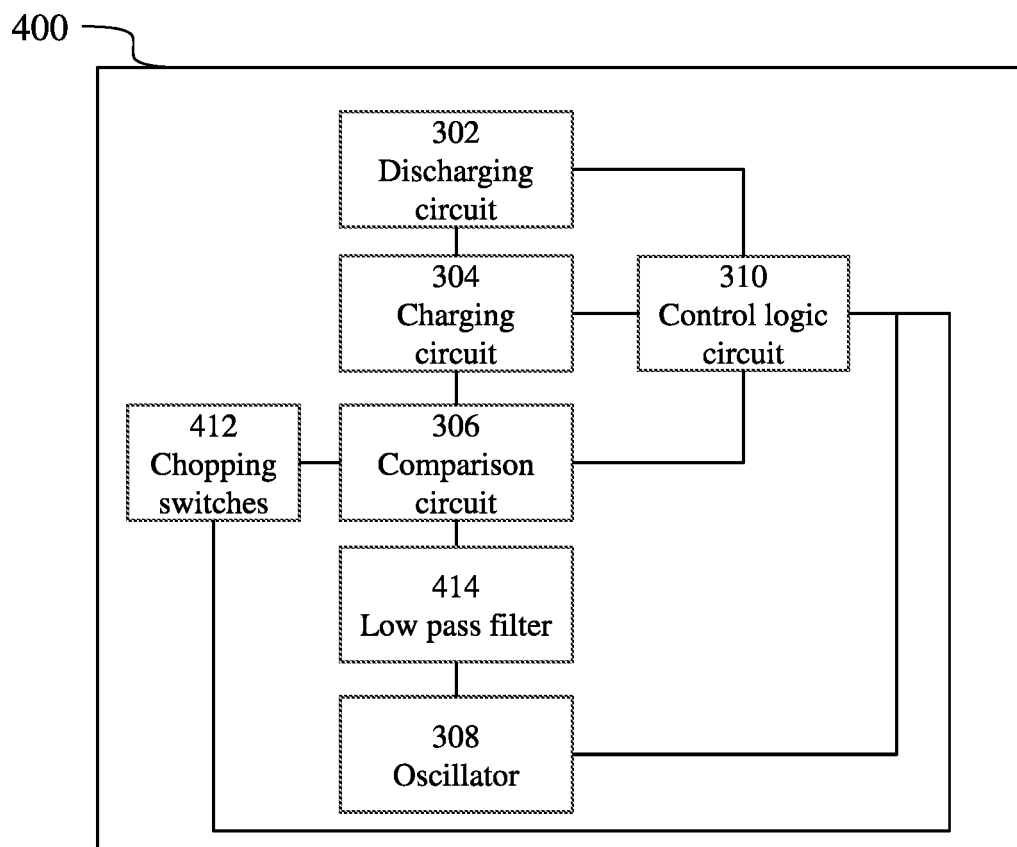


**FIG. 1**

**FIG. 2**

**FIG. 3****FIG. 4**

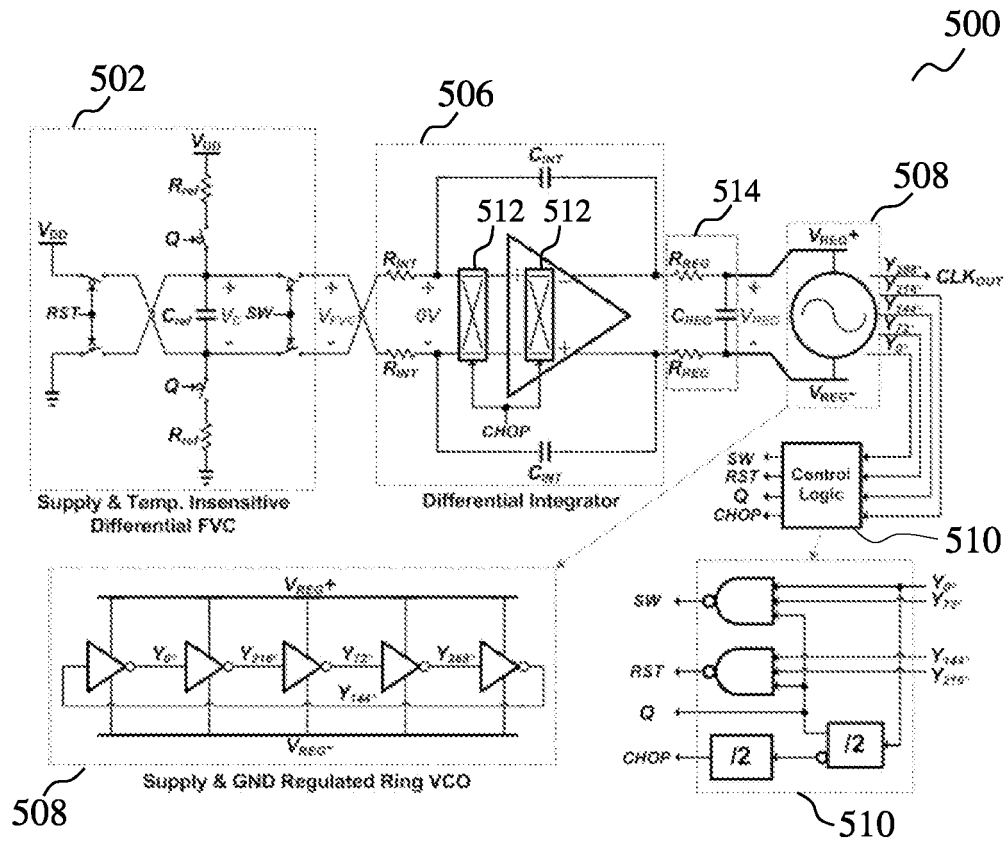


FIG. 5

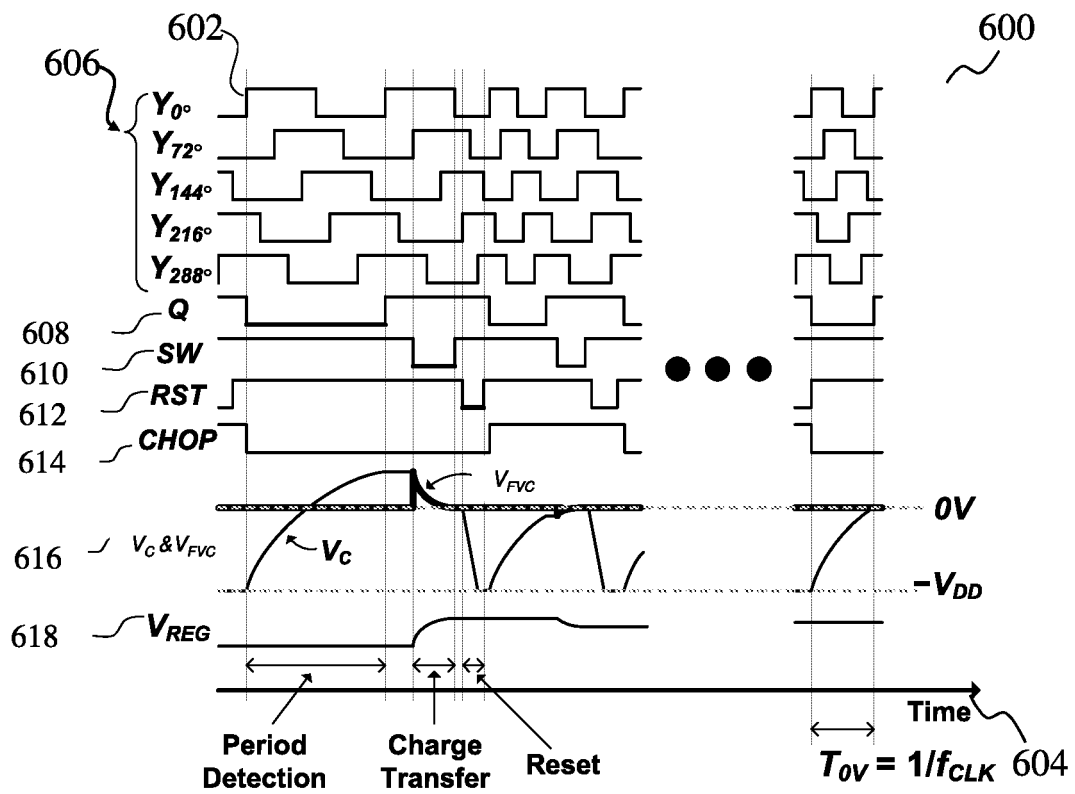
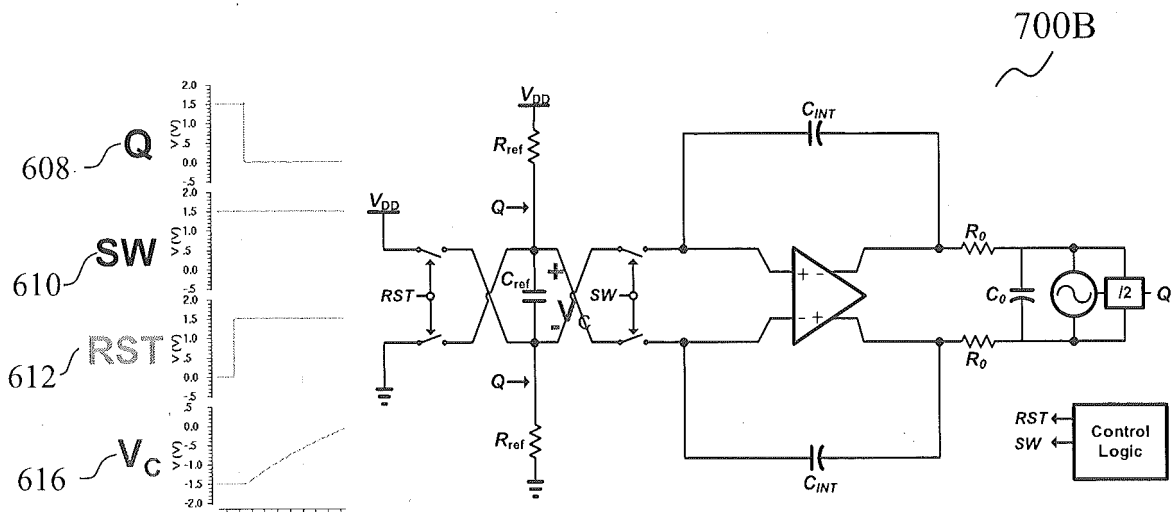
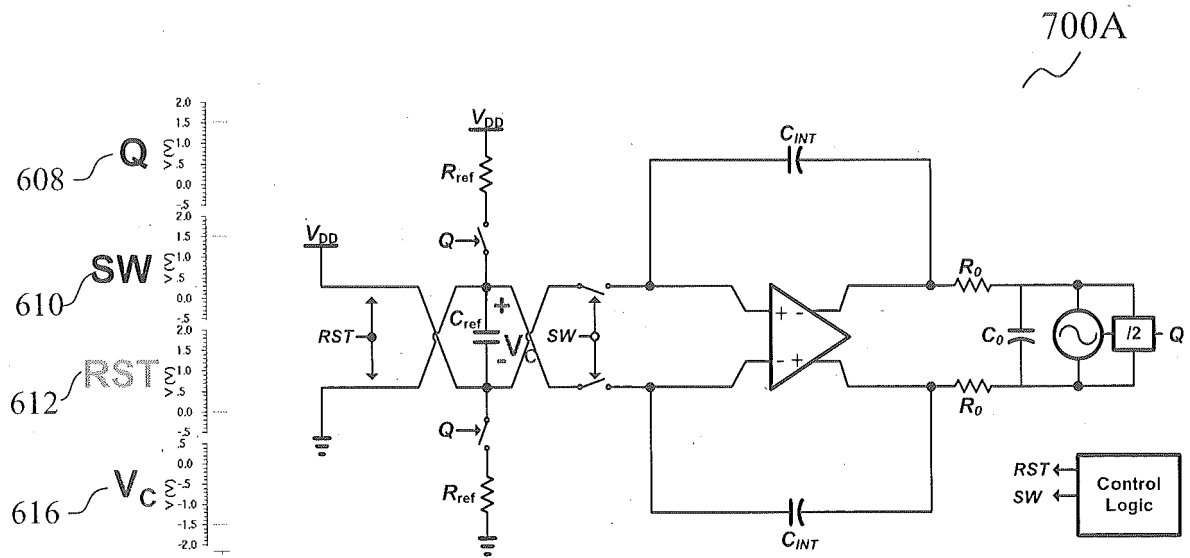


FIG. 6



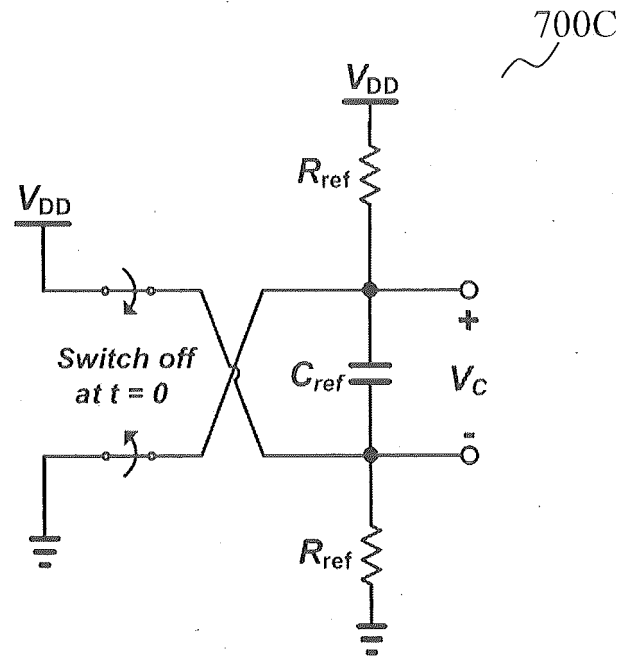


FIG. 7C

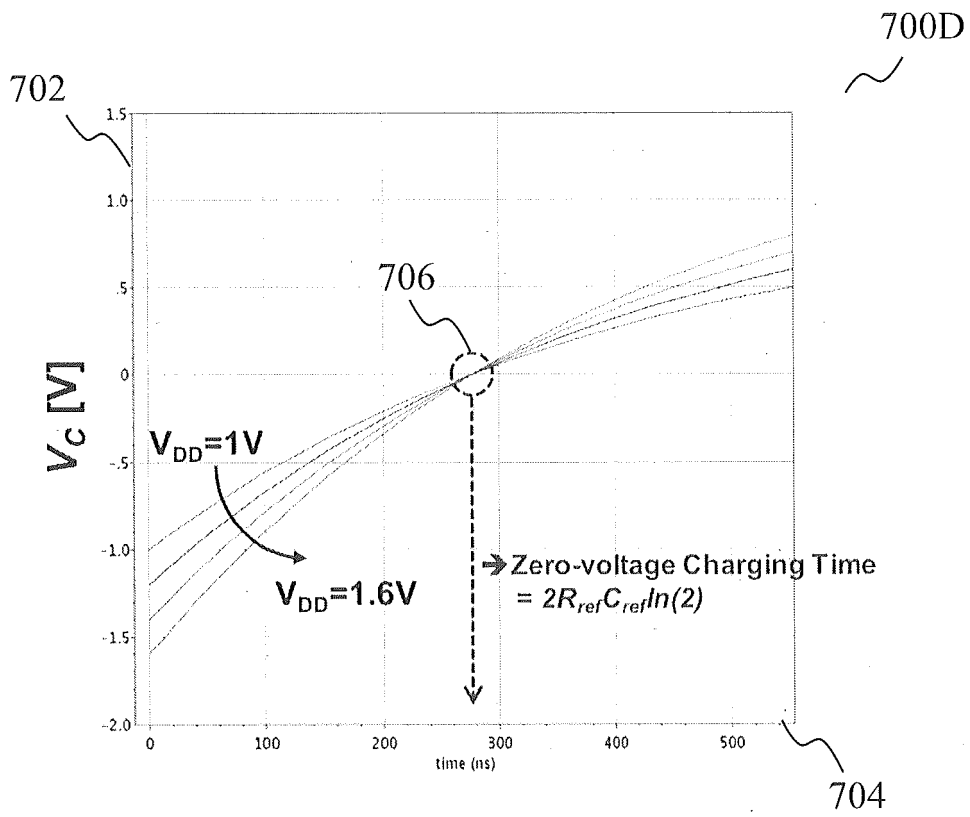


FIG. 7D

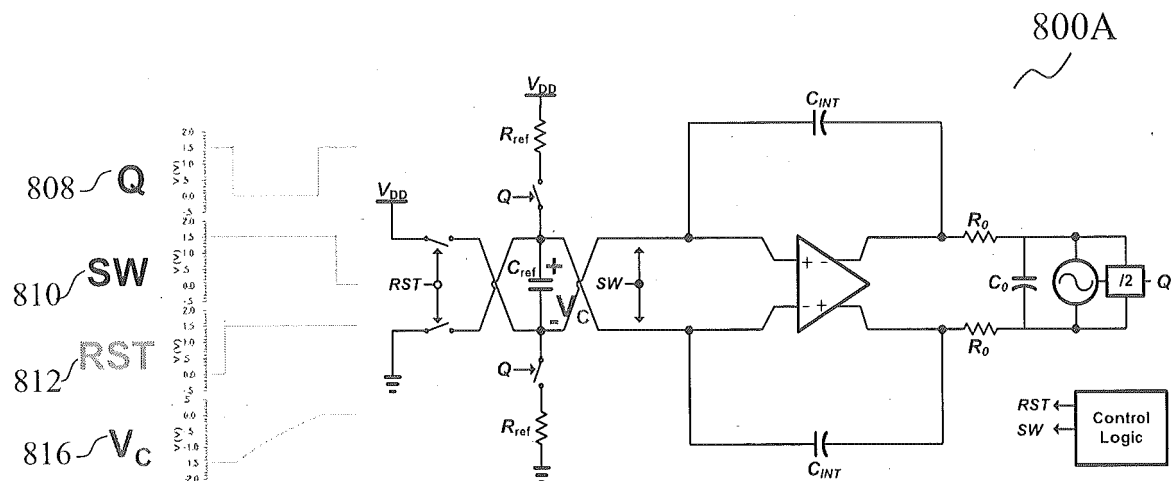


FIG. 8A

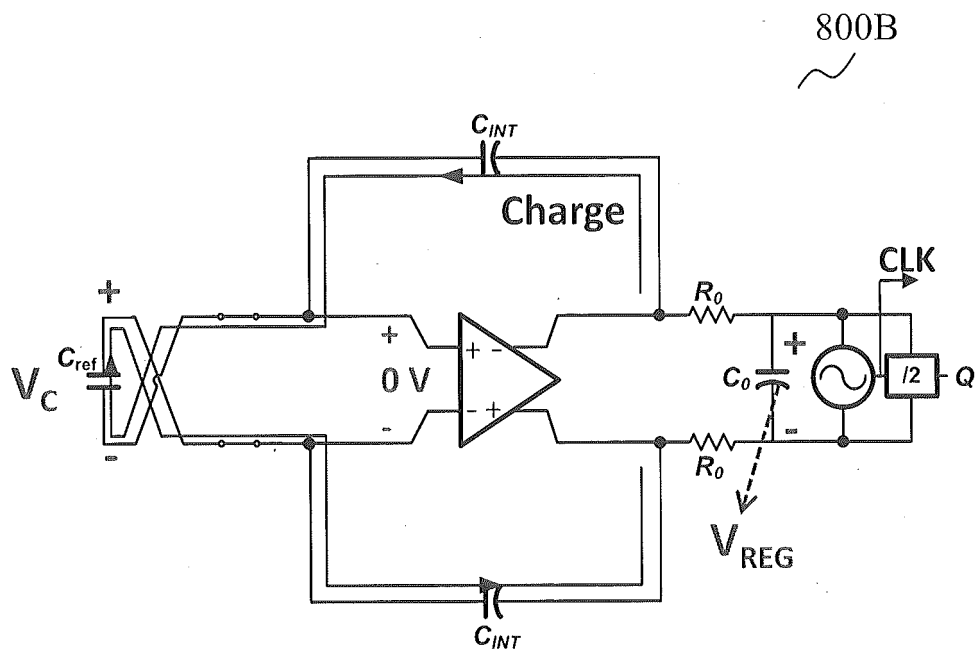


FIG. 8B

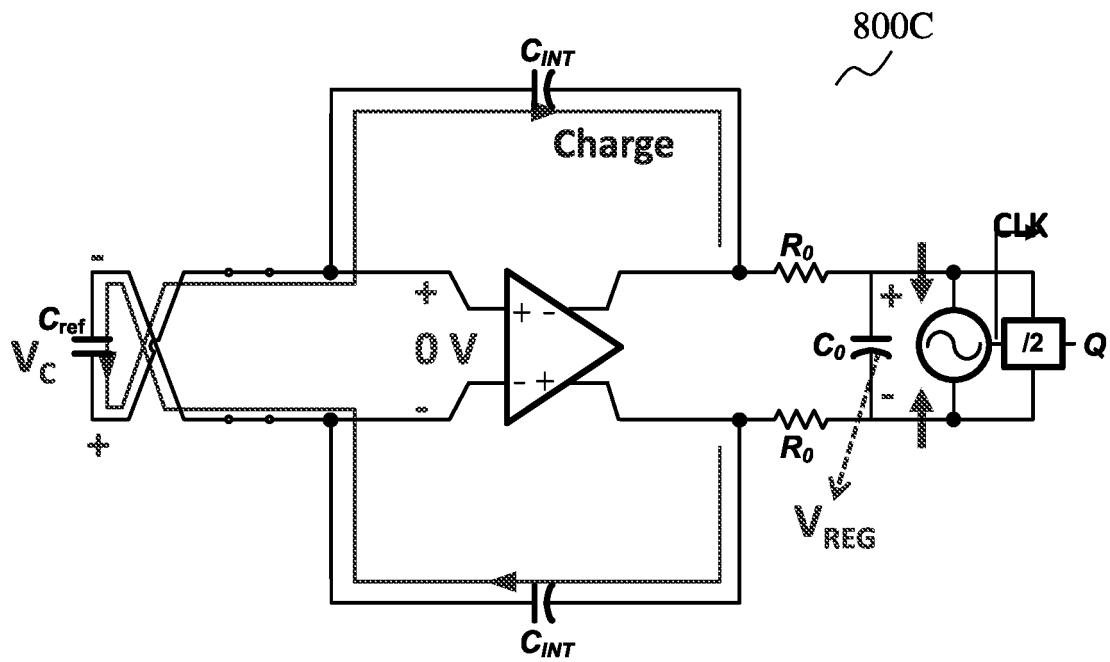


FIG. 8C

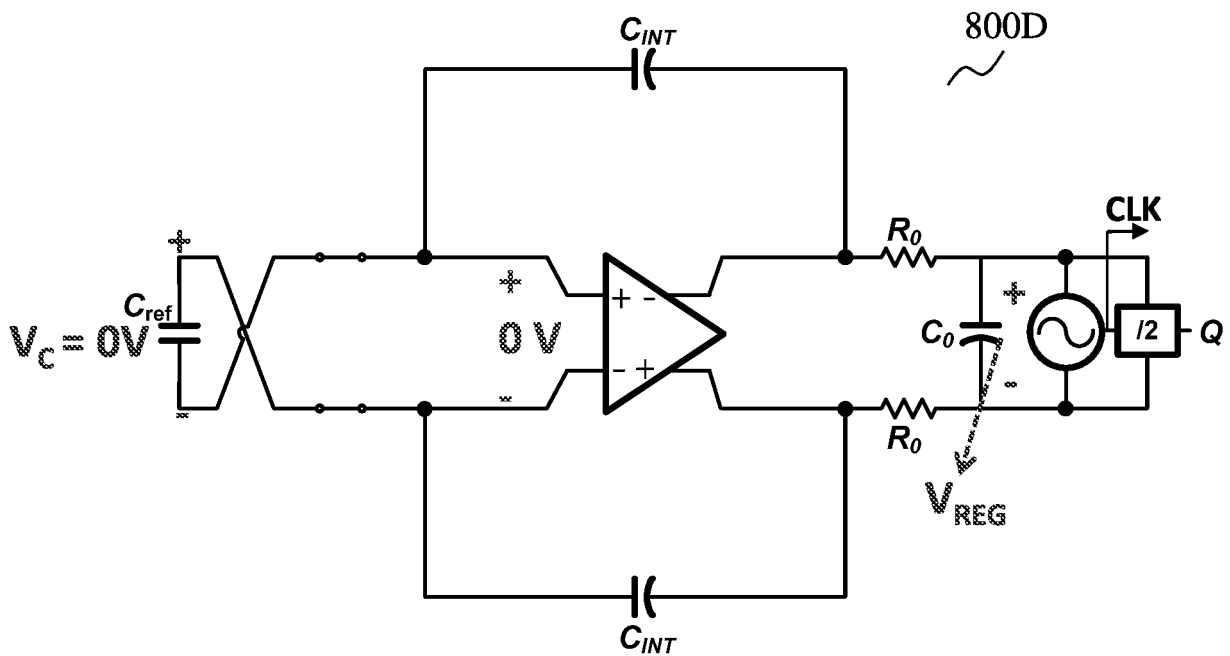


FIG. 8D

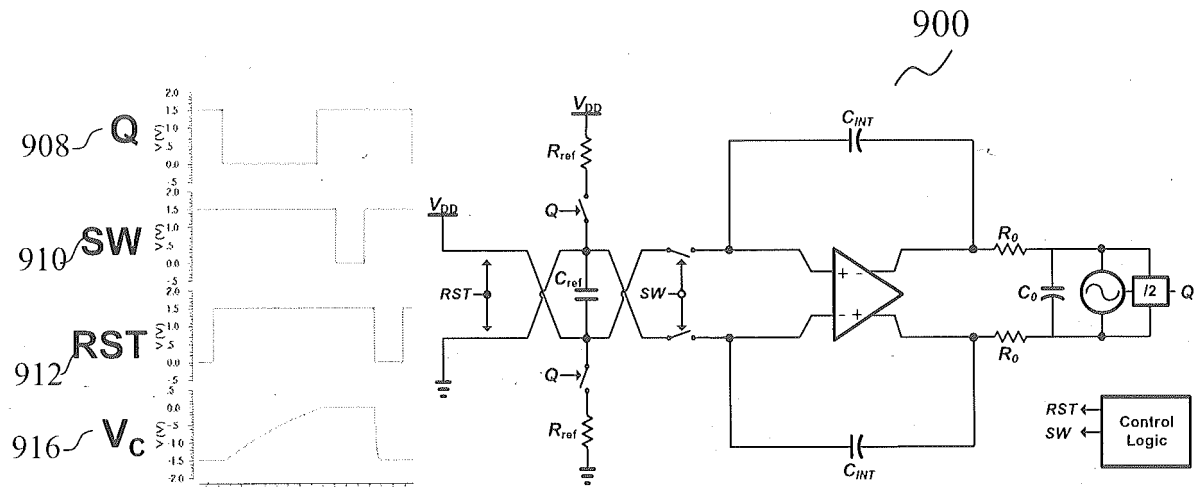


FIG. 9

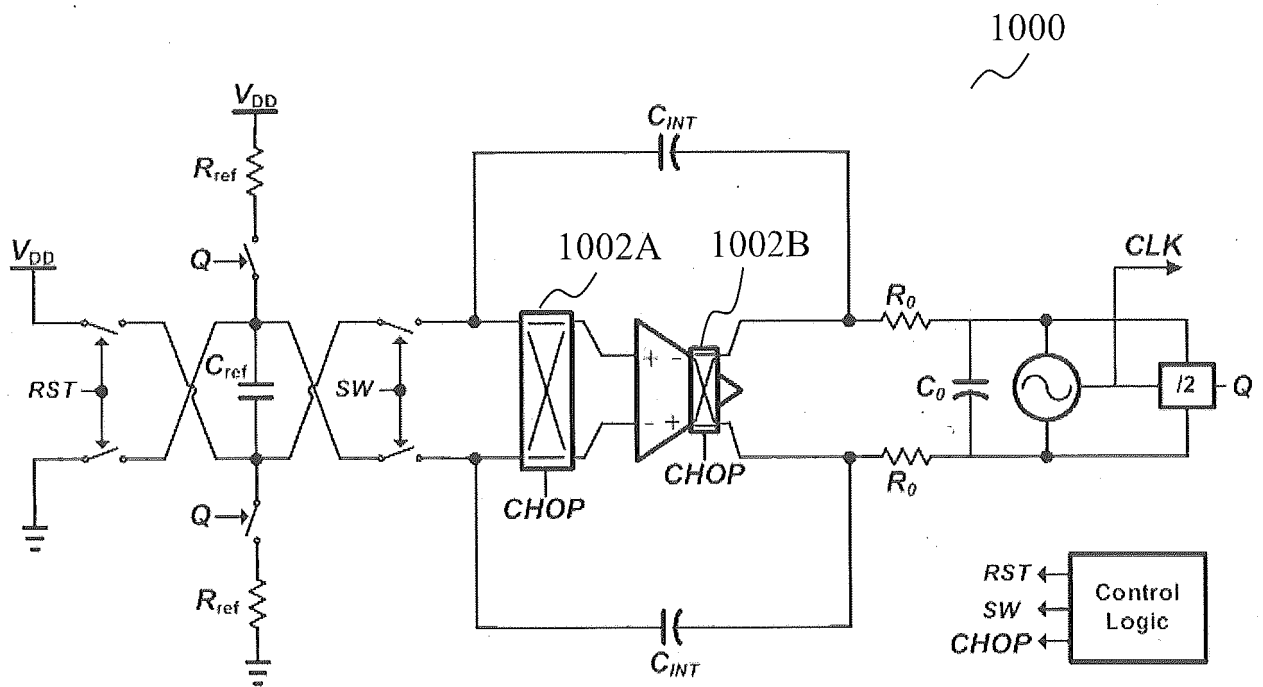


FIG. 10

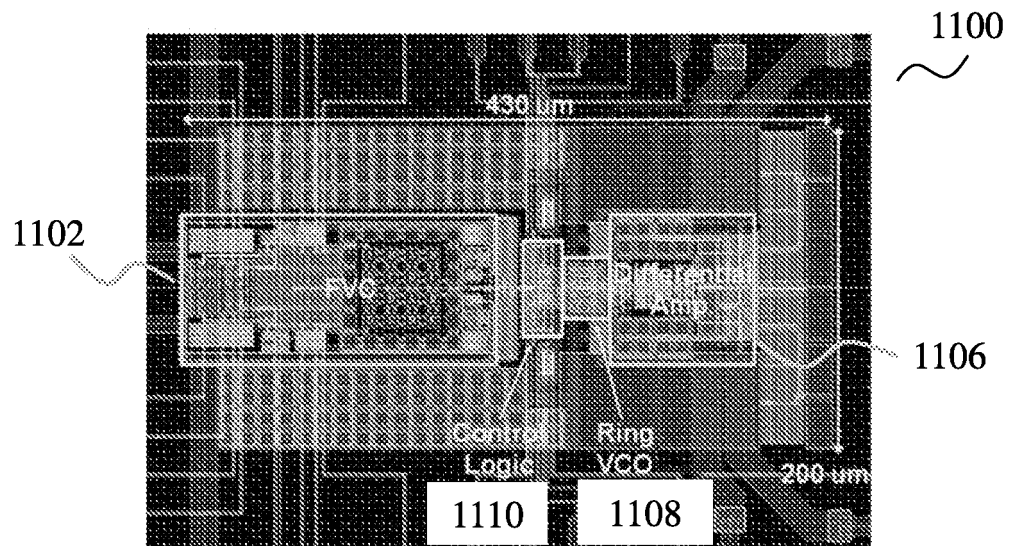


FIG. 11

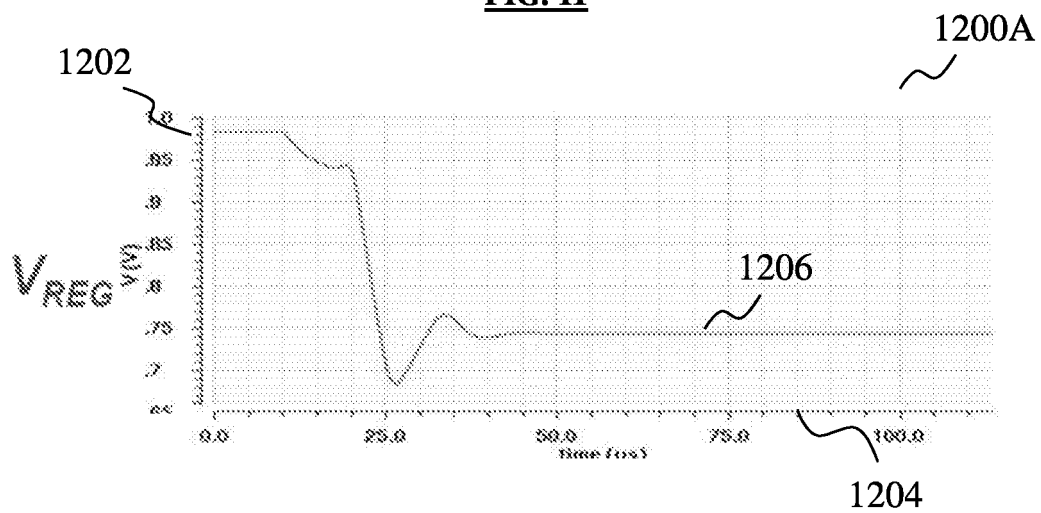


FIG. 12A

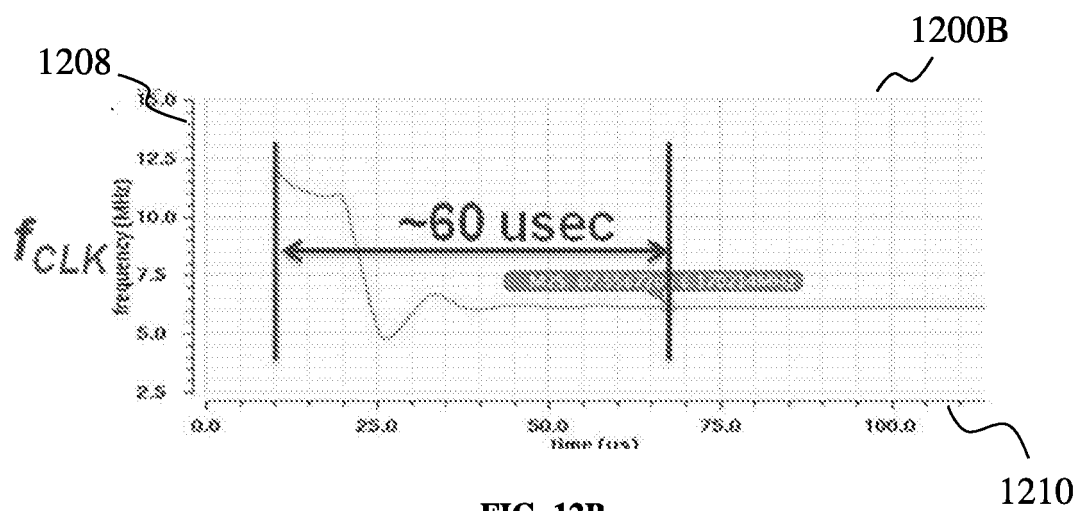


FIG. 12B

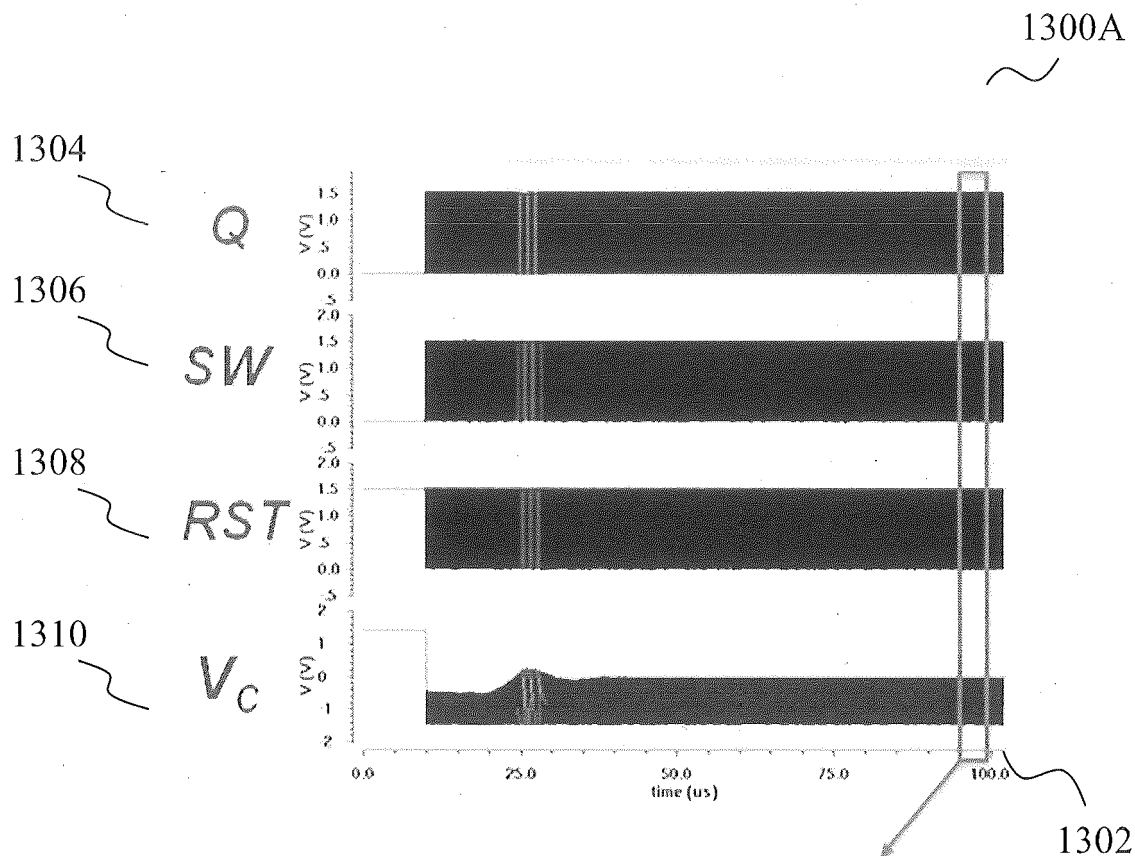


FIG. 13A

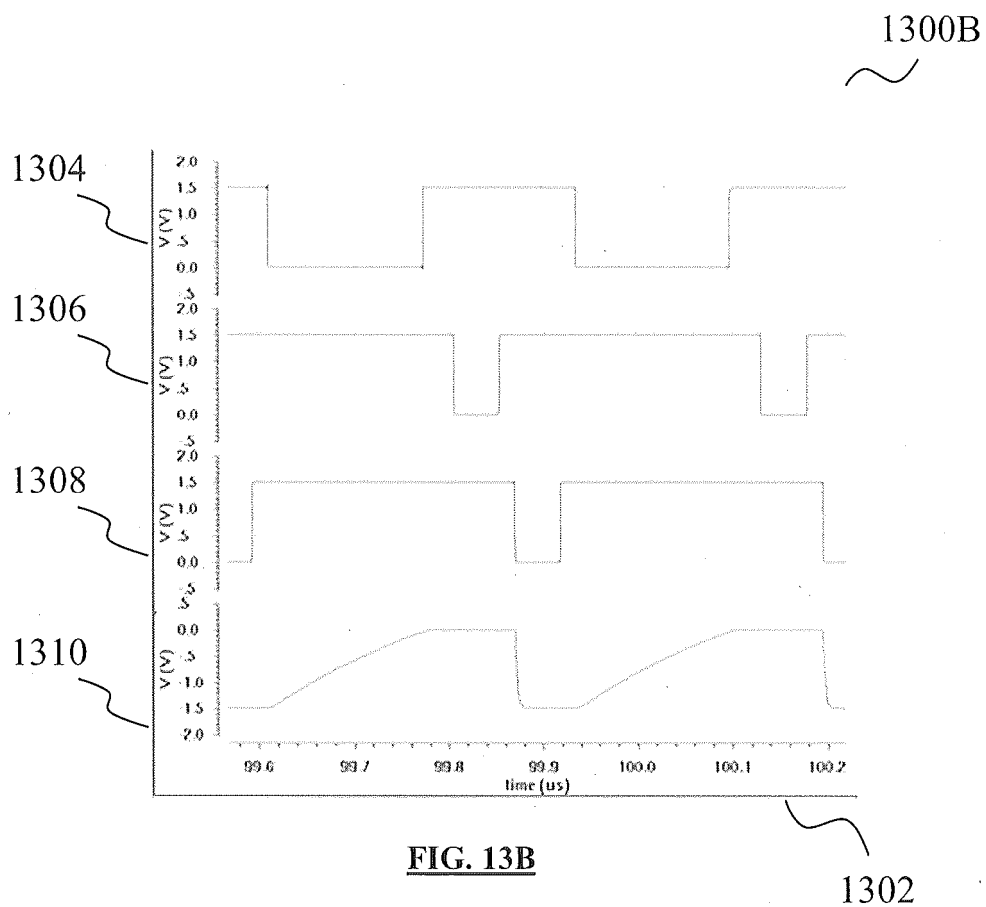


FIG. 13B

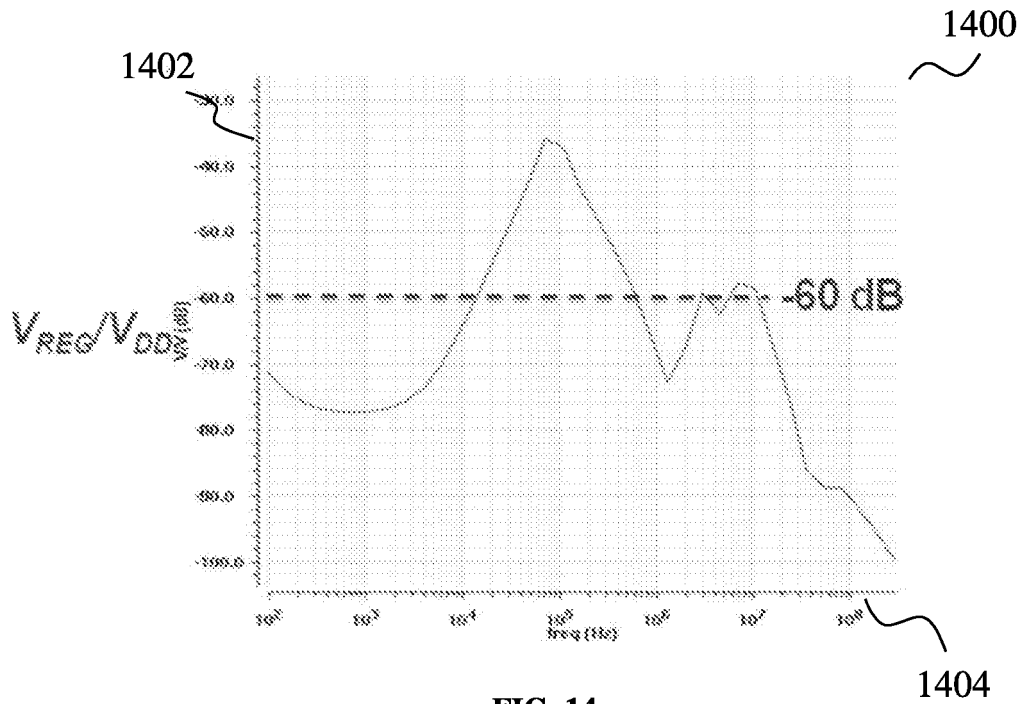


FIG. 14

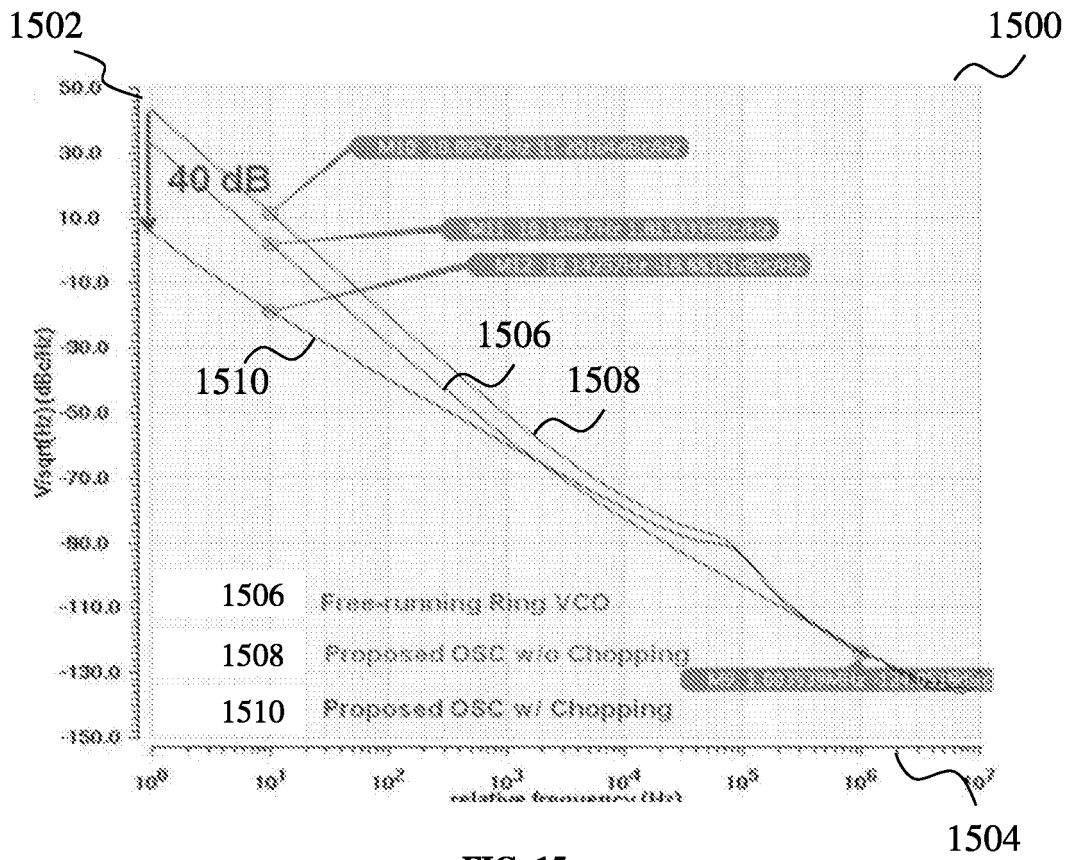


FIG. 15

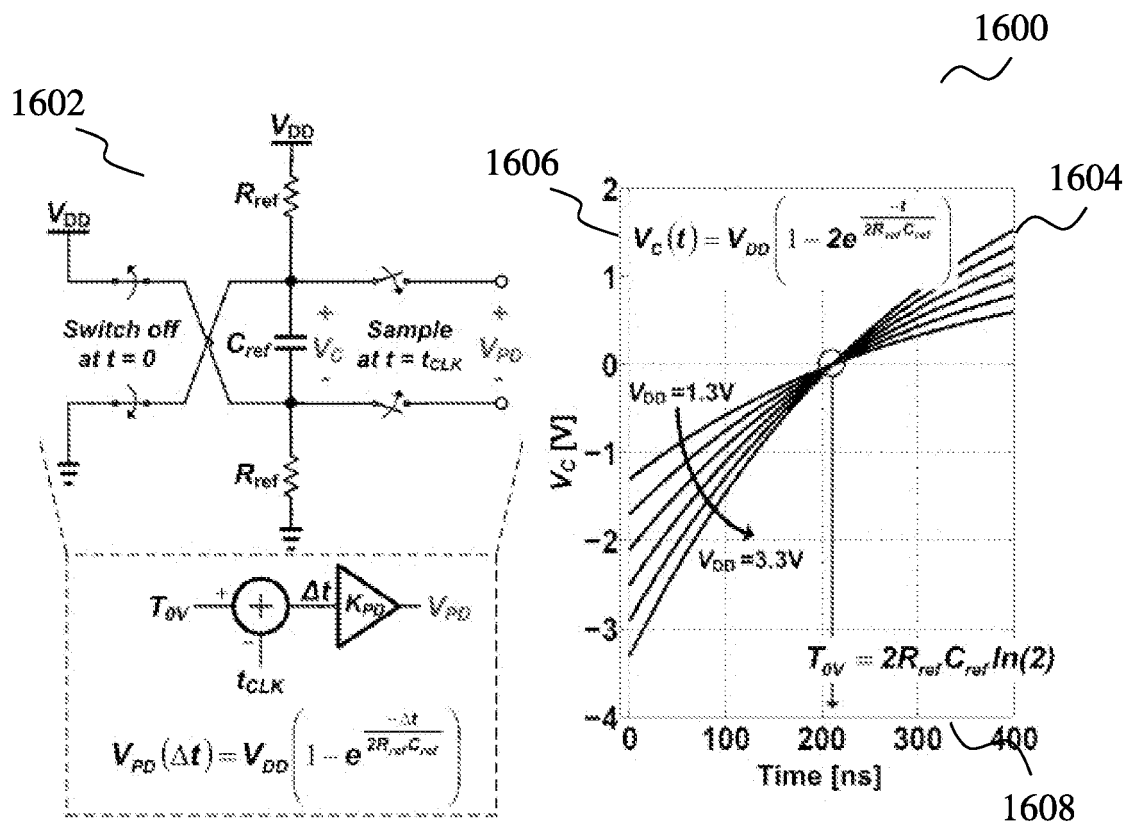


FIG. 16

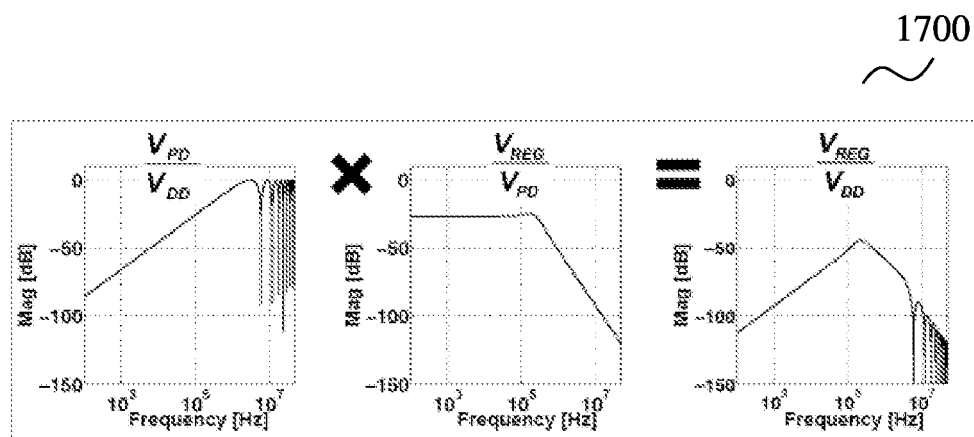
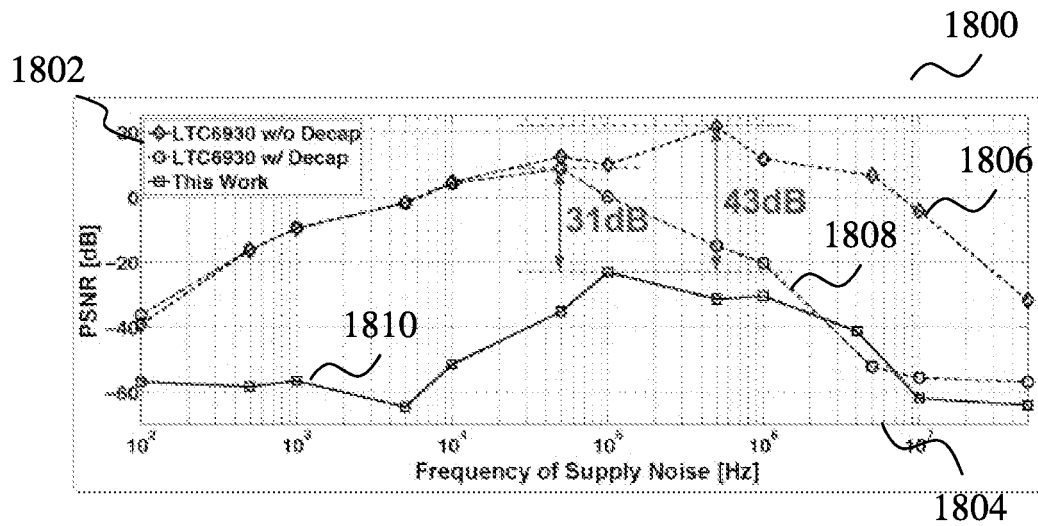
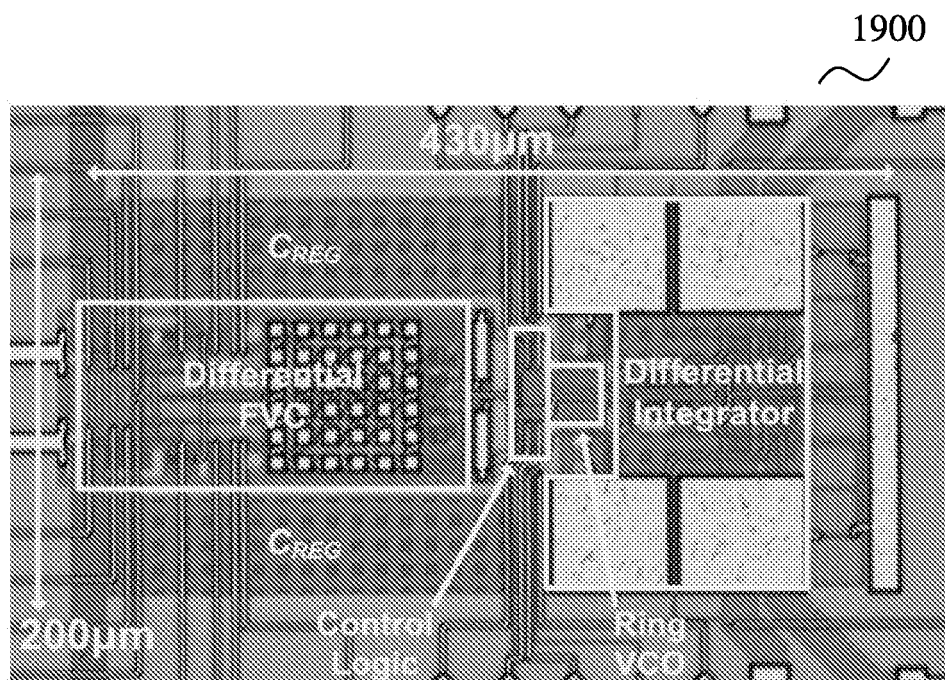
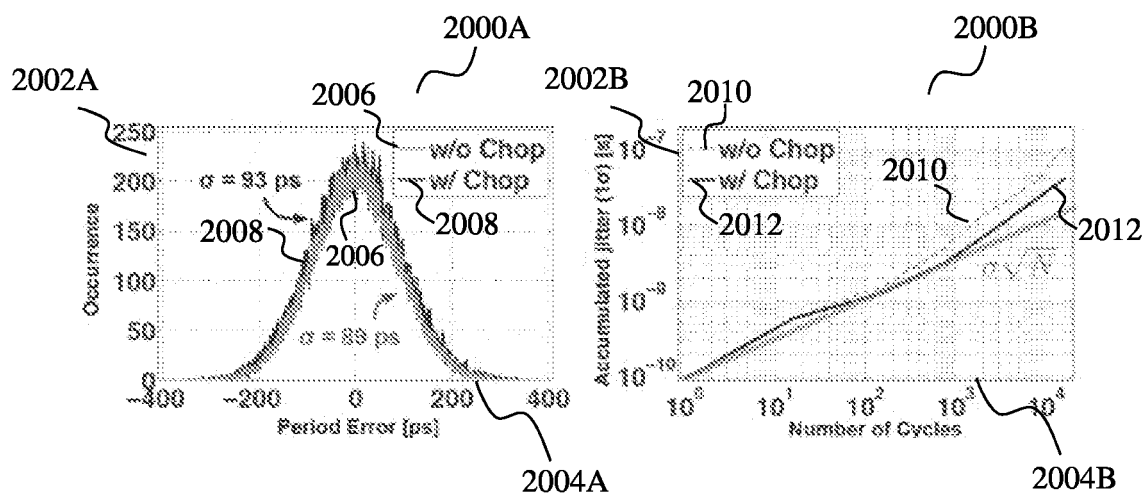
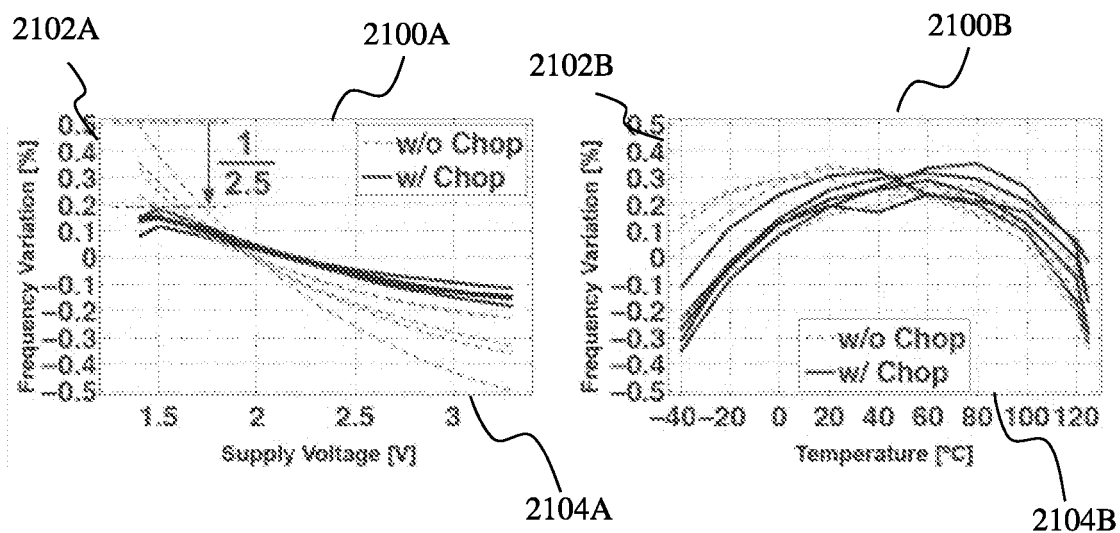


FIG. 17

**FIG. 18****FIG. 19**

**FIG. 20****FIG. 21**

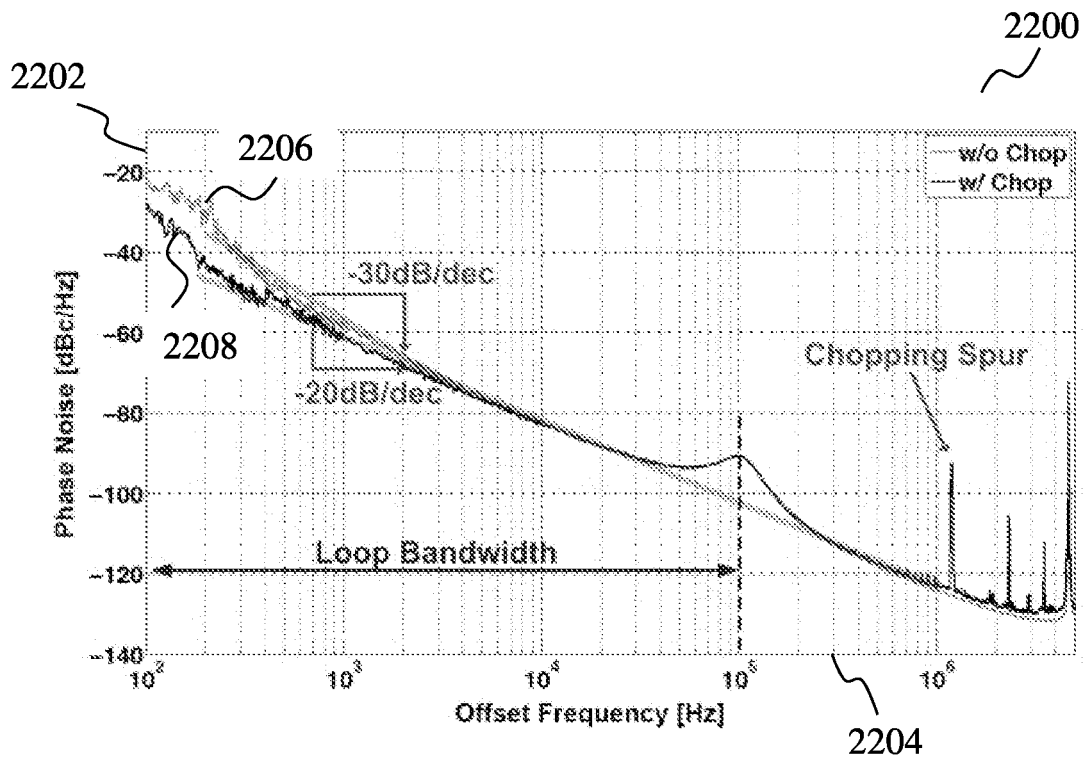


FIG. 22

Parameters	JSSC 2010 [1]	ISSCC 2009 [2]	ISSCC 2013 [3]	LTC6930 [4]	This Work
Technology [nm CMOS]	180	130	65	N/A	180
Decoupling Capacitor	N/A	N/A	N/A	Needed (100nF)	None
Supply Regulator	None	None	None	Needed	None
Frequency [MHz]	14	3.2	12.6	5	4.7
Area [mm ²]	0.04 (Core)	0.073 (Core)	0.01 (Core)	N/A	0.086 (Overall)
Min. V _{DD} [V]	1.7	1.4	1.1	1.7	1.4
Power [μW]	45	38	98.4	340	53
Period RMS Jitter [%]	0.04	0.14	~0.07	0.11	0.04
Worst-Case PSNR [dB]	N/A	N/A	N/A	9 ¹	-22
Freq. Variation [%] to V _{DD}	±0.16 @1.7 to 1.9V	±0.4 @1.4 to 1.6V	±0.07 @1.1 to 1.5V	±0.1 @1.7 to 3.7V	<±0.2 @1.4 to 3.3V
Freq. Variation [%] to Temp.	±0.19 ² @-40 to 125°C	±0.25 @20 to 60°C	±0.82 @0 to 80°C	<±0.6 @-40 to 125°C	<±0.35 @-40 to 125°C
Samples	1	1	1	Commercial Product	5

¹ With a decoupling capacitor of 0.1μF² With a temperature compensation voltage

FIG. 23