A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

The present invention relates to a semiconductor integrated circuit device, and more particularly to a technique which renders the density of integration of input and output buffers higher in a master slice type semiconductor integrated circuit device and which is accordingly effective for increasing the number of pins and reducing the size of a chip and further for enhancing the functions of the chip.

A semiconductor integrated circuit device (IC) requires input and output buffers for interfacing with the exterior. As shown in Fig. 1 of the accompanying drawings, input or output buffers 4 are located between a plurality of bonding pads 2 which are arranged in the peripheral edge of a chip (pellet) 1 and an internal circuit 3 which is located centrally of the chip 1.

In a gate array type or master slice type semiconductor integrated circuit device in which a desired logic circuit can be freely fabricated as the internal circuit by a wiring step, the input and output functions of the bonding pads need to be selected at will in accordance with the design of the internal circuit. To this end, various devices are used for the buffers.

Fig. 2 of the accompanying drawings shows an

example of the device. The buffers 4 are provided in correspondence with the bonding pads 2. In each of the buffers 4, circuit elements 5 which form the input buffer and circuit elements 6 which form the output buffer are arranged. In accordance with the design of the internal circuit 3, either the input or output circuit elements within the buffer 4 are selected and are connected to the bonding pad 2 as well as the internal circuit 3. Thus, the buffer 4 can be constructed as either the input or the output buffer, and the bonding pad 2 can be constructed as either an input terminal or an output terminal.

With the above arrangement, however, both the input and output circuit elements 5 and 6 must be formed in each buffer 4. Therefore, the occupying area per buffer becomes large. Since the large sized buffers are arrayed in the peripheral edge of the chip, an increase in the number of the bonding pads 2 (the number of the pins) is limited. On the other hand, when the number of the bonding pads is increased, the chip size must be increased accordingly.

In order to solve this problem, an example in which the number of the bonding pads 2 is approximately double that in the above example is shown in Fig. 3 of the accompanying drawings. This example has been proposed in Japanese Patent Publication No. 211248/82

Both the input buffer and the output buffer can be constructed of one buffer 4, and two bonding pads 2A, 2B are provided for each buffer. Thus,the input buffer and the output buffer can be connected to the pins and function independently of each other.

We have found that although the improved arrangement can afford the two functions of inputting and outputting independently of each other by the use of the single buffer, the functions of the respective bonding pads 2A, 2B are fixed either to the inputting (for example, 2A) or to the outputting (for example, 2B). This leads to problems as stated below. The allotment of the inputting and outputting functions to the respective pads 2 as the signal pins becomes less versatile, and accordingly the versatility of the selection of the functions is reduced. Moreover, although the total number of the pads 2A and 2B increases, the number of the inputting or outputting pads is limited to about one half of the total number mentioned above. For this reason, in the case of the application to the kind of circuit in which the numbers of input signals and output signals do not balance and either is much larger, as is usual in a logic circuit employed in a gate array LSI, the substantial number of pads is not greatly different from the number of pads of the foregoing arrangement in Fig. 2, and it is

difficult to achieve the purposes of increasing the number of pads and reducing the chip size.

It is an object of the present invention to provide a semiconductor integrated circuit device which can increase the numbers of input and output pins while reducing the chip size and which can enhance pin functions and other chip functions.

It is another object of the present invention to provide a semicondcutor integrated circuit device which can set input buffers and output buffers at any desired positions and in a number approximately double that in previously known arrangements.

According to the present invention there is provided a semiconductor integrated circuit device including:

(a) a semiconductor substrate;

(b) a plurality of identical unit cells on the substrate, except for the wiring patterns, each unit cell having two regions, each region having a plurality of components including MISFETs;

(c) a bonding pad associated with each unit cell;

(d) wiring leads for each unit cell interconnecting at least some of the components of that unit cell, and including an interconnection to the bonding pad associated with that cell, the wiring leads interconnecting said at least some of the components of the unit cells so that each unit cell forms either an input circuit or an output circuit, wherein at least one first MISFET in a first unit cell forms an input circuit and at least one first MISFET in a second unit cell forms an output circuit.

The MISFETs of each region of each cell may include a first group of MISFETs connected in parallel. The first group of MISFETs may comprise at least two or three MISFETs.

The first group of MISFETs in a first region

may comprise n-channel MISFETs, and the first group of MISFETs in a second region may comprise p-channel MISFETs.

In each region the MISFETs of the first group of MISFETs may have gate electrodes of substantially the same shape, which may also be parallel to each other.

The MISFETs of the first group in each region may share source or drain regions with adjacent MISFETs in that region and may have substantially equal channel lengths and equal channel widths.

The first group of MISFETs of a unit cell forming an input circuit may form the at least one first MISFET of that unit cell, and the first group of MISFETs of a unit cell forming an output circuit may form the corresponding at least one first MISFET of that cell.

In each region a second group consisting of at least two or three MISFETs may be connected in parallel.

The MISFETs of the second group in a first region may comprise n-channel MISFETs, and the second group of MISFETs in a second region may comprise p-channel MISFETs.

The MISFETs of the second group may have gate electrodes of substantially the same shape.

The shape of the gate electrodes of the MISFETs of the first and second groups is the same.

The gate electrodes of the MISFETs of the second group may be arranged in parallel to each other.

The gate electrodes of the MISFETs of the group may be perpendicular to the gate electrodes of the MISFETs of the second group.

The MISFETs of the second group may have substantially equal channel lengths and gate widths.

The gate widths of the MISFETs of the second group may be less than the gate widths of the MISFETs of the first group.

A further MISFET may be provided in each region, each additional MISFET having a gate width which is less than the gate width of the MISFETs of the first group in a respective region.

The additional MISFET in the first region may be an n-channel MISFET and the additional MISFET in the second region may be a p-channel MISFET.

The at least one first MISFET in a unit cell forming an input circuit may be a protective

MISFET connected to at least one further MISFET of that unit cell, the gate electrode of the at least one further MISFET being connected to the bonding pad associated with the unit cell for receiving a signal from the bonding pad.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein:

Figs. 4A and 4B are respectively a plan view and a partial enlarged view of a preferred embodiment of a semiconductor integrated circuit device;

Fig. 5 is an enlarged plan view of a buffer portion;

Fig. 6 is an enlarged sectional view taken along line Vi-Vi in Fig. 5;

Fig. 7A is a plan view of the state in which a buffer is constructed as an input buffer, whilst Fig. 7B is an equivalent circuit diagram thereof; and

Fig. 8A is a plan view of the state in which the buffer is constructed as an output buffer, whilst Fig. 8B is an equivalent circuit diagram thereof.

Referring to Figs. 4A to 8B in which the present invention is applied to a master slice type LSI composed of complementary MISFETs.

The semiconductor integrated circuit device 10 is constructed on a substantially square chip (pellet) as generally shown in Fig. 4A. In the central part of the chip, a large number of MISFETs (MIS field effect transistors) of the p-channel and n-channel are formed as the circuit elements of a logic circuit portion 11. In the peripheral edge of the chip, a plurality of buffers 12 and bonding pads 13 corresponding

thereto are arrayed. The buffer 12 is a circuit portion for which any of a plurality of different input or output circuit functions can be selected by altering the wiring pattern thereof. Besides, it is a unit cell for forming an input or output circuit. Such unit cells have the same pattern except the wiring patterns, and are repeatedly arranged. In the illustrated state, no wiring is performed for the circuit elements of the logic circuit portion 11 or the buffers 12 or between the bonding pads 13 and the buffers 12. The required number of logic circuits and input and output circuits can be fabricated by providing the necessary wiring during the step of wiring.

As seen from a partial enlarged view of the peripheral edge portion in Fig. 4B, circuit elements 7 within the buffers 12 are indistinguishably formed so as to be usable when either input buffers or output buffers are to be constructed.

Since input elements and output elements need not be provided individually in respectively required numbers, the occupying area of the buffer 12 can be reduced to about one half of that of the buffer 4. As shown in Fig. 4A, the bonding pads 13 which are about double in number as compared with those in the example of Fig. 2 and are substantially

equal in number to those in the example of Fig. 3 are arrayed and formed in the peripheral edge of the chip 10. Inside the bonding pads 13, the buffers 12 are formed individually with one buffer 12 corresponding to one bonding pad 13.

Regarding the example of Fig. 2, since the occupying area of the buffer 12 is rendered about one half of that of the buffer 4, it is permitted to provide the buffers 12 and the bonding pads 13 numbering approximately double on a chip of equal area. The buffer 12 can have its function set at will as the input or output buffer. As to the design of the input and output portions, accordingly, the present embodiment is approximately twice as versatile as that of the example of Fig. 2.

Regarding the example of Fig. 3, the numbers of the bonding pads are equal, but the function of each bonding pad can be set for inputting or outputting at will. This is based on the fact that, by reducing the area of each buffer to one half, the functions of the buffers can be set for inputting or outputting at will in correspondence with the individual bonding pads. In the example of Fig. 3, the functions are half fixed, for instance, the bonding pads 2A are used for inputting while those pads 2B are used for outputting. As to the design of the input and output

portions, accordingly, the present embodiment is approximately twice as versatile as the example of Fig. 3.

The buffer 12 is shown on enlarged scale in Fig. 5, and its section taken along line VI-VI in Fig. 5 is shown in Fig. 6. The buffer 12 is constructed of two regions 14 and 15. The first region 14 shown on the right hand side consists of p-channel MOSFETs (hereinafter referred to as a "pMOSFET" region) whilst the second region 15 shown on the left hand side consists of n-channel MOSFETs (hereinafter referred to as a "nMOSFET" region). Circuit elements made of the respective MISFETs are formed in each region. The plurality of p-MOSFETs are formed in an n-type silicon semiconductor substrate 16 in the region 14 of the buffer 12, while the plurality of nMOSFETs are formed in a p-type well region 17 formed in the region 15.

The pMOSFETs of the pMOSFET region 14 are provided as follows. A first group of pMOSFETs 20 consist of six series-connected pMOSFETs which are constructed of six polycrystalline silicon gate electrodes 18 arranged in parallel and p^+-type source or drain regions 19 formed in self-alignment to these gates 18, and each of which has its gate width set at 78 μm. A second group of pMOSFETs 23 consist of five pMOSFETs which are constructed of five polycrystalline silicon gate electrodes 21 of p+-type source or drain regions 22 formed in self-alignment thereto, and each of which has a gate width of 20 μm. A third pMOSFET 26

is formed with p^+-type source or drain regions 25 in self-alignment to a single gate electrode 24 of polycrystalline silicon, and has its gate width set at 7 μm.

On the other hand, the nMOSFET region 15 is formed with a first group of nMOSFETs 27, a second group of nMOSFETs 28 and a third nMOSFET 29 substantially in line symmetry to the pMOSFET region 14. More specifically, as shown in Fig. 6, the first group of nMOSFETs 27 include six series-connected nMOSFETs which are constructed of six polycrystalline silicon gate electrodes 30 formed in parallel, and n^+-type source or drain regions 31 formed in self-alignment thereto, the gate width of each of the nMOSFETs being set at 78 μm. The second group of nMOSFETs 28 consist of five nMOSFETs which are constructed of five polycrystalline silicon gate electrodes 32 and n^+-type source or drain regions 33 formed in sel-alignment thereto, and each of which has its gate width set at 20 μm. The third nMOSFET 29 is constructed of a polycrystalline silicon gate electrode 34 and n^+-type source and drain layers 35 formed in self-alignment thereto, and has its gate width set at 35 μm.

The second group of pMOSFETs 23 and the second group of nMOSFETs 28 are formed in such a manner

that every two elements are isolated and that parts thereof and the third pMOSFET 26 and nMOSFET 29 are unitarily constructed respectively. The reason is that any logic layout can be readily organised with the arrangement. It is also the reason that an inverter which is very often used in the input buffer or output buffer is readily constructed as an inverter having any desired gate width. Referring to Fig. 6, the buffer portion includes SiO_2 film 36 a phosphosilicate glass (PSG) film 37, and a thick SiO_2 film 38 formed by the local oxidation of the substrate surface.

According to the above construction, when aluminium (Al) wiring leads are formed on the buffer 12 in the wiring step, this buffer can be constructed either as an input buffer or an output buffer in accordance with the wiring pattern.

Figs. 7A and 7B show the state in which the buffer 12 is formed as an input buffer. Marks x in the drawing denote the connections between the respective regions (the same holds true hereinbelow).

A wiring lead 38 connected to the bonding pad 13 is connected to n^+-type semiconductor layers 31a which serve as one-side electrodes for causing the currents of the first group of nMOSFETs 27 to flow. The gates 30, and semiconductor layers 31b which serve as the other-side electrodes for causing

the currents of the MOSFETs to flow are connected to earth potential G as a reference potential. The six MOSFETs have all their gates, sources and drains connected in parallel respectively, whereby they become, in effect, a MOSFET which has a gate width of 468 (= 78μm x 6) μm and which is formed as a clamping diode D. The diode D serves to prevent the destruction of the MOSFETs whose gate electrodes are supplied with a signal from the bonding pad 13. That is, this MOSFET is a protective MOSFET for preventing the destruction of the other MOSFETs. An input protective resistor R which is made of a polycrystalline silicon film in similar manner to the gate electrode is arranged between the bonding pad 13 and the clamping diode D.

A wiring lead 39 connects the third nMOSFET 29 and the third pMOSFET 26, to form a first-stage CMOS inverter I_{1i}. One MOSFET is selected from each of the second group of nMOSFETs 28 and the second group of pMOSFETs 23 so as to form a second-stage CMOS inverter I_{2i} in which the respective MOSFETs have gate widths of 20 μm. A third-stage CMOS inverter I_{3i} is formed in similar manner. Three MOSFETs are selected from the second group of nMOSFETs 28, and are connected in parallel. Three MOSFETs are selected

from the group of pMOSFETs 23, and are connected in parallel. Each of the parallel connections of the MOSFETs is regarded as one MOSFET having a gate width of 60 (= 20 μm x 3) μm, and a final-stage CMOS inverter I_{Fi} is formed by the use of these parallel connections. The output of the final-stage inverter I_{Fi} is connected to the internal circuit portion 11 by a wiring lead 40. In Fig. 7A, a wiring lead 41 is provided for connection to earth, and a wiring lead 42 is provided for connection of a power source potential (V_{CC}).

The input buffer thus formed is shown in Fig. 7B. Excess current is clamped by the large clamping diode D having the gate width of 468 μm. A signal level is adjusted, that is, a logic threshold voltage is adjusted by the respective gate widths 35 μm and 7 μm of the nMOSFET 29 and pMOSFET 26 of the first-stage inverter I_{1i}. Thus, the input signal from a TTL is suited to the CMOS device. The input signal is waveshaped by the second and third stages of CMOS inverters I_{2i} and I_{3i}, and is thereafter amplified by the final stage of CMOS inverter I_{Fi}. The output of the buffer is connected to the internal circuit portion 11 by the wiring lead 40. The input buffer does not use the first group of pMOSFETs 20.

Figs. 8A and 8B show the state in which the buffer 12 is formed as the output buffer.

A wiring lead 43 connected to the internal circuit 11 connects one MOSFET selected from each of the second group of nMOSFETs 28 and the second group of pMOSFETs 23, to form a first-stage CMOS inverter I_{10} in which the gate widths of the respective MOSFETs are 20 μm. Two MOSFETs are selected from the group of MOSFETs 28, and are connected in parallel. Two MOSFETs are selected from the group of MOSFETs 23, and are connected in parallel. Each of the parallel connections of the MOSFETs is, in effect, deemed one MOSFET having a gate width of 40 μm, and a second-stage CMOS inverter I_{20} is formed by the use of these parallel connections. All the MOSFETs of the first groups of nMOSFETs 27 and pMOSFETs 20 are connected in parallel respectively. Each of the parallel connections is deemed one MOSFET having a gate width of 468 μm, and a final-stage CMOS inverter I_{Fo} for driving an external circuit is formed by the use of these parallel connections. The third nMOSFET 29 and pMOSFET 26 are not used. In Figs. 8A and 8B, a wiring lead 44 is provided for connection to earth, a wiring lead 45 for connection to the power source potential (V_{CC}), and a wiring lead 46 for connection to the bonding pad 13 as an output line.

The output buffer thus formed is shown in Fig. 8B. An output signal from the internal circuit portion 11 waveshaped and amplified by the first stage and second stage of CMOS inverters I_{10}, I_{20} is greatly amplified by the final stage of CMOS inverter I_{FO}, and the amplified signal is supplied to the bonding pad 13 and delivered to the exterior so as to drive an external circuit.

All the buffers 12 shown in Figs. 4A and 4B have the arrangement shown in Fig. 5. Accordingly, any of the buffers 12 can be set as either the input buffer or the output buffer at will, and the bonding pad 13 can be set as either the input pin or the output pin.

With the semiconductor device (chip) of the above construction, accordingly, the respective elements of the first, second and third nMOSFETs 27, 28, 29 and pMOSFETs 20, 23, 26 in the buffer 12 can be utilised as the inputting or outputting elements merely by altering their connections with different wiring patterns, and the entire buffer 12 can be set for either inputting or outputting at will. Thus, the buffer 12 can have its occupying area reduced by omitting the elements to the extent that they can be used for both inputting and outputting. Accordingly

the density of arranging the buffers on the chip 10 is enchanced, and increases in the number of buffers and the number of bonding pads (the number of pins) corresponding thereto can also be increased. Conversely, when the number of buffers is held equal, reduction in the chip size can be achieved.

Meanwhile, since the buffer 12 can be set for either inputting or outputting at will, the bonding pad 13 can be freely set as either the input terminal or the output terminal. Accordingly, even in the kind of a circuit device in which only input signals or output signals are large in number, the number of bonding pads can be caused to correspond thereto, and moeover, the arrangement of the input and output terminals is as desired. Thus, the versatility of the design of the terminal functions or the functions of the whole chip can be enhanced. By the way, the versatility of setting the pin functions can be rendered double or even higher than that in the prior art device shown in Fig. 2 or Fig. 3.

According to the foregoing construction, a clock receiving buffer can also be formed in such a way that two of the buffers 12, 12 are used between which wiring utilizing the elements is laid. A bi-directional buffer may well be constructed.

The above described embodiment has the following advantages.

Since elements in a buffer can be utilized for either inputting or outputting by altering the wiring, the buffer can be set as either an input buffer or an output buffer at will. Therefore, a bonding pad provided in correspondence with the buffer can be enhanced in pin versatility for inputting and outputting, and the versatility of design as the whole chip can be enhanced.

Since the same elements in the buffer can be utilized for both inputting and outputting, the number of required elements can be decreased to that extent. Thus, the occupying area of one buffer is reduced, so that the number of buffers or the number of bonding pads which can be formed on an identical chip can be increased.

Since the occupying area of one buffer can be reduced, the chip size can be reduced in the case of an equal number of pins. By the way, in a CMOS master slice on the scale of 1000 - 2000 gates, it is the actual situation that the chip size is determined by the numbers of input and output buffers.

The buffer can be set for either inputting or outputting, while at the same time, an increase

in the number of pins (the number of bonding pads) can be realised owing to the reduced occupying area of the buffer. Especially in a semiconductor integrated circuit device in which the numbers of input signals and output signals do not balance and either number is much larger, the versatility of design is high.

Since the buffer is formed into a CMOS structure, the power consumption of the buffer can be reduced.

Since the buffer is formed by a plurality of MISFETs of unit gate width, a MISFET of desired gate width or various circuits employing such MISFETs can be formed in accordance with the connection number of the elements, and the versatility of the circuit of the input or output buffer can be enhanced.

Since either a clamping MOSFET requiring a large area in the input buffer or an external circuit driving MOSFET requiring a large area in the output buffer is formed by the same MOSFET, the buffer area can be substantially reduced.

The following modifications are possible:

(a) the buffer need not be formed of CMOS transistors, but can be formed only of pMOSFETs or preferably nMOSFETs.

(b) the pattern configuration of elements (MISFETs) within the buffer or the number of gates and the gate widths thereof and further the circuits of input and output buffers formed by wiring can be freely designed in a manner other than that shown.

(c) an internal circuit can be designed either by the master slice method or exclusively, (a) the elements can be formed of bipolar transistors.

Whilst the invention has been described in relation to the application to a CMOS logic master slice LSI, it is not restricted thereto but is applicable to general semiconductor devices having input and output buffers.

CLAIMS.

1. A semiconductor integrated circuit device including:

(a) a semiconductor substrate;

(b) a plurality of identical unit cells on the substrate, except for the wiring patterns, each unit cell having two regions, each region having a plurality of components including MISFETs;

(c) a bonding pad associated with each unit cell;

(d) wiring leads for each unit cell interconnecting at least some of the components of that unit cell, and including an interconnection to the bonding pad associated with that cell, the wiring leads interconnecting said at least some of the components of the unit cells so that each unit cell forms either an input circuit or an output circuit, wherein at least one first MISFET in a first unit cell forms an input circuit and at least one first MISFET in a second unit cell forms an output circuit.

2. A device according to claim 1, wherein the MISFETs of each region of each cell include a first group of MISFETs connected in parallel.

3. A device according to claim 2, wherein in each region, the first group of MISFETs comprises at least two MISFETs.

4. A device according to claim 2 or claim 3, wherein in each region the first group of MISFETs comprises at least three MISFETs.

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5. A device according to any one of claims 2 tc 4, wherein the first group of MISFETs in a first region comprise n-channel MISFETs, and the first group of MISFETs in a second region comprise p-channel MISFETs.

6. A device according to any one of claims 2 to 5, wherein in each region the MISFETs of the first group of MISFETs have gate electrodes of substantially the same shape.

7. A device according to any one of claims 2 to 6, wherein in each region, the gate electrodes of the MISFETs of the first group are parallel to each other.

8. A device according to any one of claims 2 to 7, wherein the MISFETs of the first group in each region share source or drain regions with adjacent MISFETs in that region.

9. A device according to any one of claims 2 to 8, wherein in each region, the MISFETs of the first group have substantially equal channel lengths.

10. A device according to any one of claims 2 to 9, wherein in each region, the MISFETs of the first group have substantially equal channel widths.

11. A device according to any one of claims 2 to 10, wherein the first group of MISFETs of a unit cell forming an input circuit form the at least one first MISFET of that unit cell, and the first group of MISFETs of a unit cell forming an output circuit form the corresponding at least one first MISFET of that cell.

12. A device according to any one of claims 2 to 11, including in each region a second group of MISFETs connected in parallel.

13. A device according to claim 12, wherein the MISFETs of the second group in a first region comprise n-channel MISFETs, and the second group of MISFETs in a second region comprise p-channel MISFETs.

14. A device according to claim 12 or claim 13, wherein in each region, the second group consists of at least two MISFETs.

15. A device according to claim 14, wherein in each region, the second group consists of at least three MISFETs.

16. A device according to any one of claims 12 to 15, wherein in each region, the MISFETs of the second group have gate electrodes of substantially the same shape.

17. A device according to claim 16, as dependant on claim 6, wherein in each region, the shape of the gate electrodes of the MISFETs of the first and second groups is the same.

18. A device according to any one of claims 12 to 17, wherein in each region, the gate electrodes of the MISFETs of the second group are parallel to each other.

19. A device according to claim 18 as dependant on claim 7, wherein in each region, the gate electrodes of the MISFETs of the first group are perpendicular to the gate electrodes of the MISFETs of the second group.

20. A device according to any one of claims 12 to 19, wherein in each region, the MISFETs of the second group have substantially equal channel lengths.

21. A device according to any one of claims 12 to 20, wherein in each region, the MISFETs of the second group have substantially equal gate widths.

22. A device according to claim 21, wherein in each region, the gate widths of the MISFETs of the second group are less than the gate widths of the MISFETs of the first group.

23. A device according to any one of claims 12 to 22, having in addition a further MISFET in each region, each additional MISFET having a gate width which is less than the gate width of the MISFETs of the first group in a respective region.

24. A device according to claim 23, wherein the additional MISFET in the first region is an n-channel MISFET and the additional MISFET in the second region is a p-channel MISFET.

25. A device according to any one of the preceding claims, wherein the at least one first MISFET in a unit cell forming an input circuit is a protective MISFET connected to at least one further MISFET of that unit cell, the gate electrode of the at least one further MISFET being connected to the bonding pad associated with the unit cell for receiving a signal from the bonding pad.

26. A device according to claim 25 as dependant on claim 12, wherein the MISFETs of the second group of MISFETs comprise the at least one further MISFET.

27. A device according to claim 1, wherein the first MISFET in the first unit cell is used to form a protective MISFET and the first MISFET in the second unit cell is used to form an inverter.

28. A semiconductor integrated circuit device substantially as herein described with reference to and as illustrated in Figures 4A to 8B of the accompanying drawings.
