

ABSTRACT

Disclosed are a semiconductor memory device, a controller, and a memory system.

The semiconductor memory device includes a memory cell array including a plurality of
5 memory cells, and an error correcting code (ECC) decoder configured to receive first data
and a parity output from selected memory cells of the memory cell array. The ECC
decoder generates a syndrome based on the first data and the parity, generates a decoding
status flag (DSF) indicating a type of an error of the first data by the syndrome, and
outputs the second data and the DSF to an external device outside of the semiconductor
10 memory device when a read operation of the semiconductor memory device is performed.

FIG. 1