or semiconductor packages 166.

In FIG. 5e, ~~shows~~ semiconductor die 170, similar to semiconductor die 124 from FIG. 4c, ~~that~~ include a back surface 172 and an active surface 174 opposite the back surface. Active surface 174 includes contact pads 176 and an insulating or passivation layer 180 conformally applied over the active surface using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. Insulating layer 180 contains one or more layers of silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), or other material having similar insulating and structural properties. A portion of insulating layer 180 is removed by laser direct ablation (LDA) using laser 181, etching, or other process to form openings 182 in insulating layer 180 to expose contact pads 176. Semiconductor die 170 are mounted to substrate 144 with back surface 172 oriented toward second surface 148 of substrate 144 and with active surface 174 oriented away from substrate 144.

Before semiconductor die 170 are mounted to substrate 144, the semiconductor die optionally undergo a backgrinding process with polishing to remove bulk semiconductor material from back surface 172 to reduce a thickness of the semiconductor die. After backgrinding and optional polishing, a die attach tape or adhesive 178 is disposed over back surface 172 of semiconductor die 170 before the semiconductor die are singulated. Alternatively, die attach tape or adhesive 178 is disposed over back surface 172 of semiconductor die 170 after the semiconductor die are singulated. Semiconductor die 170 are mounted to substrate 144 using a pick and place operation in which proper alignment of the semiconductor die on the substrate is facilitated by the presence of fiducial alignment marks on

the substrate of BGA packages 166. Semiconductor die 170 are individually mounted to substrate 144, or alternatively, are mounted to the substrate at a strip level. Semiconductor die 170 are mounted to second surface 148 of substrate 144 with a plurality of bumps 164 laterally offset and disposed around a periphery of mounted semiconductor die 170. In one embodiment, semiconductor die 170 have an area or footprint larger than an area or footprint of semiconductor die 124 such that semiconductor die 124 are disposed within a footprint of semiconductor die 170 over second surface 148 of substrate 144. Alternatively, semiconductor die 170 have an area or footprint equal to or smaller than an area or footprint of semiconductor die 124.

After semiconductor die 170 are mounted to substrate 144, B-stage curing can be applied to semiconductor die 170 and BGA packages 166 to further cure die attach tape or adhesive 178. Additionally, an optimized annealing process may be applied to semiconductor die 170 after the semiconductor die have been mounted to substrate 144 in order to control warpage and maintain acceptable planarity of BGA package 166.

In FIG. 5f, similar to FIG. 5e, ~~shows~~ semiconductor die 170 are mounted to substrate 144 with back surface 172 oriented toward second surface 148 of substrate 144. Rather than showing die attach tape or adhesive 178 initially disposed over back surface 172 of semiconductor die 170 as in FIG. 5e, FIG. 5f shows die attach adhesive 190 ~~is~~ initially disposed over and contacts substrate 144 while being separate from semiconductor die 170. As a bare semiconductor die 170, i.e., without a die attach adhesive, is mounted to substrate 144, adhesive 190 comes in contact with back surface 172 of the semiconductor die as well as side surfaces of the semiconductor

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die that extend
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between back surface 172 and active surface 174.

In FIG. 5g, ~~shows~~ semiconductor die 170 are mounted to BGA packages 166 to form SoP packages 196. SoP packages 196 are singulated through substrate 144, through encapsulant 160, and between bumps 164, semiconductor die 124, and semiconductor die 170 of BGA packages 166 using a saw blade or laser cutting tool 198 to form individual SoP packages 196.

In FIG. 5h, similar to FIGs. 5e-5g, ~~shows~~ semiconductor die 170 are mounted to substrate 144 with back surface 172 oriented toward second surface 148 of substrate 144. Rather than showing semiconductor die 170 being mounted to unsingulated substrate 144 as in FIGs. 5e and 5f, FIG. 5h shows semiconductor die 170 ~~are~~ mounted to substrate 144 opposite semiconductor die 124 after bumps 164 have been mounted to the substrate and after the substrate has been singulated as described above in FIG. 5g. Semiconductor die 170 are mounted to singulated BGA packages 166 either with die attach tape or adhesive 178 initially disposed over back surface 172 of semiconductor die 170 as shown in FIG. 5e, or with die attach adhesive 190 initially disposed over and contacting substrate 144 as shown in FIG. 5f. By mounting semiconductor die 170 to singulated BGA packages 166, the BGA packages can be tested before attachment of the semiconductor die such that the semiconductor die are only mounted to known good BGA packages 166, thereby increasing ~~a~~the yield of SoP packages 196.

FIG. 5i shows a cross sectional view of a portion of temporary substrate or carrier 200 containing sacrificial or recyclable base material such as silicon, steel, polymer, beryllium oxide, or other suitable low-cost, rigid material for structural support. An interface layer or carrier tape 202 is formed or laminated over carrier 200 as a temporary adhesive

Similarly, a portion of semiconductor die 170 including, e.g., insulating layer 180 and contact pads 176 are also deposited within, and surrounded by, a thickness of releasable layer 204 or a single layer of carrier tape or adhesive.

FIG. 5j shows a plan or top view of SoP packages 196 mounted to carrier 200 with thermally releasable layer 204 as described in FIG. 5i. Gaps 206 are disposed around a periphery of SoP packages 196 and are disposed between adjacent SoP packages. FIG. 5j also shows an intersection 208 between two gaps 206 that is formed at corners of four adjacent SoP packages 196.

In FIG. 5k, ~~shows~~ an encapsulant or molding compound 210 is pre-dispensed or laminated over carrier 200, carrier tape 202, thermally releasable layer 204, as well as over and around SoP packages 196. Alternatively, transfer molding or other suitable process may be used to apply molding compound 210. Encapsulant 210 can be polymer composite material, such as epoxy resin with filler or fiber, epoxy acrylate with filler or fiber, or polymer with proper filler or fiber. In one embodiment, the filler in encapsulant 210 includes particles with a size less than or equal to about 100 μm at either a liquid, powder, or granular phase and is selected to have a content level and characteristics that facilitate the filling of gaps 206 and for filling an area around bumps 164 between BGA packages 166 and carrier 200. The filler in encapsulant 210 is further selected to control warpage and to improve package reliability. Encapsulant 210 is dispensed on thermally releasable layer 204, and in one embodiment is dispensed at a central location on carrier 200, e.g., at intersection 208 of gaps 206 at the corners of four adjacent SoP packages 196. Thus, a reconstituted wafer or fan-out substrate 214 is formed that

includes embedded SoP packages 196 and encapsulant 210. SoP packages 196 are embedded together in encapsulant 210, which is non-conductive and environmentally protects the SoP packages from external elements and contaminants.

In FIG. 5l, ~~shows~~ chase mold 218 is brought together with carrier 200, carrier tape 202, and thermally releasable layer 204 to enclose reconstituted wafer 214 within the mold for encapsulation. Chase mold 218 is brought together with carrier 200, carrier tape 202, and thermally releasable layer 204 by moving chase mold 218 around SoP packages 196 and encapsulant 210, or alternatively, by moving the SoP packages and encapsulant into the mold. In one embodiment, chase mold 218 includes only a first or top portion that is brought together with carrier 200, carrier tape 202, and thermally releasable layer 204 without a second or bottom mold portion. Carrier 200, carrier tape 202, and thermally releasable layer 204 serve as the bottom mold portion for the encapsulation process. Alternatively, semiconductor die SoP packages 196, carrier 200, carrier tape 202, and thermally releasable layer 204 may be disposed within a mold including multiple portions, such as top and bottom portions. After SoP packages 196 and encapsulant 210 are disposed within chase mold 218, the encapsulant can be partially or completely cured. After SoP packages 196 are embedded within encapsulant 210 to form reconstituted wafer 214, the reconstituted wafer is removed from chase mold 218.

In FIG. 5m, ~~shows~~ reconstituted wafer 214 is removed from chase mold 218. Carrier 200, carrier tape 202, and thermally releasable layer 204 are fully debonded and removed from bumps 164, semiconductor die 170, and encapsulant 210 by activating thermally releasable layer 204. Alternatively, debonding is accomplished by chemical etching, mechanical

peeling, CMP,

Claims

What is claimed:

~~1. A method of making a semiconductor device, comprising:~~

~~providing a ball grid array (BGA) package including first bumps;~~

~~mounting a first semiconductor die to the BGA package between the first bumps;~~

~~mounting the BGA package and first semiconductor die to a carrier;~~

~~depositing a first encapsulant over the carrier and around the BGA package and first semiconductor die;~~

~~removing the carrier to expose the first bumps and first semiconductor die; and~~

~~forming a fan-out interconnect structure electrically connected to the first bumps and first semiconductor die.~~

~~2. The method of claim 1, wherein providing the BGA package further includes:~~

~~providing a substrate;~~

~~mounting a second semiconductor die over the substrate;~~

~~electrically connecting the second semiconductor die to the substrate;~~

~~depositing a second encapsulant over the second semiconductor die and substrate; and~~

~~forming the first bumps over the substrate opposite the second semiconductor die.~~

~~3. The method of claim 1, wherein the first semiconductor die includes a height less than a height of the first bumps.~~

~~4. The method of claim 1, further including forming a warpage balance layer over the BGA package.~~

~~5. The method of claim 1, further including exposing a surface of the BGA package from the first encapsulant.~~

~~6. The method of claim 1, wherein forming the fan-out interconnect structure further includes:~~

~~forming a first insulating layer;~~

~~forming a first conductive layer over the first insulating layer and electrically connected to the first bumps and the first semiconductor die;~~

~~forming a second insulating layer over the first conductive layer; and~~

~~forming second bumps over the second insulating layer and electrically connected to the first conductive layer.~~

~~7~~1. A method of making a semiconductor device, comprising:

providing a semiconductor package further including, ~~first interconnect structures;~~

~~mounting a first semiconductor die to the semiconductor package between the first interconnect structures~~

(a) providing a substrate,

(b) disposing a first semiconductor die below a first surface of the substrate, ~~;~~

(c) depositing a first encapsulant ~~around~~ below the ~~semiconductor package and~~ first semiconductor die~~; and~~

~~forming a second interconnect structure electrically connected to the first interconnect structures and first~~

~~semiconductor die~~ and completely covering the first surface of the substrate, and

(d) disposing a plurality of first bumps directly on a second surface of the substrate opposite the first surface;

disposing a second semiconductor die over the second surface of the substrate between the first bumps including a back surface of the second semiconductor die oriented toward the second surface of the substrate;

depositing a second encapsulant around the substrate, first semiconductor die, first encapsulant, first-bumps, and second semiconductor die, wherein an active surface opposite the back surface of the second semiconductor die and a portion of the first bumps are exposed from the second encapsulant;

forming a first insulating layer over the second encapsulant and the active surface of the second semiconductor die;

forming a first conductive layer in contact with a contact pad of the second semiconductor die, the exposed portion of the first bumps, and the first insulating layer; and

forming an interconnect structure over the first conductive layer, wherein a height of the semiconductor device is less than 1 millimeter (mm).

~~8. The method of claim 7, wherein providing the semiconductor package further includes:~~

providing a substrate;

mounting a second semiconductor die over the substrate;

electrically connecting the second semiconductor die to the substrate;

depositing a second encapsulant over the second semiconductor die and substrate; and

forming the first interconnect structures over the substrate opposite the second semiconductor die.

92. The method of claim 71, wherein forming the second interconnect structure further includes:

forming a first insulating layer over the first encapsulant and in an opening over the first semiconductor die;

forming a first conductive layer over the first insulating layer and electrically connected to the first interconnect structures and the first semiconductor die;

forming a second insulating layer over the first conductive layer; and

forming a second bumps over the second insulating layer and electrically connected to the first conductive layer.

103. The method of claim 71, further including forming a warpage balance layer over the semiconductor package.

11. The method of claim 7, further including forming a second encapsulant around the first semiconductor die before forming the first encapsulant around the semiconductor package and first semiconductor die.

~~12. The method of claim 7, further including forming a conductive layer between the first semiconductor die and the second interconnect structure.~~

~~13~~4. The method of claim ~~7~~1, wherein the first ~~interconnect structures include a~~ bump~~s~~ ~~or~~include a stud bump.

~~14~~5. A method of making a semiconductor device, comprising:

providing a substrate;

~~providing~~disposing a first semiconductor ~~package including first interconnect structures~~ die below a first surface of the substrate;

~~mounting a first semiconductor die to the semiconductor package between the first interconnect structures; and~~

~~forming a second interconnect structure electrically connected to the first interconnect structures and first semiconductor die~~disposing a second semiconductor die over a second surface of the substrate;

forming a bump over the second surface of the substrate including a side surface of the bump adjacent to a side surface of the first semiconductor die; and

disposing an encapsulant contacting the side surface of the bump and the side surface of the second semiconductor die and around the first semiconductor die, second semiconductor die, and bump, wherein an active surface of the second semiconductor die and a portion of the bump are exposed from the encapsulant.

~~15. The method of claim 14, wherein providing the semiconductor package further includes:~~

~~providing a substrate;~~

~~mounting a second semiconductor die over the substrate;~~

~~electrically connecting the second semiconductor die to the substrate;~~

~~depositing an encapsulant over the second semiconductor die and substrate; and~~

~~forming the first interconnect structures over the substrate opposite the second semiconductor die.~~

~~16~~6. The method of claim ~~14~~5, wherein the ~~first~~second semiconductor die includes a height less than a height of the ~~first interconnect structures~~bump.

~~17~~7. The method of claim ~~14~~5, further including forming a warpage balance layer over the first semiconductor ~~package~~die.

~~18~~8. The method of claim ~~14~~5, further including ~~forming~~disposing a shielding layer or heat sink over the first semiconductor ~~package~~die.

~~19~~9. The method of claim ~~14~~5, further including~~:~~

~~depositing an encapsulant around the semiconductor package and first semiconductor die; and~~

forming an opening~~s~~ in the encapsulant ~~at an outer surface of the semiconductor device~~ to provide stress relief.

~~20~~10. The method of claim ~~15~~5, ~~wherein the second semiconductor die is~~ further including electrically connect~~ed~~ing ~~to the substrate~~ the first semiconductor die to the substrate with bond wires or microbumps.

~~21~~11. A semiconductor device, comprising:

a semiconductor package including,

(a) a substrate ~~first interconnect structures;~~,

(b) a first semiconductor die ~~mounted to the semiconductor package between the first interconnect structures~~ disposed below a first surface of the substrate;

(c) a first encapsulant ~~disposed~~deposited ~~around~~below the ~~semiconductor package and~~ first semiconductor die~~; and~~

~~a second interconnect structure electrically connected to the first interconnect structures and first semiconductor die.~~ and completely covering the first surface of the substrate, and

(d) a plurality of first bumps disposed directly on a second surface of the substrate opposite the first surface;

a second semiconductor die disposed over the second surface of the substrate between the first bumps including a back surface of the second semiconductor die oriented toward the second surface of the substrate;

a second encapsulant deposited around the substrate, first semiconductor die, first encapsulant, first-bumps, and second semiconductor die, wherein an active surface opposite the back surface of the second semiconductor die and a portion of the first bumps are exposed from the second encapsulant;

a first insulating layer formed over the second encapsulant and the active surface of the second semiconductor die;

a first conductive layer formed over and contacting a contact pad of the second semiconductor die, the exposed portion of the first bumps, and the first insulating layer; and

an interconnect structure formed over the first conductive layer, wherein a height of the semiconductor device is less than 1 millimeter (mm).

~~22. The semiconductor device of claim 21, wherein the semiconductor package further includes:~~

~~a substrate;~~

~~a second semiconductor die mounted to the substrate; and~~

~~a second encapsulant disposed over the second semiconductor die and substrate opposite the first interconnect structures.~~

~~23~~12. The semiconductor device of claim ~~2~~1, further including a warpage balance layer formed over the semiconductor package.

~~24~~13. The semiconductor device of claim ~~2~~1, wherein ~~a surface of the semiconductor package~~ the second surface of the substrate is exposed from the first encapsulant.

~~25~~14. The semiconductor device of claim ~~2~~1, wherein the ~~second~~ interconnect structure further includes:

~~a first insulating layer;~~

~~a first conductive layer formed over the first insulating layer and electrically connected to the first interconnect structures and the first semiconductor die;~~

a second insulating layer formed over the first conductive layer; and

a plurality of second bumps formed over the second insulating layer and electrically connected to the first conductive layer.

15. A semiconductor device, comprising:

a semiconductor package including a first semiconductor die and a first encapsulant disposed under and around the first semiconductor die;

a second semiconductor die disposed over a surface of the semiconductor package;

a plurality of bumps formed over and contacting the surface of the semiconductor package and outside a footprint of the

second semiconductor die, wherein the second semiconductor die is disposed directly between the bumps; and

a second encapsulant deposited under and around the semiconductor package, bumps, and second semiconductor die, wherein an active surface of the second semiconductor die and a portion of the bumps are exposed from the second encapsulant.

16. The semiconductor device of claim 15, wherein a width of the semiconductor device is substantially equal to a width of the semiconductor package.

17. The semiconductor device of claim 15, wherein the second encapsulant is a paste printed on the semiconductor package.

18. The semiconductor device of claim 15, wherein the first encapsulant further includes an opening partially but not completely through the first encapsulant.

19. The semiconductor device of claim 15 further including a substrate disposed between the first semiconductor die and second semiconductor die.

20. The semiconductor device of claim 15, further including an interconnect structure formed over the bumps and second semiconductor die.

21. The semiconductor device of claim 11, wherein a side surface of the second semiconductor die is disposed adjacent to a side surface of one of the plurality of first bumps.

22. The semiconductor device of claim 11, wherein the first encapsulant further includes an opening opposite the substrate.

23. A semiconductor device, comprising:

a substrate;

a first semiconductor die disposed below a first surface of the substrate;

a second semiconductor die disposed over a second surface of the substrate opposite the first surface;

a bump disposed over the second surface of the substrate and outside a footprint of the second semiconductor die including a side surface of the bump disposed adjacent to a side surface of the second semiconductor die; and

an encapsulant contacting the side surface of the bump and the side surface of the second semiconductor die and deposited around the first semiconductor die, second semiconductor die, and bump, wherein an active surface of the second semiconductor die and a portion of the bump are exposed from the encapsulant.

24. The semiconductor device of claim 23, wherein the encapsulant further includes an opening.

25. The semiconductor device of claim 23, further including an interconnect structure formed over the bump and second semiconductor die.

26. The semiconductor device of claim 23, wherein the second semiconductor die includes a height less than a height of the bump.

27. The semiconductor device of claim 23, wherein a back side of the second semiconductor die is oriented toward the second surface of the substrate.

28. The semiconductor device of claim 23, further including:

an insulating layer formed over the encapsulant and the active surface of the second semiconductor die; and

a conductive layer formed over and contacting a contact pad of the second semiconductor die, the exposed portion of the bump, and the insulating layer.

29. The semiconductor device of claim 23, wherein a height of the semiconductor device is less than 600 micrometers (μm).

30. The semiconductor device of claim 11, wherein the height of the semiconductor device is less than 600 micrometers (μm).

31. The semiconductor device of claim 15, wherein a height of the semiconductor device is less than 600 micrometers (μm).

32. The semiconductor device of claim 20, wherein the interconnect structure further includes:

an insulating layer formed over the second encapsulant and the active surface of the second semiconductor die; and

a conductive layer formed over and contacting a contact pad of the second semiconductor die, the exposed portion of the bumps, and the insulating layer.