

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
16 May 2019 (16.05.2019)



(10) International Publication Number
WO 2019/094470 A1

(51) International Patent Classification:

H05K 3/40 (2006.01) H01P 5/02 (2006.01)
H05K 3/42 (2006.01) H01P 1/04 (2006.01)

(21) International Application Number:

PCT/US2018/059625

(22) International Filing Date:

07 November 2018 (07.11.2018)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/584,264	10 November 2017 (10.11.2017)	US
62/584,260	10 November 2017 (10.11.2017)	US
62/636,364	28 February 2018 (28.02.2018)	US
62/636,375	28 February 2018 (28.02.2018)	US
15/988,296	24 May 2018 (24.05.2018)	US

(71) Applicant: **RAYTHEON COMPANY** [US/US]; 870 Winter Street, Waltham, MA 02451-1449 (US).

(72) Inventors: **SOUTHWORTH, Andrew, R.**; 870 Winter Street, Waltham, MA 02451-1449 (US). **SIKINA, Thomas, V.**; 870 Winter Street, Waltham, MA 02451-1449 (US). **HAVEN, John, P.**; 870 Winter Street, Waltham, MA 02451-1449 (US). **BENEDICT, James, E.**; 870 Winter Street, Waltham, MA 02451-1449 (US). **WILDER, Kevin**; 870 Winter Street, Waltham, MA 02451-1449 (US).

(74) Agent: **NOE, Keith F.** et al.; Lando & Anastasi, LLP, Riverfront Office Park, One Main Street, Suite 1100, Cambridge, MA 02142 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,

(54) Title: ADDITIVE MANUFACTURING TECHNOLOGY MICROWAVE VERTICAL LAUNCH

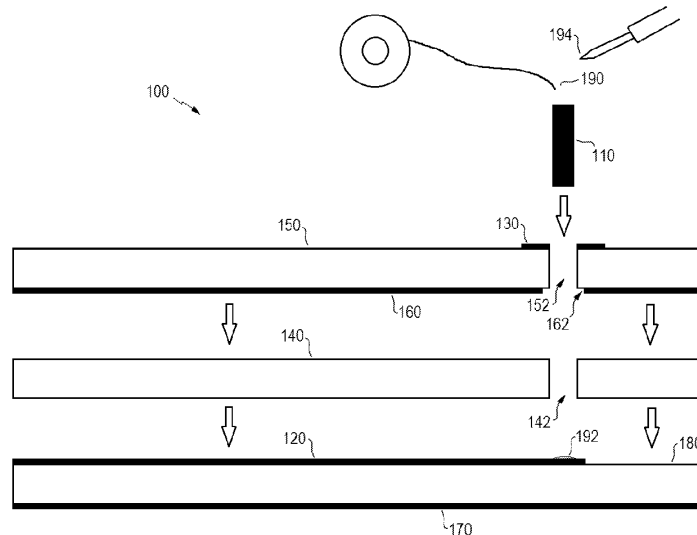


FIG. 3

(57) Abstract: Electromagnetic circuit structures and methods are provided for a circuit board that includes a hole disposed through a substrate to provide access to an electrical component, such as a signal trace line (or stripline), that is at least partially encapsulated (e.g., sandwiched) between substrates. The electrical component includes a portion substantially aligned with the hole, and an electrical conductor is disposed within the hole. The electrical conductor is soldered to the portion of the electrical component.

[Continued on next page]

SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*