(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 March 2006 (30.03.2006)

PCT

(10) International Publication Number
WO 2006/032948 A1

(51) International Patent Classification[7]: H01L 21/762

(21) International Application Number:
PCT/IB2004/003301

(22) International Filing Date:
21 September 2004 (21.09.2004)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Parc Technologique des Fontaines, Chemin des Franques, F-38190 Bernin (FR).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **AKATSU, Takeshi** [JP/FR]; 9, Place de l'Eglise, F-38330 St. Nazaire les Eymes (FR).

(74) Agents: **MARTIN, Jean-Jacques** et al.; Cabinet Regimbeau, 20, rue de Chazelles, F-75847 Parix Cédex 17 (FR).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

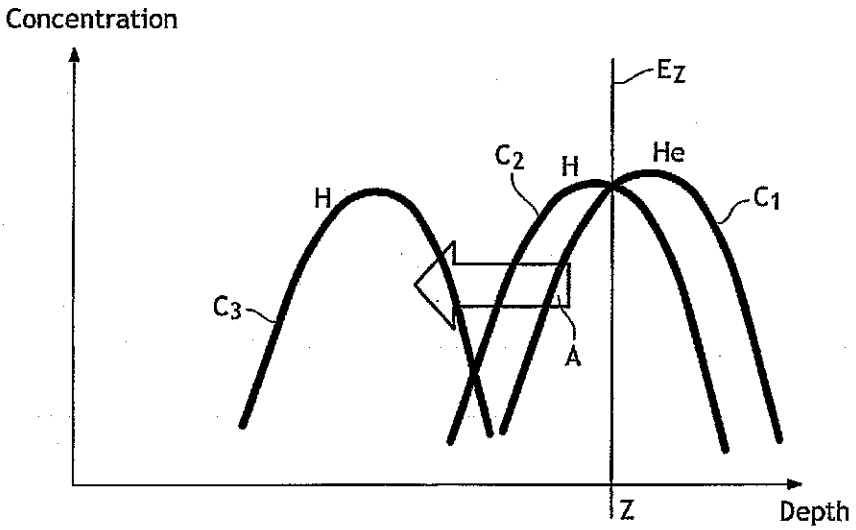
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHOD FOR OBTAINING A THIN LAYER BY IMPLEMENTING CO-IMPLANTATION AND SUBSEQUENT IMPLANTATION



(57) **Abstract:** The invention proposes a method for transferring a thin layer of semiconductor material on a substrate by the SMARTCUT™ type process, the method being characterized in that the implantation step comprises: a first implantation operation consisting in carrying out an implantation of species so as to create said embrittlement zone at a first depth in the thickness of the donor substrate; a second implantation operation consisting in carrying out an implantation of species according to second implantation conditions chosen to create: - at a second depth different from said first depth so as not to affect the detachment that has to take place at the level of the embrittlement zone at said first depth, gettering region preventing the diffusion of species implanted during said first implantation operation towards said face of the donor substrate under which implantation is carried out, thus limiting blisters formation.

WO 2006/032948 A1