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METHOD FOR MAKING FIELD EFFECT TRANSISTORS HAVING SUB-LITHOGRAPHIC GATES WITH VERTICAL SIDE WALLS

ABSTRACT

Method for the formation of field effect transistors (FETs) and general, and metal oxide field effect transistors (MOSFETs) (20) in particular, comprising the following steps of:

- forming a dielectric stack (31,35) on a semiconductor structure;
- defining an etch window (33) on the dielectric stack (31,35);
- defining a gate hole in the dielectric stack (31,35) by transferring the etch window into the dielectric (31,35) stack using a reactive ion etching (RIE) process;
- depositing a side wall layer (46);
- removing the side wall layer (46) from horizontal surfaces of the dielectric stack (31,35) and gate hole (34) such that side wall spacers (46) remain which reduce the lateral size of the gate hole (34);
- depositing a gate conductor (36) such that it fills the gate hole (34);
- removing the gate conductor (36) covering the portions of the semiconductor structure surrounding the gate hole (34);
- removing at least part of the dielectric stack (31,35); and
- removing the side wall spacers (46).

Fig.2



