METHODS FOR FORMING AND INTEGRATED CIRCUIT STRUCTURES CONTAINING ENHANCED-SURFACE-AREA CONDUCTIVE LAYERS

Field of the Invention

This invention relates to semiconductor devices and the fabrication thereof, and particularly to ruthenium-containing conductive layers and the formation and use thereof.

Background of the Invention

A capacitor generally includes two electrical conductors in close proximity to, but separated from, each other. The two conductors form the "plates" of the capacitor, and may be separated by a dielectric material. When a voltage is applied across the plates of a capacitor, electrical charge accumulates on the plates. If the plates are electrically isolated essentially immediately after a voltage is applied, the accumulated charge may be stored on the plates, thus "storing" the applied voltage difference.

The fabrication of integrated circuits involves the formation of conductive layers for use as various circuit components, including for use as capacitor plates. Memory circuits, such as DRAMs the like, use conductive layers to form the opposing plates of storage cell capacitors.

The drive for higher-performance, lower-cost integrated circuits dictates ever-decreasing area for individual circuit features, including storage capacitors. Since capacitance of a capacitor (the amount of charge that can be stored as a function of applied voltage) generally varies with the area of capacitor plates, as the circuit area occupied by the storage capacitor decreases, it is desirable to take steps to preserve or increase capacitance despite the smaller occupied area, so that circuit function is not compromised.

Various steps may be taken to increase or preserve capacitance without increasing the occupied area. For example, material(s) having higher dielectric constant may be used between the capacitor plates. Further, the plate surfaces may

be roughened to increase the effective surface area of the plates without increasing the area occupied by he capacitor.

One method for providing a roughened surface for a plate of a storage cell capacitor is to form the plate of hemispherical grain polysilicon (HSG), possibly with an overlying metal layer. The hemispherical grains of HSG enhance the surface area of the plate without increasing its occupied area.

HSG presents difficulties in fabrication, however, because of the formation of silicon dioxide on and near the HSG. A silicon dioxide layer may form on the HSG, particularly during deposition of the capacitor's dielectric layer. Even with an intervening metal layer present, oxygen from the deposition of the dielectric layer can diffuse through the metal layer, forming silicon dioxide at the polysilicon surface. Silicon diffusion through the metal layer may also produce a silicon dioxide layer between the metal and the dielectric layers.

Silicon dioxide between the metal layer and the HSG can degrade the electrical contact to the metal capacitor plate surface. Silicon dioxide between the metal layer and the dielectric layer can decrease the capacitance of the resulting capacitor.

To attempt to avoid these negative effects caused by formation of silicon dioxide, a diffusion barrier layer may be employed between the HSG and the metal layer. But in the typical capacitor geometry, the greater the total number of layers, the larger the required minimum area occupied by the capacitor. Further, the upper surface of each additional layer deposited over the HSG tends to be smoother than the underlying surface, reducing the increased surface area provided by the HSG.

Summary

The present invention provides an enhanced-surface-area (rough-surfaced) conductive layer compatible with high-dielectric constant materials and useful in the formation of integrated circuits, particularly for plates of storage capacitors in memory cells.

The enhanced-surface-area conductive layer may be formed by first forming a film having two or more phases, such as iridium and iridium oxide phases, ruthenium and ruthenium oxide phases, rhodium and rhodium oxide phases,

platinum and platinum-rhodium phases, and the like. The film may be formed over an underlying conductive layer. At least one of the phases in the film is then selectively removed from the film, leaving at least one of the phases behind to form an enhanced-surface-area conductive layer.

In an illustrated embodiment, a phase of a layer is removed to leave a pitted surface of a non-removed phase. The pitted surface may include islands formed of the non-removed phase. An "islanded" surface may also be formed by the differential removal, the surface of which may include some pits. Any suitable selective removal process may be employed, such as an etch process or etchant, wet or dry, that etches one phase at a much greater rate than an other phase. Thermal and electrochemical selective removal techniques may also be employed. The selective removal process preferentially removes the one phase, leaving a pitted or "islanded" surface of the other phase. In the case of an islanded surface having separate or isolated islands, an underlying conductive layer may physically and electrically connect the islands. The layer of remaining pitted or islanded material, together with the underlying conductive layer, if any, constitutes an enhanced-surface-area electrically conductive layer.

The enhanced-surface-area conductive layer may be used to form a plate of a storage capacitor in an integrated circuit, such as in a memory cell of a DRAM or the like. If the material chosen to form the enhanced-surface-area conductive layer is relatively resistant to oxidation-induced decreases in conductivity, such as with ruthenium oxide or other oxygen-containing conductors, for example, then the tendency toward silicon dioxide formation may be reduced or eliminated, providing improved compatibility for use with high-dielectric-constant dielectric materials. An intervening metal layer and/or barrier such as used in the HSG approach may also be used, but is desirably omitted from the capacitor structure, allowing smaller dimensions for capacitors with the same or even greater capacitance. This allows the design and fabrication of higher speed, higher density, and lower cost memory circuits.

Brief Description of the Drawings

FIG. 1 is a cross-section of a structure with layers used in an example of a process according to one embodiment of the present invention.

FIG. 2 is a cross-section of the layers of FIG. 1 after separation or crystallization of separate phases within one of the layers.

FIG. 3 is a cross-section of the layers of FIG. 2 after preferential removal of one of the phases.

FIG. 4 is a cross section of the layers of FIG. 3 after formation of a dielectric layer on the structure.

FIG. 5 is a cross section of the layers of FIG. 4 after deposition of a conductive layer on the structure.

FIG. 6 is a cross-section of a container capacitor structure produced by a process of the present invention and included in an integrated circuit.

FIG. 7 is a computer generated plot of an X-ray diffraction study of a ruthenium-containing film both before and after preferential removal of ruthenium.

Detailed Description

The present invention allows the creation of a surface-area-enhanced conductive layer that has improved compatibility with high-dielectric-constant ("high-κ") dielectric materials.

This is achieved by forming a layer of material having at least two phases, at least one of phase of which is a conductive material. The layer may be formed over an underlying conductive layer. The layer may have two or more phases in an as-deposited state. The layer may also be treated in physical and/or chemical environments, after or during deposition, which environments enhance, control, or influence the development of zones of different phases within the layer.

After the layer having at least two phases is formed, at least one of the phases is selectively removed, leaving at least one of the phases of a conductive material behind. The remaining conductive phase or phases form, together with the underlying conductive layer, if any, an enhanced-surface area conductive layer which may be used to form a plate of a storage capacitor in an integrated circuit, such as in a memory cell of a DRAM or the like. If the material chosen to form the

enhanced-surface-area conductive layer is relatively resistant to oxidation-induced decreases in conductivity, as with an oxygen-containing conductor such as ruthenium oxide, for example, then the tendency toward silicon dioxide formation may be reduced or eliminated, providing improved compatibility for use with high-dielectric-constant dielectric materials.

Example Embodiments

In accordance with a specific embodiment of the present invention, a surface-area-enhanced conductive layer may be created by differentially removing ruthenium relative to ruthenium oxide from a film or layer containing both ruthenium (Ru) and ruthenium oxide (RuO_2) phases. The differential removal process, in this example, may involve the preferential removal of ruthenium relative to ruthenium oxide in the layer. For example, the removal may be performed with an etchant and/or etch process that preferentially etches ruthenium relative to ruthenium oxide, leaving an enhanced-surface area layer comprising ruthenium oxide.

The surface-area-enhanced conductive layer may be formed on a supporting structure 10 shown in partial cross-section in FIG. 1. The supporting structure may be any structure present in or on an integrated circuit during the fabrication thereof, but is typically a conductive material that will be in electrical contact with a capacitor plate formed by the surface-area-enhanced conductive layer.

An underlying electrically conductive layer 12 may be formed or deposited first onto the structure 10, such as by chemical vapor deposition (CVD), sputtering, or another suitable process. The layer 12 is typically of a thickness at least sufficient to maintain continuity of the layer 12, such as at least about 100 Angstroms. The layer 12 may be formed of any suitable electrically conductive material, but is desirably formed of ruthenium oxide.

An oxygen-deficient non-stoichiometric ruthenium oxide (RuO_x) layer 14 may then be deposited or formed, also by CVD, sputtering, or any other suitable process. In representative examples, the thickness of the resulting RuO_x layer 14 is between about 1 Angstrom and 500 Angstroms. The RuOx layer 14 may then be annealed to facilitate crystallization of a ruthenium phase and a ruthenium oxide

(RuO_2) phase and/or a non-stoichiometric ruthenium oxide (RuO_x) phase within the layer 14. Annealing may be accomplished, for example, by rapid thermal anneal (RTA) in non-oxidizing ambients, such as nitrogen, ammonia, helium, argon, or by other suitable annealing processes, to produce both zones 18 of ruthenium (Ru) and zones 16 of ruthenium oxide (RuO_2 and/or RuO_x) within the layer 14, as shown in FIG. 2. The gas ratios of the ruthenium and oxygen source gases during deposition of the layer 14 may be selected to create a desired ratio between the amounts of the respective phases present in the layer 14. The deposition conditions and the RTA time, temperature, and pressure may be selected to provide a desired mean size for the ruthenium zones. The ruthenium zones 18, for example, desirably extend completely through the thickness of the layer 14, as shown, and desirably have a mean diameter of about one to three times the thickness of the layer 14 most desirably about two times the thickness of the layer 14, or about 400 Angstroms for a 200-Angstrom layer 14.

The layer 14 having both ruthenium zones 18 and ruthenium oxide zones 16 may then be processed to differentially remove the ruthenium phase relative to the ruthenium oxide phase, and desirably relative to the underlying conductive layer 12. In the illustrated embodiment, ruthenium is preferentially removed relative to ruthenium oxide. A wet etch process is one suitable approach for differentially removing ruthenium. As a specific example, a wet etchant comprising ceric ammonium nitrate and acetic acid may be used. Other processes that remove ruthenium preferentially over ruthenium oxide may also be used. As additional examples, etching using ozonated water or selective dry etch processes may also be employed.

In the illustrated embodiment, the wet etch process may be controlled so as to essentially remove the ruthenium phase from the layer 14, or at least to remove those zones of ruthenium that are exposed to the etch. In the case of ruthenium zones extending completely through the layer 14, essentially all of the ruthenium phase may be removed from the layer 14, as shown in FIG. 3, leaving the ruthenium oxide zones 16.

Depending on the ratio of ruthenium phase to ruthenium oxide phase in the layer 14, the remaining ruthenium oxide zones 16 may be in the form of a layer with

pits or depressions therein, or in the form of islands or nodules 20 separated by an open web 22, or a combination of pits extending partially or entirely through the layer 14 and islands. In other words, the layer 14, following anneal, may comprise a relatively even mixture of ruthenium oxide and ruthenium phases, or it may be zones of ruthenium phase in a ruthenium oxide matrix, or zones of ruthenium oxide phase in a ruthenium matrix, depending on the composition of the pre-annealed layer, and on the anneal conditions. When the layer 14 is subsequently etched in the illustrated example, the enhanced surface-area structure results.

For a capacitor plate, generally no areas of the plate should be electrically isolated. The underlying conductive layer 12 thus serves to electrically connect all of the remaining ruthenium oxide zones 16, particularly if they are in the form of physically separated islands.

Where the remaining ruthenium oxide is the form of islands, the mean distance between nearest edges of such islands is desirably between about three to four times a thickness of a dielectric layer that conformally covers the layer 14, For example, for a capacitor that includes a 60 Angstrom thick tantalum oxide layer, the mean distance between the nearest edges of such islands is preferably is in the range of 180-240 Angstroms. Where the remaining ruthenium oxide includes pits, the pits have a mean diameter of one to three times the thickness of the layer 14 and have a mean closest distance that is at least two times the thickness of the layer 14.

The remaining ruthenium oxide zones 16 shown in FIG. 3 constitute, together with the underlying conductive layer 12, an enhanced-surface-area conductive layer compatible with high-dielectric-constant dielectric materials. To form a capacitor with the enhanced-surface-area conductive layer of FIG. 3, a layer 24 of a dielectric material is provided on the structure. The layer 24 may be of a high-dielectric-constant dielectric material, generally any dielectric with a dielectric constant of at least 9, or more preferably, a dielectric constant of at least 20, with tantalum pentoxide (Ta_2O_5) being a specific example. The dielectric material may be formed conformally over the enhanced-surface-area conductive layer, as shown in FIG. 4. Other high-constant dielectrics may also be employed, such as barium strontium titanium oxide, lead zirconium titanium oxide, and strontium bismuth tantalum oxide, for example. Because of the relatively large diameter of the

previously removed ruthenium phase zones, the layer 24 can conform somewhat to the shape of the enhanced-surface-area conductive layer, allowing an enhanced surface area on both sides of the layer 24. In other words, the surface of the layer 24 away from the remaining ruthenium oxide zones is desirably not flat, but follows at least somewhat the contours of the underlying ruthenium oxide, providing an enhanced surface area on this surface as well.

A conductive layer 26 may then be formed or deposited conformally over the dielectric layer 24, as shown in FIG. 5. The surface of layer 26 uppermost in the figure is not shown because the layer may generally be of any thickness sufficiently thick to insure continuity of the layer and sufficiently thin to fit within the overall volume allotted to the capacitor. As shown in FIG. 5, the surface of layer 26 next to the dielectric layer 24 may conform to the enhanced surface area of the dielectric layer 24, providing an enhanced surface area for the conductive layer 26 as well. The two conductive layers, one formed by layer 12 and zones 16, and one formed by layer 26, form the two plates of a capacitor. Both plates may have enhanced surface area relative to the area occupied by the capacitor. The possible omission of an intermediate metal layer and/or barrier layer above the lower plate allows for increased plate surface area and decreased overall thickness of the capacitor structure.

Application of the plate structure shown in FIG. 5 to a capacitor of an integrated circuit--a container capacitor in this example--is illustrated in the cross-section of FIG. 6. The supporting structure 10 in this example is a conductive plug of polysilicon or other conductive material formed at the bottom of an opening in a dielectric material 28 such as borophosphosilica glass (BPSG). The plug contacts a circuit element such as a transistor gate (not shown). At the sides of the cylindrical container, the BPSG itself functions a supporting structure for the capacitor plate structure. The thinness of the capacitor structure provided by the layer structure of FIG. 5 maximizes the capacitor plate surface area in the container capacitor of FIG. 6, particularly for the inner (upper) electrode, the surface area of which decreases with increasing thickness of the layer structure. The enhanced-surface-area layers also increase the effective surface area beyond that of the occupied area. The use of

the enhanced-surface-area ruthenium oxide conductive layer thus provides improved capacitance in a given area.

FIG. 7 shows X-ray diffraction data confirming the formation of ruthenium and ruthenium oxide phases as described in this example embodiment, with preferential removal of ruthenium. Deposited RuO_x films were wet etched in CR14, a well-known commercially available wet etchant comprising ceric ammonium nitrate and acetic acid. Some films were annealed in non-oxidizing ambients (for example, N_2, NH_3, He, Ar) prior to the wet etch. SEM examination of annealed films wet-etched in CR14 for 30 seconds showed pitting of the films consistent with preferential etching of ruthenium, leaving ruthenium oxide, while non-annealed films showed less evidence of selective etching. X-ray diffraction studies confirmed the presence of ruthenium and ruthenium oxide in the pre-etch annealed films, and the absence of ruthenium in the post-etch films. FIG. 7 shows the pre-etch and post-etch X-ray diffraction data, with ruthenium peaks present in a pre-etch trace 701 but absent in a post-etch trace 703.

The invention above is described in detail by means of a specific example embodiment, but is not limited thereto. Furthermore, variations within the scope and spirit of the invention discussed above will be apparent to those of skill in the art. For example, in addition to the first layer, the dielectric layer and the overlaying conductive layer may be proximate to one another, with other intervening layers, although in the desirable approach, these layers abut one another, and layers 24 and 26 need not be homogeneous as they may be formed of multiple layers or materials. The invention is accordingly defined not by the particular embodiments and variations explicitly described, but by the claims below.

We claim:

1. A method of forming an enhanced-surface-area conductive structure in the manufacture of a structure for use in an integrated circuit, the method comprising:

forming a layer containing at least two phases, the phases including at least one conductive phase; and

preferentially removing at least one of the at least two phases so as to leave behind at least the at least one conductive phase.

2. The method according to claim 1, wherein the act of removing comprises etching the layer.

3. The method of claim 1, wherein the act of forming comprises depositing the layer and annealing the layer.

4. The method of claim 1, wherein the act of forming comprises forming a layer having phases of ruthenium and of ruthenium oxide.

5. The method of claim 1, wherein the act of forming comprises depositing a layer of ruthenium oxide and annealing the layer of ruthenium oxide so as to form ruthenium and ruthenium oxide phases within the layer.

6. A method of forming a structure on an integrated circuit, the method comprising:

annealing a layer comprising oxygen-deficient non-stoichiometric conductive metallic oxide; and

removing metal from the annealed layer at a rate which is greater than the rate at which metallic oxide is removed from the layer.

7. The method of claim 6, wherein the act of annealing comprises annealing a layer comprising oxygen-deficient non-stoichiometric ruthenium oxide.

8. A method of forming a structure on an integrated circuit comprising:

at least partially separating a first layer into respective phases; and

differentially removing a first phase of the respective phases from the first layer, leaving a second phase of the respective phases within the first layer, wherein the second phase is an electrically conductive material.

9. The method according to claim 8, comprising:

providing a second layer of a dielectric material in proximity to the first layer; and providing a third electrically conductive layer in proximity to the second layer.

10. The method according to claim 9, comprising abutting the first, second, and third layers against one another with no intermediate layers.

11. The method according to claim 8 in which the act of at least partially separating the first layer into respective phases comprises at least partially separating the first layer into respective ruthenium and ruthenium oxide phases.

12. A method of forming a conductive structure, comprising:

forming a layer of electrically conductive material;

forming a layer of non-stoichiometric ruthenium oxide on the layer of conductive material;

annealing the layer of non-stoichiometric ruthenium oxide to form ruthenium and ruthenium oxide phases; and

differentially removing the ruthenium phase relative to the ruthenium oxide phase.

13. The method of claim 12, wherein the non-stoichiometric ruthenium oxide layer is oxygen-deficient.

14. A method of forming a conductive structure, the method comprising:

depositing a layer of oxygen-deficient non-stoichiometric ruthenium oxide;

annealing the deposited layer for a time and at a temperature sufficient to cause at least some separation of ruthenium and ruthenium oxide phases within the layer; and

removing ruthenium preferentially over ruthenium oxide from the layer.

15. The method of claim 14, wherein the act of annealing comprises forming zones of ruthenium phase material within the layer with at least some of the zones extending through an entire thickness of the layer.

16. The method of claim 14, wherein the act of annealing comprises forming zones of ruthenium phase material within the layer, wherein a mean diameter of such zones is in the range of about one to about three times a thickness of the layer.

17. A method of forming a conductive structure, the method comprising:

forming a layer of electrically conductive material;

forming a layer of oxygen-deficient ruthenium oxide on the layer of conductive material;

annealing the layer of oxygen-deficient ruthenium oxide to form ruthenium and ruthenium oxide phases; and

differentially removing the ruthenium relative to the ruthenium oxide.

18. The method of claim 17, wherein the act of forming a layer of oxygen-deficient ruthenium oxide comprises depositing a layer of ruthenium oxide.

19. The method of claim 17, wherein the act of differentially removing comprises preferentially etching a ruthenium phase in a layer of oxygen-deficient ruthenium oxide and ruthenium.

20. A method of forming at least one capacitor in an integrated circuit, the method comprising:

forming a first conductive layer comprising ruthenium and ruthenium oxide phases;

removing ruthenium from the first conductive layer so as to leave remaining zones of ruthenium oxide;

forming a dielectric layer on or in proximity to the remaining zones of ruthenium oxide; and

forming a second conductive layer on or in proximity to the dielectric layer.

21. The method of claim 20, wherein the dielectric layer and second conductive layer are each a single layer of a homogenous material.

22. The method of claim 20, wherein the act of forming the dielectric layer comprises forming a layer of a material having a dielectric constant of at least 9.

23. The method of claim 20, wherein the act of forming the dielectric layer comprises forming a layer of a material having a dielectric constant of at least 20.

24. The method of claim 20, wherein the act of forming the dielectric layer comprises forming a layer of tantalum pentoxide.

25. A method of forming a capacitor, comprising:

forming a first layer of conductive material;

forming a second layer over the first layer of conductive material, the second layer comprising zones of ruthenium and ruthenium oxide;

etching the zones of ruthenium so as to allow the zones of ruthenium oxide to remain;

forming a layer of dielectric material on the remaining zones of ruthenium oxide and the first layer of conductive material; and

forming a third layer of conductive material on the layer of dielectric material.

26. The method of claim 25, wherein the act of forming a first layer comprises forming a first layer of conductive material resistant to the etching performed in the act of etching the zones of ruthenium.

27. The method of claim 25, wherein the act of forming the second layer comprises forming a layer of ruthenium oxide and at least partially separating the layer of ruthenium oxide into ruthenium oxide and ruthenium phases.

28. The method of claim 25, wherein the step of forming a layer of dielectric material comprises forming a layer of dielectric material conformally over the remaining zones of ruthenium oxide such that a surface of the layer of dielectric material spaced from the surface of the remaining zones of ruthenium oxide conforms at least in part to the contours of the surface of the remaining ruthenium oxide.

29. The method of claim 25, further comprising etching the zones of the ruthenium and ruthenium oxide to have a mean closest distance that is at least twice a thickness of the layer of dielectric material.

30. An enhanced-surface-area conductive structure in an integrated circuit, the structure comprising a layer of ruthenium oxide having at least one pitted surface.

31. A capacitor structure in an integrated circuit, the structure comprising a layer of conductive metallic oxide having a pitted surface with a layer of dielectric material disposed conformally on the pitted surface.

32. The capacitor structure of claim 31, further comprising a layer of conductive material disposed on the layer of dielectric material.

33. The capacitor structure of claim 31, wherein at least some of the pits in the surface of the conductive metallic oxide layer extend completely through the conductive metallic oxide layer.

34. The capacitor structure of claim 33, wherein the pits in the surface of the conductive metallic oxide layer have a mean diameter in the range of one to three times a thickness of the conductive metallic oxide layer.

35. The capacitor structure of claim 33, wherein the pits in the surface have a mean closest distance that is at least two times a thickness of the layer of dielectric material.

36. The capacitor structure of claim 31, wherein the conductive metallic oxide layer comprises ruthenium oxide.

37. A conductive structure in an integrated circuit, the structure comprising a layer of conductive material with islands of conductive metallic oxide disposed thereon.

38. The structure of claim 37, wherein the conductive metallic oxide comprises ruthenium oxide.

39. A capacitor structure in an integrated circuit, the structure comprising:

a layer of conductive material with islands of conductive metallic oxide disposed thereon; and

a layer of dielectric material disposed conformally on the islands of conductive metallic oxide, wherein a portion of a surface of the layer of conductive material is exposed between the islands.

40. The capacitor structure of claim 39, wherein the conductive metallic oxide comprises ruthenium oxide.

41. The capacitor structure of claim 39, further comprising a layer of conductive material disposed conformally on the layer of dielectric material.

42. An integrated circuit, comprising a plurality of capacitors that include a layer of conductive metallic oxide having a pitted surface with a layer of dielectric material disposed conformally on the pitted surface.

43. A method of forming an enhanced-surface-area conductive structure in the manufacture of a structure for use in an integrated circuit, the method comprising:

forming a layer containing at least two phases, the phases including at least one conductive phase; and wherein at least one of the two phases extends completely through the layer; and

preferentially removing at least one of the at least two phases so as to leave behind at least the at least one conductive phase.

44. The method according to claim 43, wherein the act of removing comprises etching the layer.

45. The method of claim 43, wherein the act of forming comprises depositing the layer and annealing the layer.

46. The method of claim 43, wherein the act of forming comprises forming a layer having phases of ruthenium and of ruthenium oxide.

47. The method of claim 43, wherein the act of forming comprises depositing a layer of ruthenium oxide and annealing the layer of ruthenium oxide so as to form ruthenium and ruthenium oxide phases within the layer.

48. A method of forming a conductive structure in the manufacture of a structure for use in an integrated circuit, the method comprising:

forming a layer containing at least two phases, the phases including at least one conductive phase wherein at least one of the two phases extends completely through the layer; and

roughening the layer by preferentially removing at least one of the at least two phases so as to leave behind at least the at least one conductive phase.

49. The method according to claim 48, wherein the act of roughening comprises etching the layer.

50. The method of claim 48, wherein the act of forming comprises depositing the layer and annealing the layer.

51. The method of claim 48, wherein the act of forming comprises forming a layer having phases of ruthenium and of ruthenium oxide.

52. A method of forming a structure on an integrated circuit comprising:

at least partially separating a first layer into respective phases wherein at least one of the phases extends completely through the first layer; and

roughening the first layer by differentially removing a first phase of the respective phases from the first layer, leaving a second phase of the respective phases within the first layer, wherein the second phase is an electrically conductive material.

53. An enhanced-surface-area conductive structure in an integrated circuit, the structure comprising a conductive layer of ruthenium and ruthenium oxide, wherein at least one surface of the conductive layer has a plurality of pits situated at ruthenium phase zones in the conductive layer.

54. A capacitor structure in an integrated circuit, comprising:

a layer of conductive metallic oxide with a surface having a plurality of pits situated at metallic phase zones in the conductive layer; and

a layer of dielectric material disposed conformally on the pitted surface.

55. A capacitor structure in an integrated circuit, the structure comprising:

a supporting structure;

a layer of conductive metallic oxide having a surface that includes a plurality of pits situated at metallic phase zones in the conductive metallic oxide layer; and

a layer of dielectric material disposed conformally on the pitted surface.

56. The capacitor structure of claim 55, further comprising a continuous layer of conductive material disposed on the layer of dielectric material.

57. The capacitor structure of claim 55, wherein at least some of the pits in the surface of the conductive metallic oxide layer extend completely through the conductive metallic oxide layer.

58. The capacitor structure of claim 55, wherein the pits in the surface of the conductive metallic oxide layer have a mean diameter in the range of one to three times a thickness of the conductive metallic oxide layer.

59. The capacitor structure of claim 55, wherein the pits in the surface have a mean closest distance that is at least two times a thickness of the layer of dielectric material.

60. The capacitor structure of claim 55, wherein the conductive metallic oxide layer comprises ruthenium oxide.

61. A method of forming an enhanced-surface-area conductive structure, the method comprising:

forming a layer of electrically conductive material;

forming a layer of oxygen-deficient ruthenium oxide on the layer of the conductive material;

annealing the layer of oxygen-deficient ruthenium oxide to form a layer that includes ruthenium and ruthenium oxide phases; and

differentially removing the ruthenium relative to the ruthenium oxide so as to form ruthenium zones that extend substantially through the thickness of the layer of ruthenium and

ruthenium oxide phases, wherein the ruthenium zones have widths of between about one to three times a thickness of the layer of ruthenium and ruthenium oxide phases.

62. A method of forming an enhanced-surface-area conductive structure, the method comprising:

forming a layer of electrically conductive material;

forming a layer of oxygen-deficient ruthenium oxide on the layer of the conductive material;

annealing the layer of oxygen-deficient ruthenium oxide to form a layer that includes ruthenium and ruthenium oxide phases; and

differentially removing the ruthenium relative to the ruthenium oxide so as to form ruthenium oxide pits having a diameter of between about one to three times the thickness of the layer of ruthenium and ruthenium oxide phases.

63. A method of forming a conductive structure, comprising:

forming a layer of electrically conductive material;

forming a layer of non-stoichiometric ruthenium oxide on the layer of conductive material;

annealing the layer of non-stoichiometric ruthenium oxide to form ruthenium and ruthenium oxide phases; and

roughening the layer by differentially removing the ruthenium phase relative to the ruthenium oxide phase.

64. A method of forming a conductive structure, the method comprising:

depositing a layer of oxygen-deficient non-stoichiometric ruthenium oxide;

annealing the deposited layer for a time and at a temperature sufficient to cause at least some separation of ruthenium and ruthenium oxide phases within the layer; and

roughening the layer by removing ruthenium preferentially over ruthenium oxide from the layer.

65. A method of forming a conductive structure, the method comprising:

forming a layer of electrically conductive material;

forming a layer of oxygen-deficient ruthenium oxide on the layer of conductive material;

annealing the layer of oxygen-deficient ruthenium oxide to form ruthenium and ruthenium oxide phases; and

roughening the layer by differentially removing the ruthenium relative to the ruthenium oxide.

66. A method of forming at least one capacitor in an integrated circuit, the method comprising:

forming a first conductive layer comprising ruthenium and ruthenium oxide phases;

roughening the first conductive layer by removing ruthenium from the first conductive layer so as to leave remaining zones of ruthenium oxide;

forming a dielectric layer on or in proximity to the remaining zones of ruthenium oxide; and

forming a second conductive layer on or in proximity to the dielectric layer.