METHODS TO ELIMINATE CONTACT PLUG SIDEWALL SLIT

Background of Invention

1) Field of the Invention

This invention relates generally to fabrication of semiconductor devices and more particularly to methods to form contact plugs and barrier layers and interconnects.

2) Description of the Prior Art

It is well known that integrated circuit fabrication on semiconductor wafers requires the formation of precisely controlled apertures, such as contact openings, that are subsequently filled with a conductive metal and interconnected to create components and very large scale integrated (VLSI) or ultra large scale integrated (ULSI) circuits. The methods for defining and forming such openings are equally well known to those who are skilled in the art. Market demands for faster and more powerful integrated circuits have resulted in significant growth in the number of devices per cm^2, i.e., a higher packing fraction of active devices. This increased

packing fraction invariably means that the interconnections for ever-more-complicated circuits are made to smaller dimensions than before. Thus the aspect ratios of the contacts, i.e., the ratio of the opening depth to the opening diameter, have increased.

In the past, aluminum (Al) was deposited in the contact openings over a barrier layer to form contacts. However, some fabrication processes, especially those used to produce CMOS and bipolar semiconductors, now use tungsten (W) deposited within the contact opening over an adhesion/barrier layer of titanium/titanium nitride (Ti/TiN). Such adhesion/barrier layers are needed because of the extremely poor adhesion of tungsten applied by chemical vapor deposition (CVD) on such dielectrics as borophosphosilicate glass (BPSG), silicon dioxide, thermal oxide, and plasma-enhanced oxide and silicon nitride. However, it is known that tungsten adheres well to TiN and that TiN adheres well to Ti and that Ti, in turn, adheres well to the dielectrics listed. Thus, a method that achieves good adhesion of CVD tungsten to the substrate is achieved by interposing layers of titanium and titanium nitride between the dielectric and the tungsten plug.

However, the prior art W plug processes can be improved upon.

The importance of overcoming the various deficiencies noted above is evidenced by the extensive technological development directed to the subject, as documented by the relevant patent and technical literature. The closest and apparently more relevant technical developments in the patent literature can be gleaned by considering the following.

US6001726: Method for using a conductive tungsten nitride etch stop layer to form conductive interconnects and tungsten nitride contact structure - forming a contact structure for a shallow junction device - Inventor: Nagabushnam, Rajan.

US6573147: Method of forming a semiconductor device having contact using crack-protecting layer - Formation of contact involves forming crack-protecting layer on interlayer dielectric layer - Inventor: Moon, Kwang-jin; Yongin,

US20030203512A1: METHOD FOR FABRICATING SEMICONDUCTOR MEMORY DEVICE - Manufacture of semiconductor memory device, e.g. dynamic random access memory, by sequentially forming insulating layer, contact hole, first diffusion barrier, conductive layer, and conductive plug in semiconductor substrate.

US5913143: Method of making a multilayer interconnection of semiconductor device using plug. Inventor: Harakawa, Hideaki.

Summary of the Invention

The below presents a simplified summary in order to provide a basic understanding of some aspects of example embodiments of the invention. This summary is not an extensive overview of the invention. It is intended neither to identify key or critical elements nor to delineate the scope of the embodiments. Rather, the primary purpose of the summary is to present some example concepts of the invention in a simplified form as a prelude to the more detailed description that is presented later.

The example embodiments of the present invention provides a structure and a method of manufacturing a contact with a barrier layer which is characterized as follows.

A first example embodiment of a method of fabrication of a semiconductor device; comprises the following :

- forming dielectric layer over a semiconductor substrate;
- forming a contact hole in said dielectric layer;

- forming a first barrier layer over said dielectric layer and said substrate in said contact hole; said first barrier layer is comprised of Ta;
- forming a second barrier layer over said first barrier layer; said second barrier layer is comprised of TaN or WN;
- forming a first conductive layer over said second barrier layer at least filling said contact hole;
- chemical-mechanical polishing said first conductive layer to form a first contact plug in said contact hole;
- in a cleaning step, cleaning said contact plug, said first barrier layer, said second barrier layer and said dielectric layer using an etch.

An aspect of the first example embodiment comprises:

- the cleaning step preferably comprises a Cl and B chemistry.

An aspect of the first example embodiment comprises:

- forming a second dielectric layer over said first dielectric layer and said first contact plug;
- forming an interconnect opening in said second dielectric layer exposing said contact plug;
- forming an interconnect in said interconnect opening contacting said contact plug.

A second example embodiment of a method of fabrication of a semiconductor device comprise;

- forming dielectric layer over a semiconductor substrate;
- forming a contact hole in said dielectric layer;
- forming a first barrier layer over said dielectric layer and said substrate in said contact hole; said first barrier layer is comprised of tungsten nitride;
- forming a first conductive layer over said first barrier layer at least filling said contact hole;
- chemical-mechanical polishing said first conductive layer to form a first contact plug in said contact hole;
- in a cleaning step, cleaning said contact plug, said first barrier layer, said second barrier layer and said dielectric layer using an etch;

An aspect of the first example embodiment comprises:

- the cleaning step preferably comprises a Cl and B chemistry.

An aspect of the second embodiment comprises:

- forming a second dielectric layer over said first dielectric layer and said first contact plug;

- forming an interconnect opening in said second dielectric layer exposing said contact plug;
- forming an interconnect in said interconnect opening contacting said contact plug.

The above and below advantages and features are of representative embodiments only, and are not exhaustive and/or exclusive. They are presented only to assist in understanding the invention. It should be understood that they are not representative of all the inventions defined by the claims, to be considered limitations on the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages may be mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of the claimed invention have not been discussed herein. However, no inference should be drawn regarding those discussed herein relative to those not discussed herein other than for purposes of space and reducing repetition. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

Brief Description of the Drawings

The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figures 1 through 4 are cross sectional views for illustrating a method for manufacturing contact according to an first example embodiment of the present invention.

Figures 5 through 8 are cross sectional views for illustrating a method for manufacturing contact according to an second example embodiment of the present invention.

Figures 9A, 9B and 10 are cross sectional views for illustrating a method for manufacturing contact according to an process known by the inventors (not prior art).

Detailed Description of the Example Embodiments

All embodiments described are example embodiments. An example embodiment may contain elements of several claimed embodiments. The claims define the embodiments of the invention.

First example embodiment

A first example embodiment is shown in figures 1 through 4. The first embodiment comprises (a) a contact plug that can be comprised of a Ta lower barrier layer and an upper barrier layer(s) comprised of TaN or WN and (b) a post CMP cleaning process.

Referring to figure 1, we provide a semiconductor structure 10 such as a Si wafer.

We can provide devices on or in the semiconductor structure. For example, we can form a transistor. The transistor can be comprised of at least some of the

following: a gate dielectric 30, gate electrode 32, gate silicide cap 40, sidewall spacer(s) 38, SDE (source drain extensions) 22 and source and drain regions 20, and S/D silicide regions 28.

We can form an etch stop layer 41 over the devices and substrate surface. The etch stop layer 41 can be comprised of silicon nitride.

Next, we form a dielectric layer (e.g., ILD layer) 43 over the semiconductor substrate 10. The dielectric layer can be comprised of silicon oxide, undoped silicon dioxide or SiO_2 doped with B &/or P and preferably of undoped silicon dioxide.

Next, we can form contact holes 42A 42B through the dielectric layer to expose the substrate or silicide 28 (if present). Contact hole 42B will be used to form a connection between the S/D region 20 and the gate silicide 40 using a subsequently formed plug. Contact hole 42A will be used to form a connection between the S/D region 20 and a higher metal layer using a subsequently formed plug.

A. First barrier layer (e.g., Ta)

Then we form a first barrier layer 44 over the dielectric layer 43 and the substrate 10 in the contact holes 42A 42B. Preferably the first barrier layer can be comprised of Ta and is preferably comprised essentially of Ta. The Ta is

preferably formed by a physical vapor deposition process (PVD) and can have a thickness between 10 and 100 angstroms over the dielectric layer 43.

B. second barrier layer (e.g., TaN or WN)

Still referring to figure 1, we form a second barrier layer 48 on the first barrier layer 44.

The second barrier layer 48 can be comprised of TaN (tantalum nitride) or WN (tungsten nitride) and combinations thereof and preferably consists essentially of TaN or WN. The TaN can be formed by a physical vapor deposition process (PVD) or Chemical vapor deposition process (CVD). The WN can be formed by a physical vapor deposition process (PVD) or chemical vapor deposition process (CVD).

The second barrier layer 48 can have a thickness between 10 and 500 angstroms over the dielectric layer.

C. first conductive layer

Then we form a first conductive layer (not shown) on the second barrier layer 48 at least filling the contact holes 42A 42B.

The first conductive can be comprised of tungsten (W) and is most preferably consists essentially of W. The W layer can be formed by forming a W nucleating layer and then forming a W layer using a CVD deposition process. The first conductive layer can be formed over top of the dielectric layer.

D. Planarize the first conductive layer

Referring to figure 2, we planarize the first conductive layer and remove the barrier layer from over the top of the dielectric layer preferably using a chemical-mechanical polishing (CMP) process to form first contact plugs 52 in the contact holes.

E. Cleaning step (e.g., touch up etch)

Referring to figure 3, we perform a touch up etch to try to remove any W residue on the top surface (such as of dielectric layer 43 and plug) after the CMP. To clean, we can reactive ion etch the contact plug, the first barrier layer, the second barrier layer and the dielectric layer.

The W touch up RIE can be done in any metal etch RIE tool. The main etch chemistry comprise a Cl and B containing etch and is more preferably a Cl_2 and BCl_3 containing etch chemistry.

A feature of the embodiment's Cl and B containing etch is that the etch rate of the first barrier layer 44 (e.g., Ta) and the second barrier layer 48 (e.g., TaN or WN) is similar or about equal to (e.g., within +/- 5%) the etch rate of W. The etch time can be between 1 and 2 minutes. The etch can removed a thickness of the W contact plug 52 between about 200 to 500 A and an oxide 43 thickness between about 300 to 800 A.

The etch parameters are preferably set to get the etch rates of the dielectric layer (e.g., oxide) the barrier layers and the plug (e.g., w) with 10 % and more preferably within 5%.

Figure 3 shows top surfaces 56 of the barrier layers and the absence of the "slit" (such as the etching of the barrier layers 44 48 selective to the W plug and the dielectric layer).

The embodiment's refractory metal nitrides barrier layers (e.g., TaN and WN) have a better etch resistance to the W touch up etch (comprised of Cl and B) than barrier layers comprised of Ti or/and TiN.

F. second dielectric layer

Higher level dielectric layers and interconnect layers can be formed thereover.

Referring to figure 4, we form a second dielectric layer 70 over the first dielectric layer 43 and the first contact plugs 52.

We can form an interconnect opening in the second dielectric layer 70 exposing the contact plug 52.

We can form interconnects (M1) (74 76) in the interconnect openings contacting the contact plugs 52. The interconnects 74 76 can be comprised of a upper barrier layer 74 and upper conductive interconnects 76. The upper barrier layer 74 can be comprised of Ta or TaN. Preferably the upper barrier layer 74 is comprised of a first upper barrier layer and a second upper barrier layer over the first upper barrier layer. The first upper barrier layer can be compromise of Ta and the second upper barrier layer can be comprised of TaN The upper barrier layer can have a thickness between 10 and 500 angstroms.

The upper conductive interconnects 76 can be comprised of Cu.

The device can be further processed using conventional processes.

The embodiments' barrier layers 44 48 that are resistant to the W touch up RIE prevent shorts between the M1 to polysilicon.

II. second example embodiment (e.g., WN barrier layer)

A second example embodiment uses a barrier layer comprised of WN. Figures 5 thru 8 show the second example embodiment. Similar elements can have the same characteristics as described above for the first embodiment.

We provide a semiconductor structure 10 such as a Si wafer.

We can provide devices on or in the semiconductor structure. For example, we can form a transistor that can be comprised of: a gate dielectric 30, gate electrode 32, gate silicide 40; sidewall spacer(s) 38, SDE 22 and source and drain regions 20; and S/D silicide regions 28.

We can form an etch stop layer 41 over the devices and substrate surface. The etch stop layer 41 can be comprised of silicon nitride.

Next, we can form a dielectric layer 43 over a semiconductor substrate 10. The dielectric layer 43 can be comprised of silicon oxide.

Next, we can form contact holes 42A 42B through the dielectric layer to expose the substrate or silicide 28 (if present). Contact hole 42B shows a subsequent connection between the S/D region 20 and the gate silicide 40.

A. barrier layer – WN

Still referring to figure 5, we form a first barrier layer 49 over the dielectric layer 43 and the substrate 10 in the contact holes 42A 42B. The first barrier layer 49 can be comprised of WN (tungsten nitride) and preferably consists essentially of tungsten nitride WN. The WN barrier layer can be formed by a chemical vapor deposition process (CVD), Atomic layer deposition process (ALD), or a physical vapor deposition process (PVD). The barrier layer can have a thickness between about 10 and 500 angstroms over the dielectric layer.

B. contact

We form a first conductive layer (not shown) on the first barrier layer at least filling the contact hole. The first conductive is comprised of tungsten (W) and most preferably W.

Referring to figure 6, we can chemical-mechanical polish (CMP) the first conductive layer to form a first contact plugs 52 in the contact holes. The CMP also preferably removes the first barrier layer 49 on the top of the dielectric layer 43. The CMP process can leave some contaminants on the resulting surfaces.

C. clean step - touch up etch

Referring to figure 7, we can clean or touch up the surfaces to remove any contaminates and resides left by the previous processes such as the CMP. We

can reactive ion etch the contact plug, the first barrier layer, the second barrier layer and the dielectric layer to remove contaminates such as W particles after the W CMP.

The touch up RIE process can be the same as describe above in the first embodiment.

Figure 7 shows top surfaces 56 of the barrier layers are about even with the top surfaces of the W plug 52 and the dielectric layer 43. Also note the absence of a sidewall "slit" between the plug 52 and the dielectric layer 43 (etching of the barrier layer 49 selective to the W plug and the dielectric layer) that can cause problems. The barrier layer, the dielectric layer and the plug have about the same etch rates (preferably within +/- 5 %) in the RIE touch up clean etch comprising B and Cl.

The etch parameters are preferably set to get the etch rates of the dielectric layer (e.g., oxide) the barrier layers and the plug (e.g., W) +/- within 10 % and more preferably within +/- 5%.

D. upper interconnect (e.g., M1)

Referring to figure 8, we form a second dielectric layer 70 over the first dielectric layer 43 and the first contact plugs 52.

Next we form an interconnect opening in the second dielectric layer exposing the contact plug.

We form an interconnect 74 76 in the interconnect opening contacting the contact plug. The interconnects 74 76 can be comprised of a upper barrier layer 74 and upper conductive interconnects (e.g., Cu) 76. The upper barrier layer 74 and upper interconnect can be made as described above in the first embodiment.

The device can be further processed using conventional processes.

E. a problem some example embodiments could solve

Referring now to the drawing and more particularly to figures 9A, 9B and 10, there is shown a contact structure over which some of the example embodiments of the present invention are an improvement. It is to be understood in this regard that no portion of Figs 9A, 9B and 10 are admitted to be prior art as to the present invention. Figures 9A, 9B and 10 are not prior art. Rather, this highly simplified diagram is an effort to provide an improved understanding of possible problems that are overcome by the some of the example embodiments of teh invention.

Figure 9A shows a cross sectional view of a contact plug 52 and barrier film 104 106 after W plug 52 CMP.

Figure 9B shows a cross sectional view of a contact plug 52 and barrier film 104 106 after a RIE touch up etch (e.g., Cl_2 and BCl_3 chemistry). The barrier film is

comprised of a first barrier layer 104 comprised of Ti and a second overlying barrier layer 106 comprised of TiN. A W plug is formed in the opening over the barrier film 104 106.

As shown figure 9B, the RIE etches the barrier film 104 106 at a fairly fast rate compared to the dielectric layer 43 and W plug 52 to form sidewalls slits 110. The etch rates of Ti and TiN (barrier layers 104 106) in Cl_2 and BCl_3 etch chemistries are at least 2 times faster (e.g., 200%) than that of W (W plug 52).

The slit is bad because it may cause the M1 overetch into contact dielectric layer 43 which may result in a M1 to polysilicon short.

Referring to figure 10, we can see that the M1 litho and RIE (reactive ion etch) provide an excessive over etch that creates a hole 200 in the dielectric layer near the sidewall slit because the slit allowed the RIE to start deep below the dielectric layer surface. This can cause an upper interconnect 76 to gate 32 short. In some cases, the distance (dielectric layer 43 thickness) between bottom of M1 line 76 and top poly gate 32 can be as small as 500 A. The sidewall slit and subsequent over etch can cause the upper interconnect 76 to gate 32 short.

III. aspects of the example embodiments

The example embodiments of the invention form barrier layers under a W contact plug. The barrier layers are resistant to a particular RIE etch used on a W touch up etch after a W plug CMP step. The combination of the compositions of the barrier layers (e.g., Ta, TaN and WN) and the W touch up RIE etch chemistry (e.g., Cl and B) prevent the problem of a slit formation that can cause shorts.

A. non-limiting example embodiments

In the above description numerous specific details are set forth such as flow rates, pressure settings, thicknesses, etc., in order to provide a more thorough understanding of the present invention. Those skilled in the art will realize that power settings, residence times, gas flow rates are equipment specific and will vary from one brand of equipment to another. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these details. In other instances, well known process have not been described in detail in order to not unnecessarily obscure the present invention.

Given the variety of embodiments of the present invention just described, the above description and illustrations show not be taken as limiting the scope of the present invention defined by the claims.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. It is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

CLAIMS

1. A method of fabricating an integrated circuit comprising:

providing a substrate prepared with a dielectric layer with a contact plug opening;

lining the contact plug opening with a barrier layer; and

filling the contact plug opening with a conductive material to form a contact plug in the contact plug opening;

polishing the substrate, wherein polishing produces a top surface of the contact plug which is coplanar with top surfaces of the barrier layer and dielectric layer; and

cleaning with a touch up etch after polishing to remove residue of the conductive material on the dielectric layer, wherein the touch up etch etches the barrier layer and conductive material at similar etch rates to avoid corrosion of the barrier layer which causes contact plug sidewall slit.

2. The method of claim 1 wherein the conductive material filling in the contact plug opening comprises tungsten.

3. The method of claim 1 wherein:

the conductive material comprises a non-copper conductive material; and

the barrier layer comprises refractory metal or nitrides thereof including Ta, TaN, WN or a combination thereof.

4. The method of claim 3 wherein an etch chemistry of the touch up etch comprises Cl and B.

5. The method of claim 1 comprises forming a sub-barrier layer between the dielectric layer and the barrier layer.

6. The method of claim 5 wherein an etch chemistry of the touch up etch comprises Cl and B.

7. The method of claim 5 wherein the sub-barrier layer comprises Ta.

8. The method of claim 7 wherein an etch chemistry of the touch up etch comprises Cl and B.

9. A method of fabricating a semiconductor device comprising:

providing a substrate prepared with circuit elements thereon;

forming a dielectric layer on the substrate;

patterning the dielectric layer to form a contact plug opening;

lining the contact plug opening with a barrier layer;

forming a contact plug in the opening, wherein the contact plug comprises a barrier layer lining the opening and a conductive material filling the contact opening, the conductive material having a top surface coplanar with top surfaces of the barrier layer and dielectric layer from polishing; and

cleaning with a touch up etch after polishing to remove residue of the conductive material on the dielectric layer, wherein the touch up etch etches

the barrier layer and conductive material at similar etch rates to avoid corrosion of the barrier layer which causes contact plug sidewall slit.

10. The method of claim 9 wherein the etch rates of the conductive material and the barrier layer are within 10% of each other during cleaning.

11. The method of claim 9 wherein the barrier layer comprises refractory metal or nitrides thereof including Ta, TaN, WN or a combination thereof, and the method comprises forming a sub-barrier layer between the dielectric layer and the barrier layer.

12. The method of claim 11 wherein the sub-barrier layer has an etch rate substantially similar to that of the conductive material and the barrier layer during cleaning.

13. The method of claim 11 wherein the sub-barrier layer has an etch rate within 10% of that of the conductive material and the barrier layer during cleaning.

14. A method of fabricating a semiconductor device comprising:

providing a substrate prepared with circuit elements thereon;

forming a dielectric layer on the substrate;

patterning the dielectric layer to form a contact plug opening;

depositing a barrier layer on the substrate, the barrier layer lining the contact plug opening;

depositing a conductive material to fill the contact plug opening;

polishing the substrate to remove excess conductive material and barrier layer over the dielectric layer to form a contact plug in contact with the barrier layer, wherein a top surface of the contact plug is coplanar with top surfaces of the barrier and dielectric layers; and

cleaning with a touch up etch after polishing to remove residue of the conductive material on the dielectric layer, wherein the touch up etch etches the barrier layer and conductive material at similar etch rates to avoid corrosion of the barrier layer which causes contact plug sidewall slit.

15. The method of claim 14 wherein the barrier layer comprises refractory metal or nitrides thereof including Ta, TaN, WN or a combination thereof, and the method comprises forming a sub-barrier layer between the dielectric layer and the barrier layer.

16. The method of claim 15 wherein the sub-barrier layer has an etch rate substantially similar to that of the conductive material and the barrier layer during cleaning of the contact plug.

17. The method of claim 9 wherein an etch chemistry of the touch up etch comprises Cl and B.

18. The method of claim 10 wherein an etch chemistry of the touch up etch comprises Cl and B.

19. The method of claim 11 wherein an etch chemistry of the touch up etch comprises Cl and B.

20. The method of claim 14 wherein the etch rates of the conductive material and the barrier layer are within 10% of each other during cleaning.

21. The method of claim 16 wherein the sub-barrier layer has an etch rate within 10% of that of the conductive material and the barrier layer during cleaning.

22. A method of fabricating a device comprising:

providing a substrate prepared with a first layer;

patterning the first layer to form an opening; and

forming a fill in the opening, the fill comprises a liner layer lining the opening and a second material filling the opening, wherein top surfaces of the liner layer, second material, and first layer are coplanar,

wherein the liner layer and the second material can be etched with similar etch rates during a subsequent touch up etch to remove residue of the second material on the first layer to avoid formation of sidewall slits due to corrosion of the liner layer.

23. The method of claim 22 wherein the opening comprises a contact plug opening and filling the contact plug opening forms a contact plug.

24. The method of claim 23 further comprises:

polishing the second material to form the contact plug; and

performing the subsequent touch up etch to remove residue of the second material on the first layer.

25. The method of claim 24 wherein an etch chemistry of the touch up etch comprises Cl and B.

26. The method of claim 22 wherein:

the first material comprises a dielectric material;

the liner layer comprises a refractory metal or nitrides thereof including Ta, TaN, WN or a combination thereof; and

the second material comprises a conductive material including tungsten.

27. The method of claim 26 further comprises:

polishing the second material to form the contact plug; and

performing the subsequent touch up etch to remove residue of the second material on the first layer.

28. The method of claim 27 wherein an etch chemistry of the touch up etch comprises Cl and B.

29. A method of fabricating a semiconductor device comprising:

providing a substrate prepared with a dielectric layer with a contact plug opening;

lining the contact plug opening with a barrier layer comprising refractory metal or nitrides thereof including Ta, TaN, WN or a combination thereof;

filling the contact plug opening with a non-copper conductive material comprising W to form a contact plug in the contact plug opening;

polishing the substrate, wherein a top surface of the contact plug is coplanar with top surfaces of the barrier layer and dielectric layer; and

cleaning with a touch up etch after polishing to remove residue of the conductive material on the dielectric layer, wherein the touch up etch etches the barrier layer and conductive material at similar etch rates to avoid contact plug sidewall slit formation.