close proximity to grounded surfaces or conductors. For example, in 277 V phase-to-ground, three-phase, multiple feeder systems having one phase faulted to ground, the magnitude of the capacitive charging currents on the unfaulted phases of the non-affected feeders can easily reach a magnitude that will "false trip" the non-affected feeders' GFCIs.

[0004] As such, a need exists for a GFCI system that can provide improved tripping "intelligence" or "security" for polyphase power systems at all system voltage levels, and in particular, polyphase power systems operating above 125V phase-to-ground.

[0005] A further need exists for an improved GFCI system for three-phase, multi-feeder systems having a ground-fault sensor (GFS) sensitivity corresponding to the lower limit of the human "let-go" threshold of current, i.e., 4-6 mA, which will reliably trip on the affected feeder(s) without causing false interruptions on the unaffected feeder(s). GFSs designed to trip at such low currents typically include current transformers that may be susceptible to magnetic saturation due to high-level ground current conditions on involved branch or feeder circuits. Magnetic saturation of the transformers may cause the corresponding GCFIs to falsely trip non-faulted circuits.

SUMMARY OF THE INVENTION

[0006] In one aspect, there is provided a ground-fault circuit-interrupter (GFCI) system for a polyphase power supply and a main bus circuit coupled thereto, the main bus circuit having a plurality of individual feeder circuits, the GFCI system comprising: a voltage unbalance detection device coupled to the power supply and the main bus circuit for detecting a voltage unbalance among phases of the power supply; a plurality of GFCI units respectively associated with the main bus and each one of the feeder circuits, each of the GFCI units being operative to generate a fault signal corresponding to a fault condition through an associated main bus or feeder circuit; and a processor in communication with the voltage unbalance detection device and each of the GFCI units for monitoring the voltage unbalance and fault

signals generated by the each of the GCFI units, and processor being capable of generating one or more trip signals corresponding to an actual fault based at least in part on certain predetermined relationships between the voltage unbalance and fault signals.

[0006a] In another aspect, there is provided a computer-implemented method for ground-fault circuit-interruption (GFCI) of a polyphase power supply and a main bus circuit coupled thereto, the main bus system having a GFCI unit and plurality of feeder circuits, each of the feeder circuits also having a GCFI unit associated therewith, the method comprising: monitoring a voltage unbalance of the power supply system; monitoring fault signals generated by the several GFCI units; and determining when an actual fault condition exists based on the state of the voltage unbalance and certain predetermined relationships among the fault signal generated by the GFCI unit in the main bus circuit and the fault signals generated by the GFCI units in the feeder circuits.

[0006b] A system and method for ground-fault circuit-interruption is provided for use with a polyphase power supply and a main bus circuit having multiple feeder or branch circuits. The ground-fault circuit-interrupter (GFCI) system includes a voltage unbalance detection device coupled to the power supply and the main bus circuit for detecting a voltage unbalance among the three phase voltages of the polyphase power supply during a fault condition, and a plurality of GFCI units respectively associated with the main bus and each one of the feeder circuits, each of the GFCI units being operative to generate a fault signal corresponding to a

fault condition on the associated feeder or main bus circuit. The system also includes a computer or computational processor in communication with the voltage unbalance detection device and each of the GCFI units for continuously monitoring the voltage unbalance and fault signals generated by the GCFI units.

[0007] In accordance with an embodiment~~aspect~~ of the present invention, the processor is programmed to determine when an actual fault condition exists based on a state of the voltage unbalance and certain predetermined relationships among the fault signal generated by the GFCI unit in the main bus circuit and the fault signals generated by the GFCI units in the feeder or branch circuits. The logic then determines which of the feeder or branch circuits is experiencing the actual fault condition, which then causes the processor to generate a trip signal to the GFCI unit or units corresponding to the feeder or branch circuit or circuits experiencing the actual fault condition. As such the corresponding faulted circuit or circuits are interrupted.

[0008] The logic further causes the processor to generate an inhibit (or "no trip") signal to the remainder of the GFCIs at the feeder or branch circuits, which are not experiencing the actual ground fault condition, thereby causing those non-faulted circuit or circuits to be inhibited from interruption.

[0009] The GFCI system in accordance with embodiments of the present invention can more reliably disconnect power from a faulted feeder circuit without causing the interruption of the other "healthy" feeder circuits. Embodiments of t~~T~~he present invention provides a GFCI system that can more reliably detect an actual fault, determine the location of the actual fault, and promptly interrupt the faulted circuit as required. Embodiments of t~~T~~he present invention also minimizes false trips of non- faulted circuits, especially those circuits having GFCFs that are subject to power system capacitive charging current influences and GFS magnetic saturation effects during severe phase-to-ground fault events.