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ABSTRACT

An active region (L) with a metal insulator semiconductor field effect transistor (MISFET) (Qs) formed therein for selection of a DRAM memory cell, which makes up a memory cell of the DRAM, is arranged to have an island-like pattern that linearly extends in an X direction on one principal surface of a semiconductor substrate (1). The memory-cell selection MISFET (Qs) has an insulated gate electrode (7) (word line WL) that extends along a Y direction on the principal surface of the semiconductor substrate (1) with the same width kept along the length thereof, which gate electrode is arranged to oppose another gate electrode (7) (word line WL) adjacent thereto at a prespecified distance or pitch that is narrower than said width. In addition, a bit line (BL) is provided overlying the memory-cell select MISFET (Qs) in a manner such that the bit line extends in the X direction on the principal surface of the semiconductor substrate (1) with the same width and opposes its neighboring bit line (BL) at a distance or pitch that is wider than said width.

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