

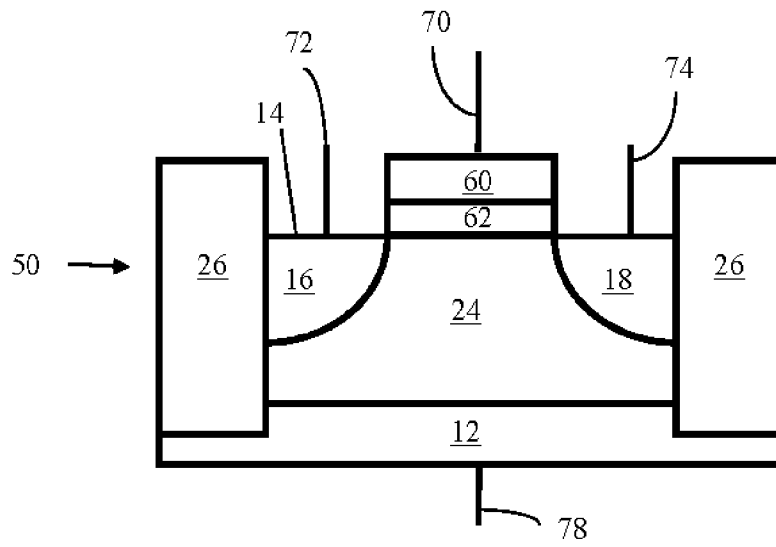


FIG. 1

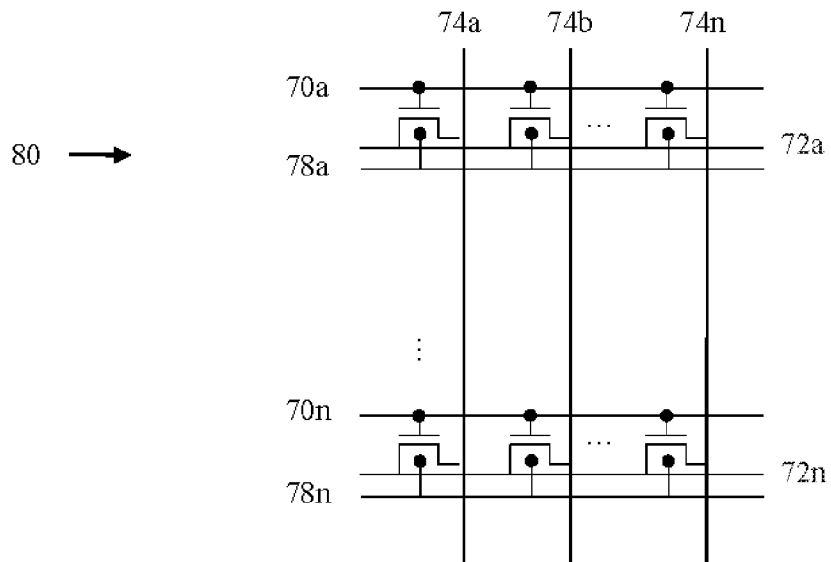


FIG. 2

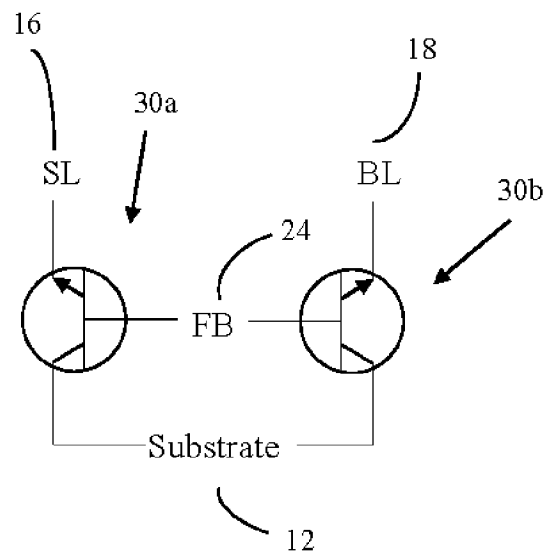


FIG. 3

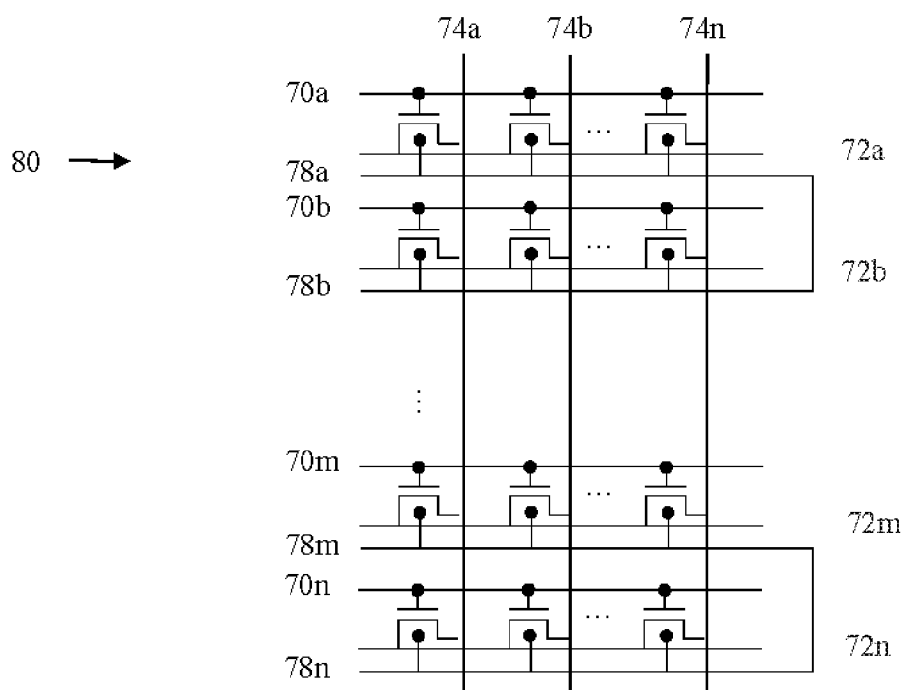


FIG. 4A

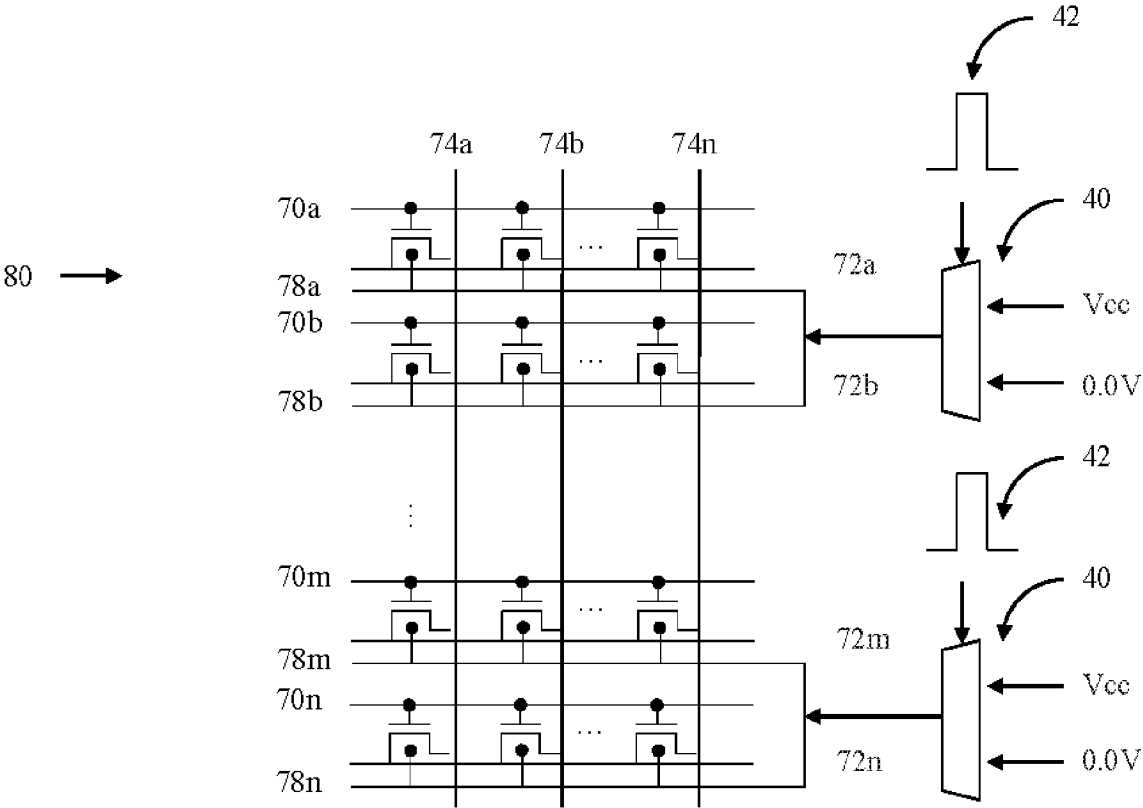


FIG. 4B

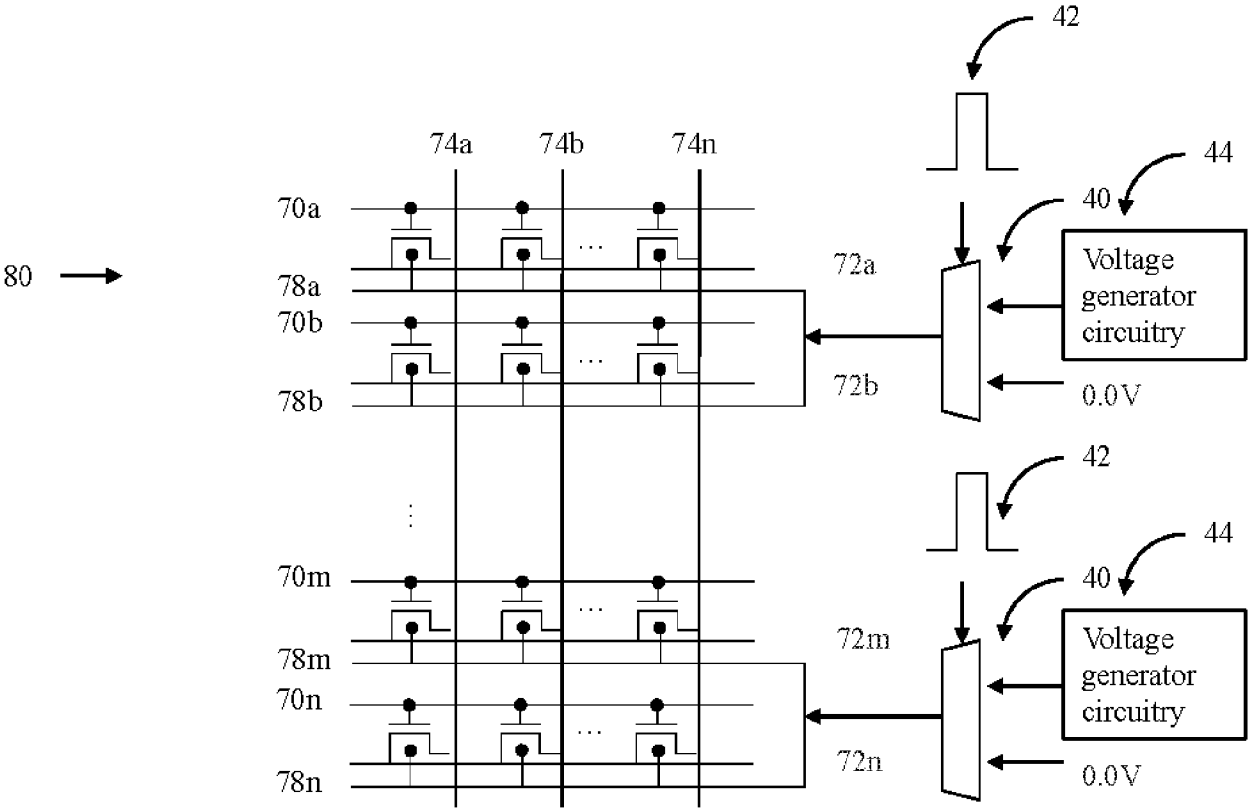


FIG. 4C

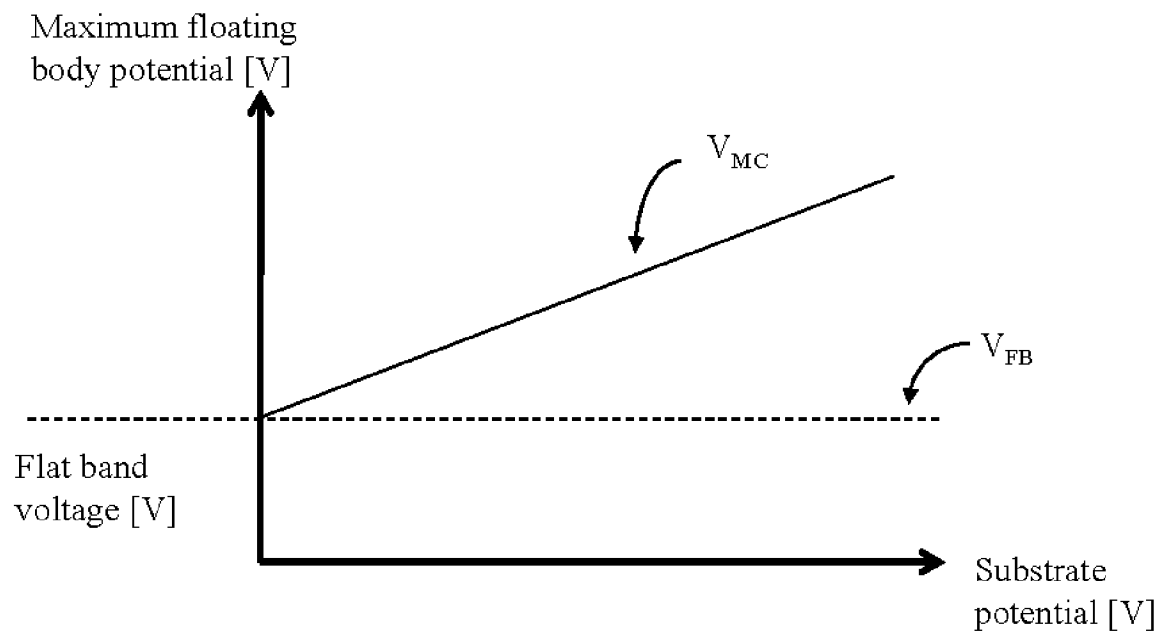


FIG. 5

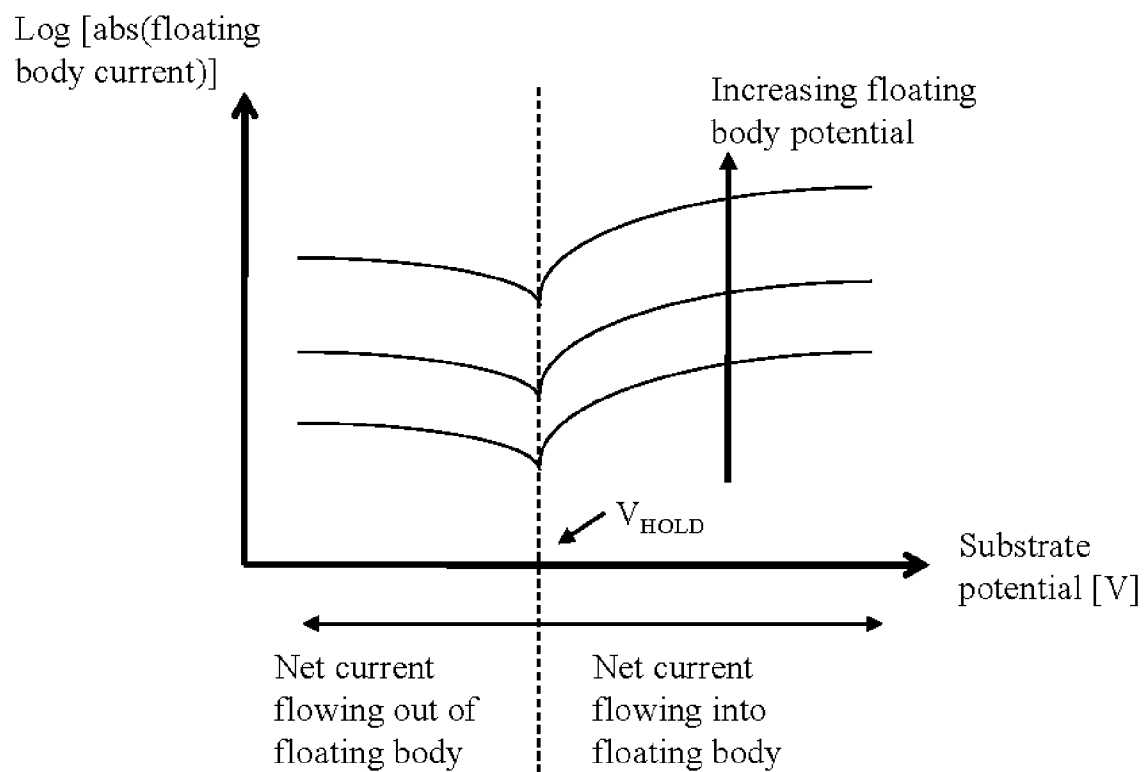


FIG. 6A

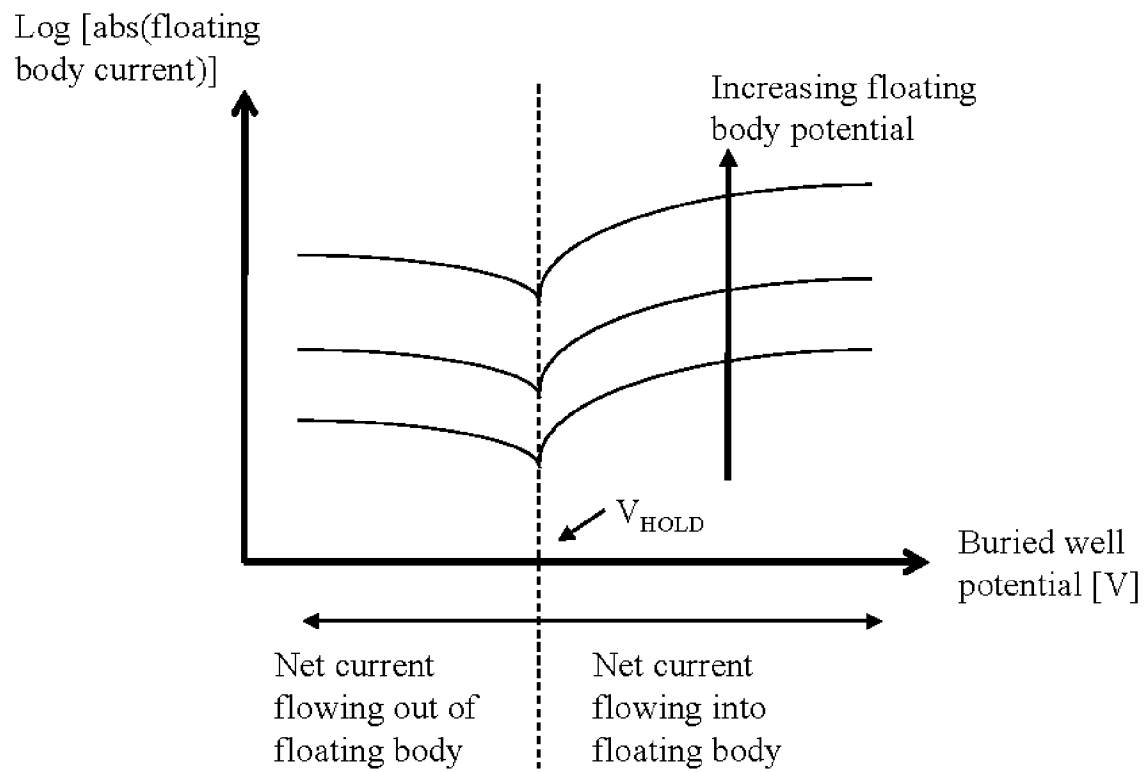


FIG. 6B

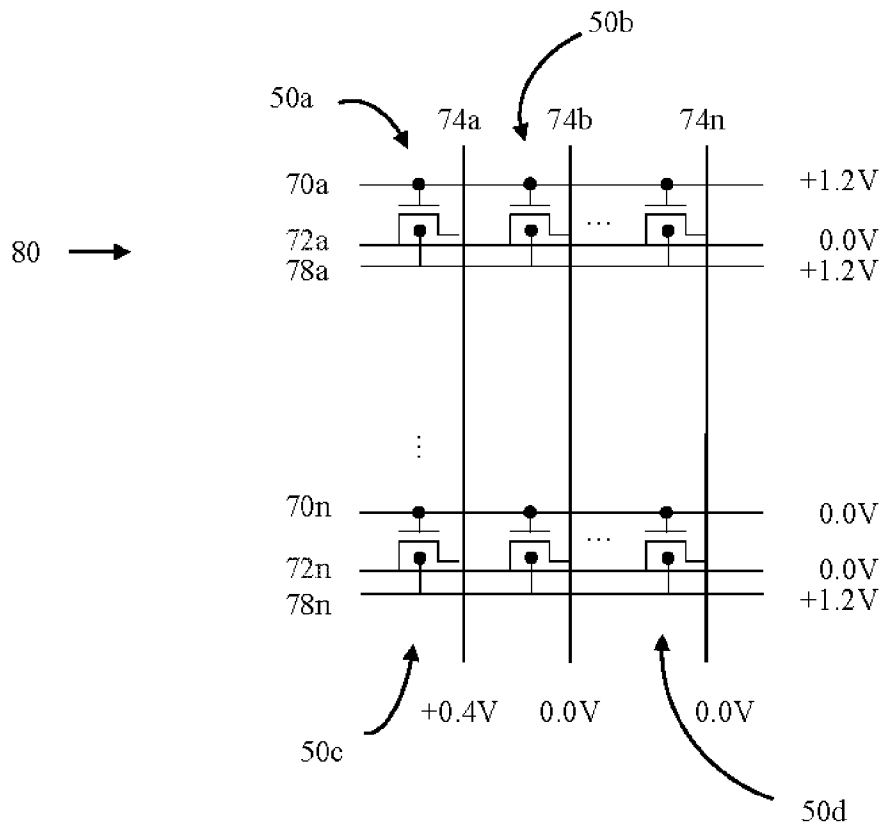
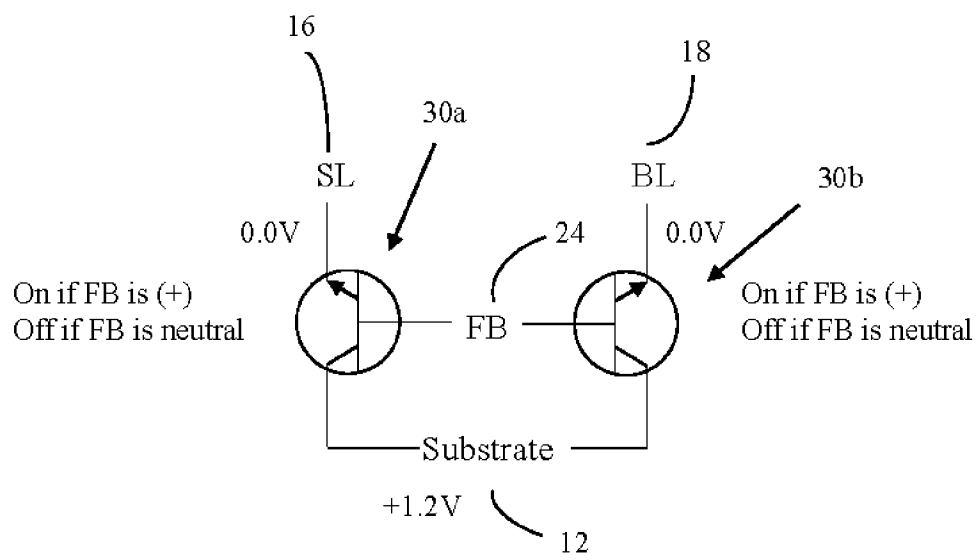


FIG. 7



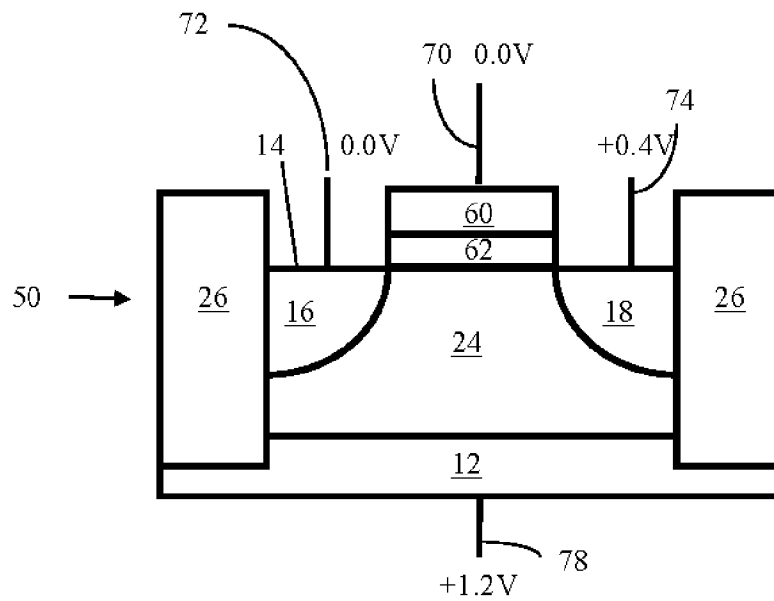


FIG. 8C

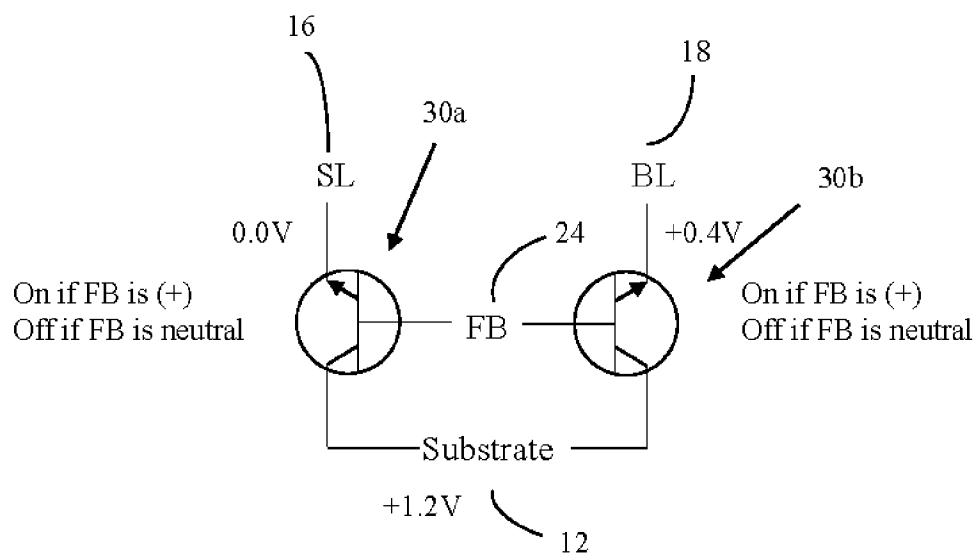
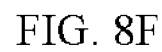


FIG. 8D



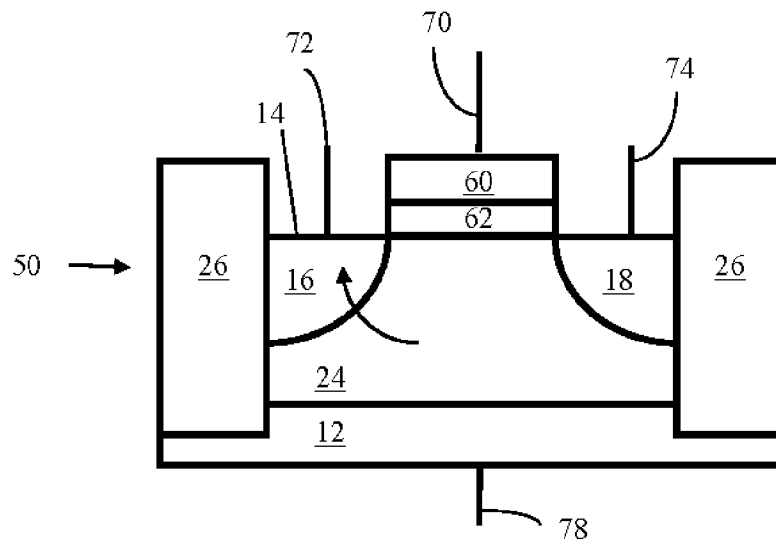


FIG. 9

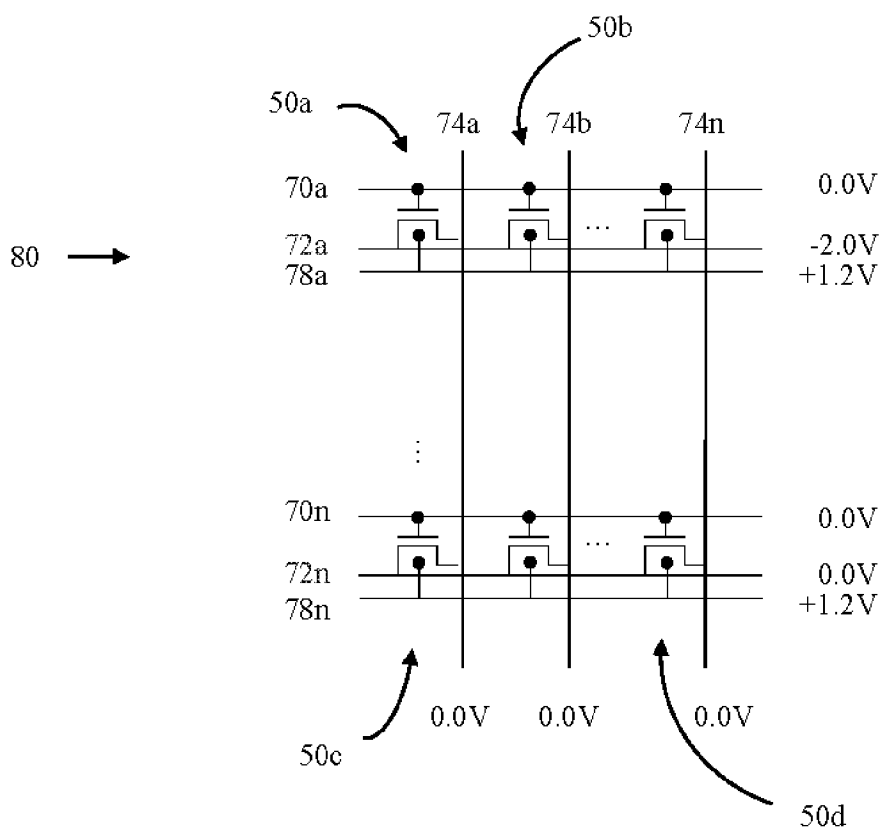


FIG. 10

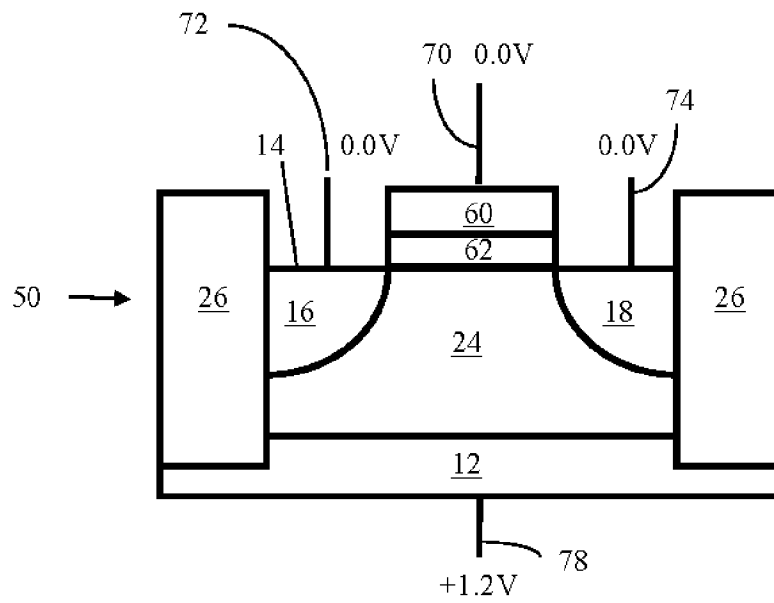


FIG. 11A

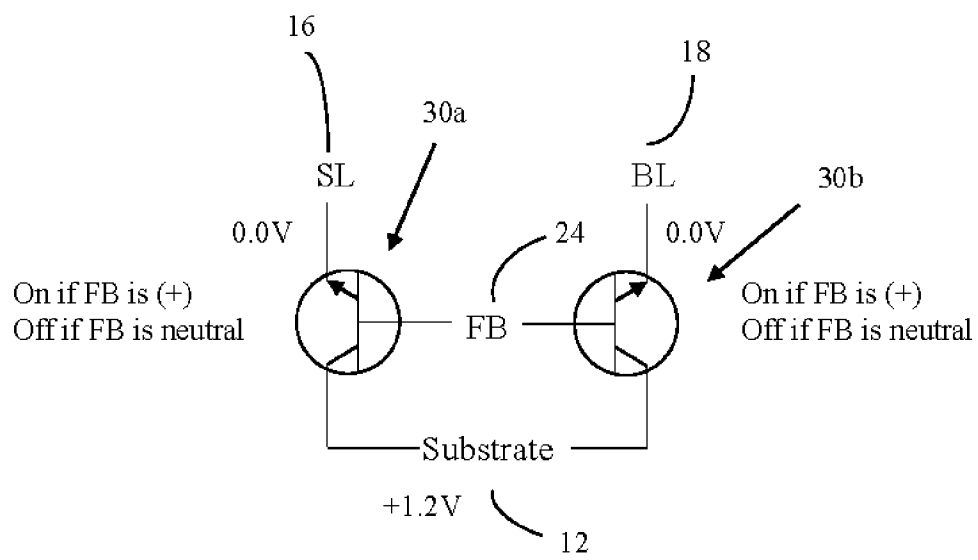


FIG. 11B



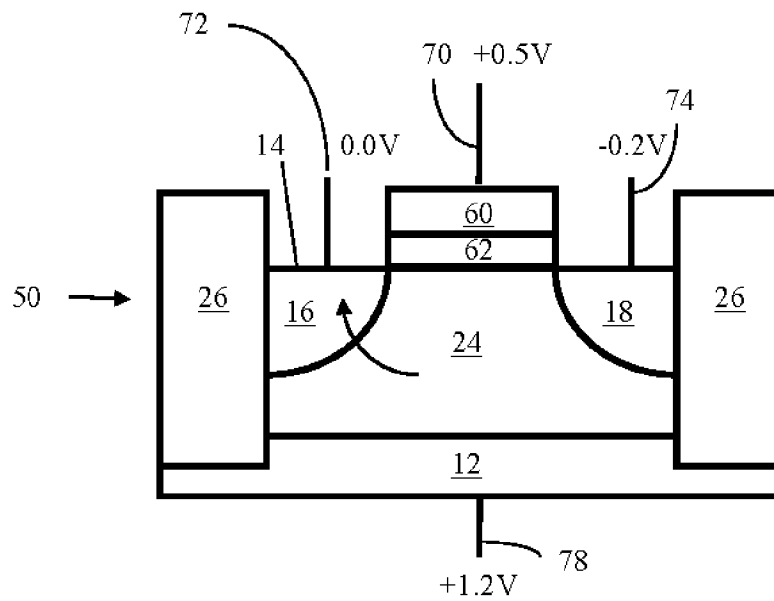


FIG. 13A

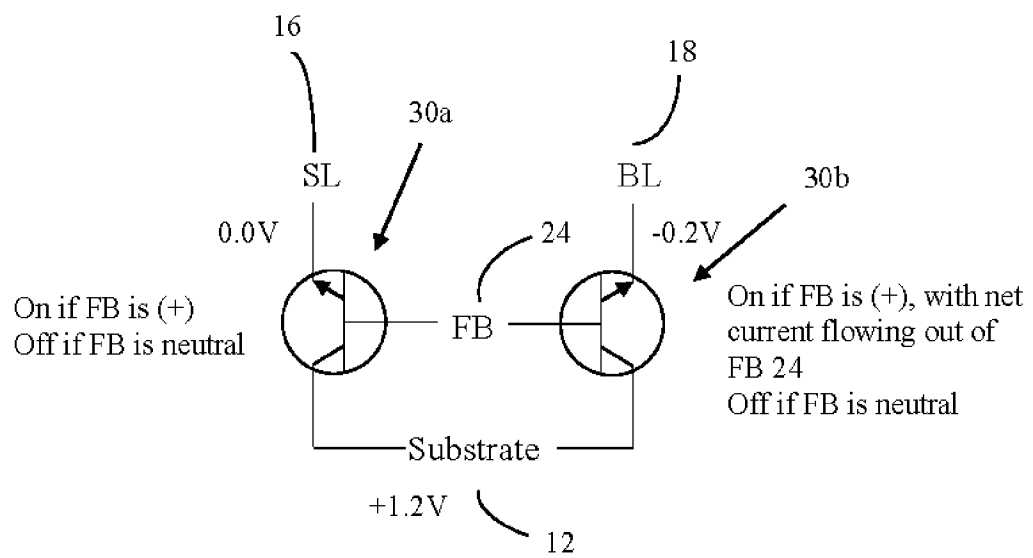


FIG. 13B

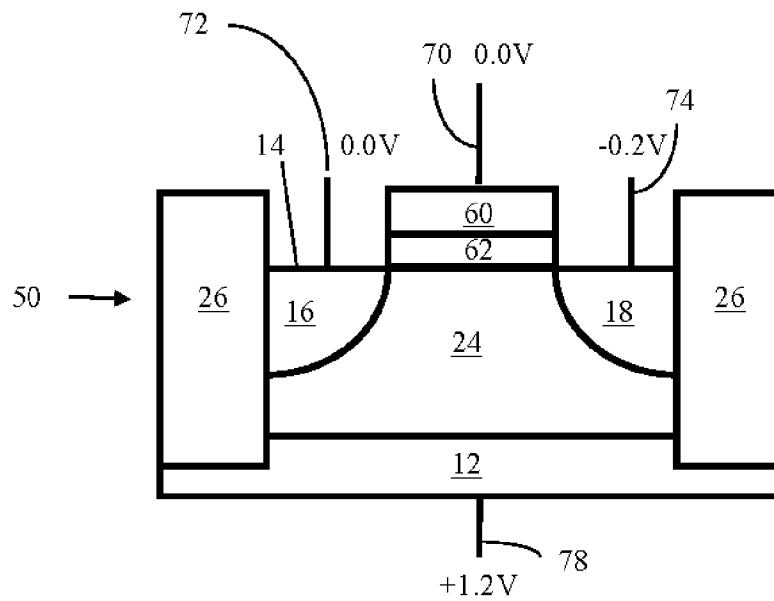


FIG. 13E

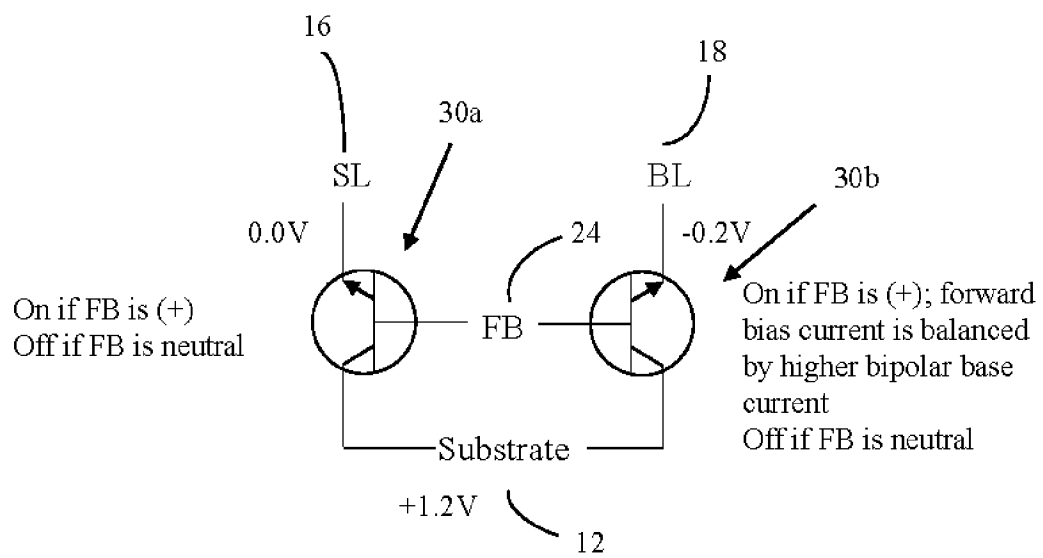


FIG. 13F

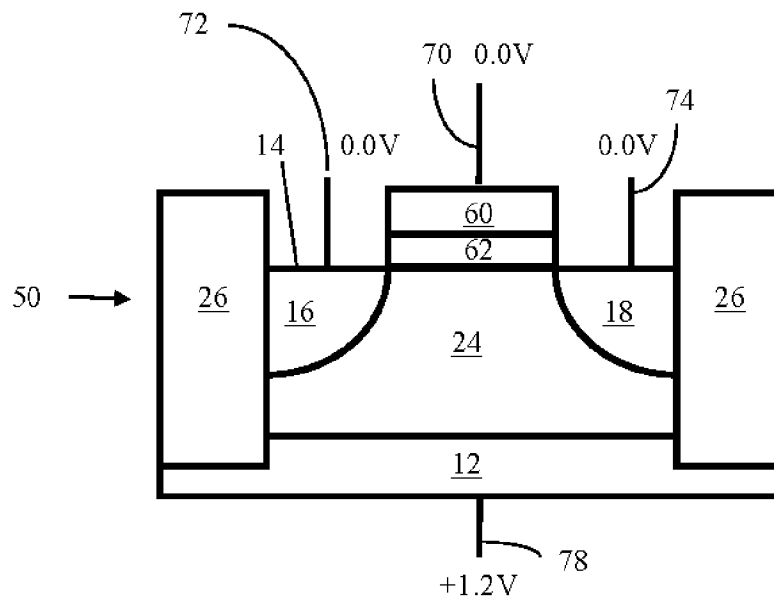


FIG. 13G

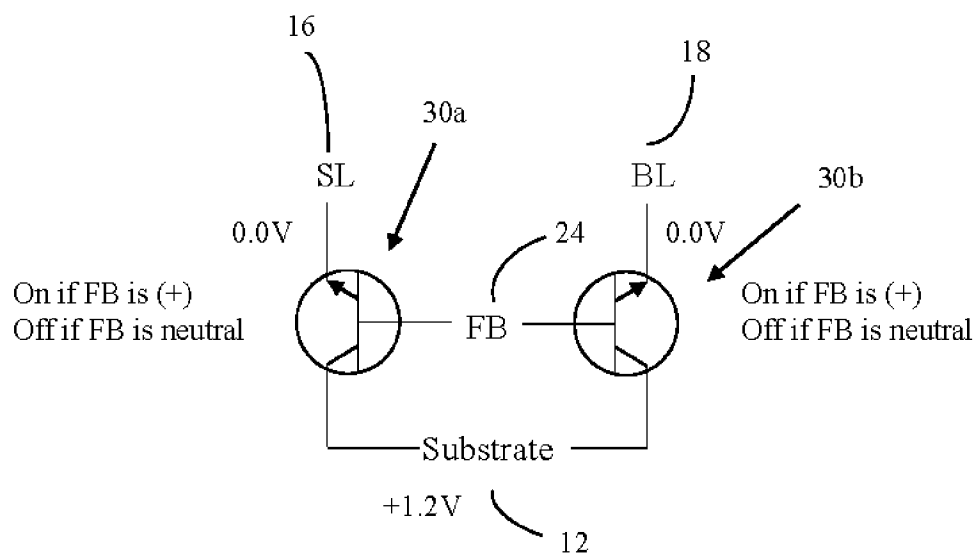


FIG. 13H

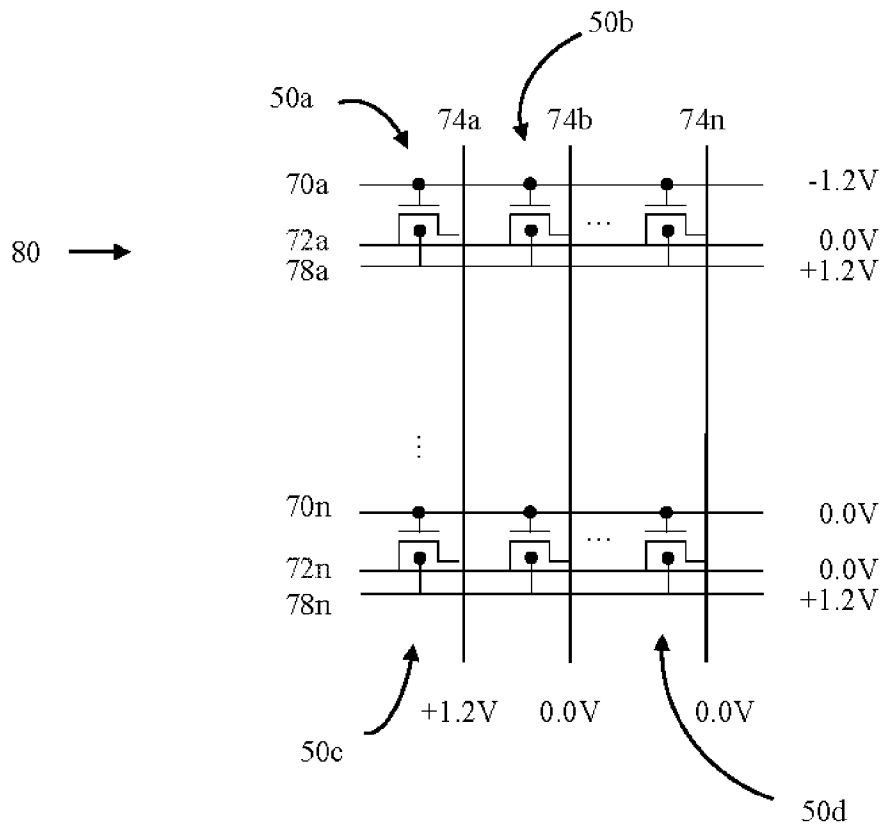
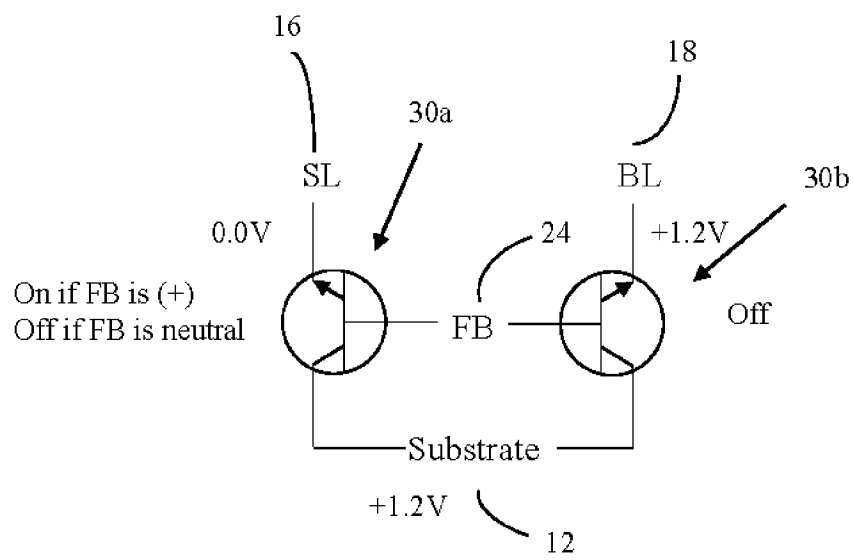


FIG. 14



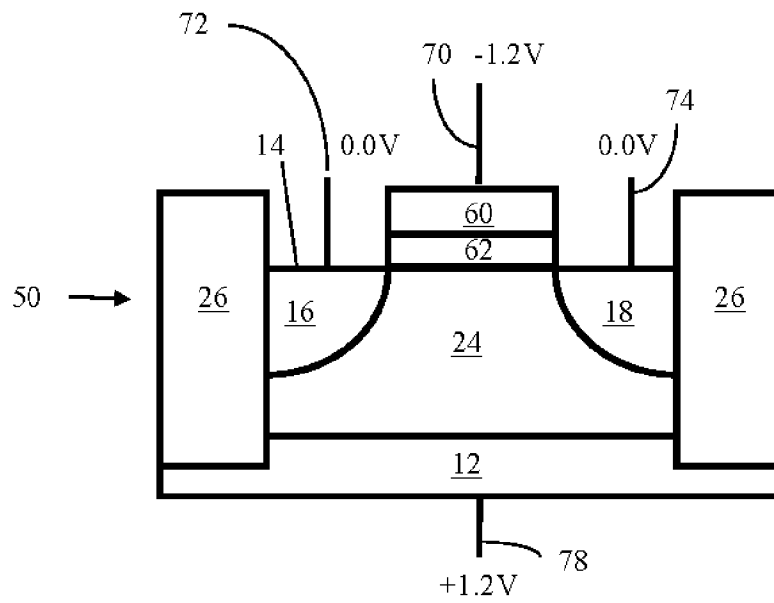


FIG. 15C

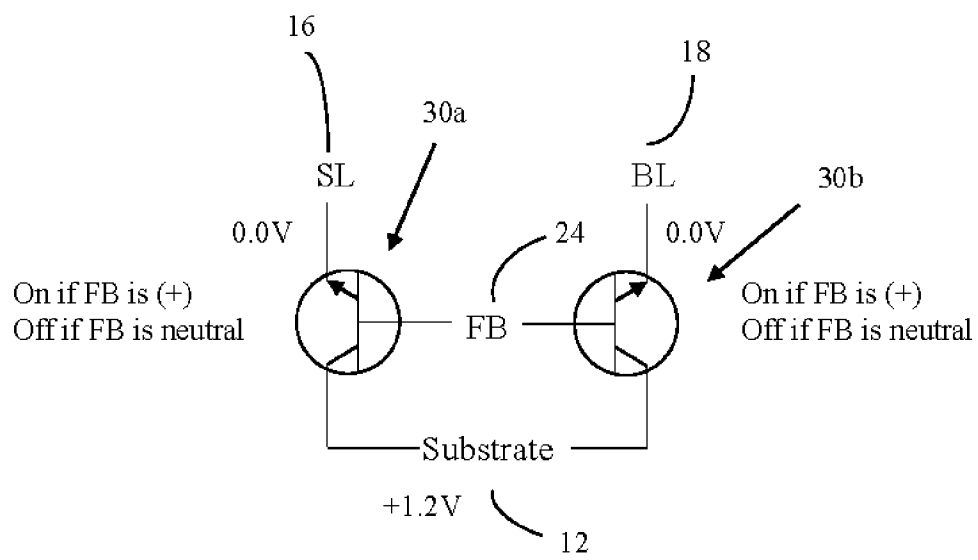


FIG. 15D

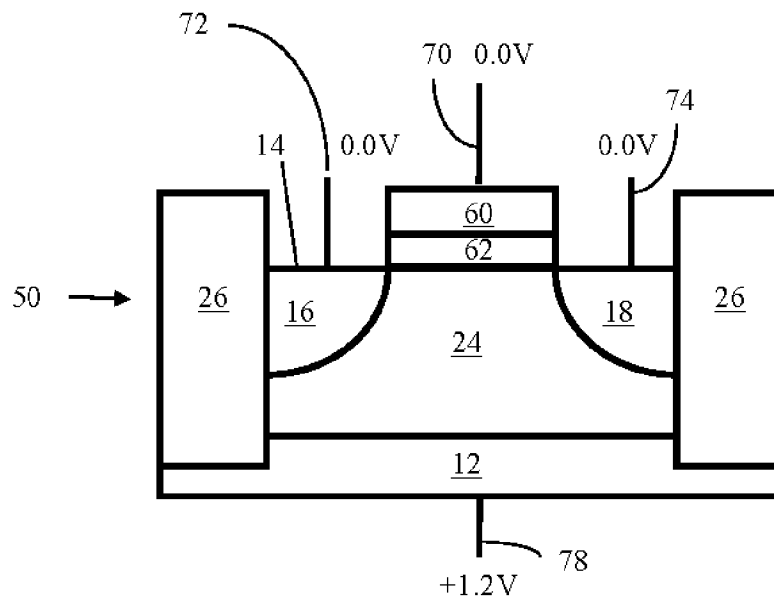


FIG. 15G

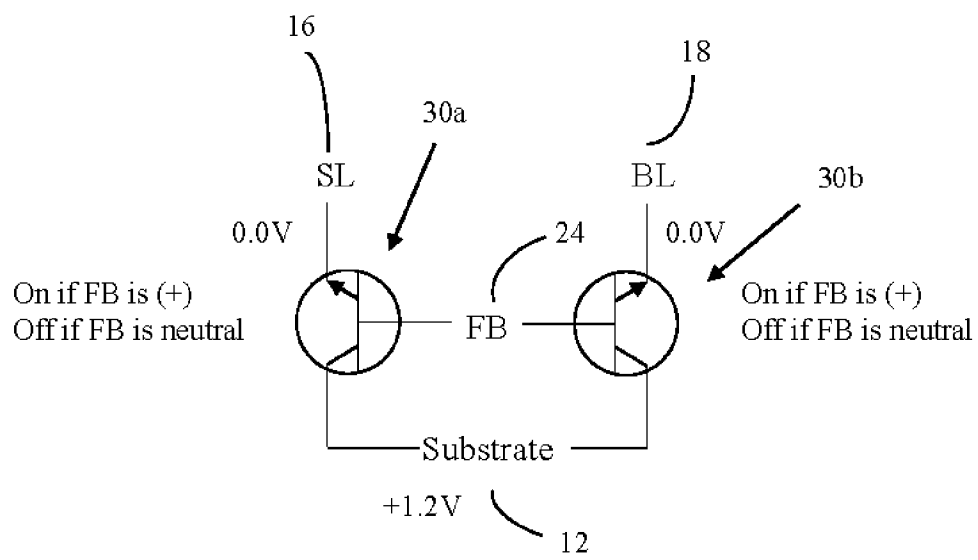


FIG. 15H

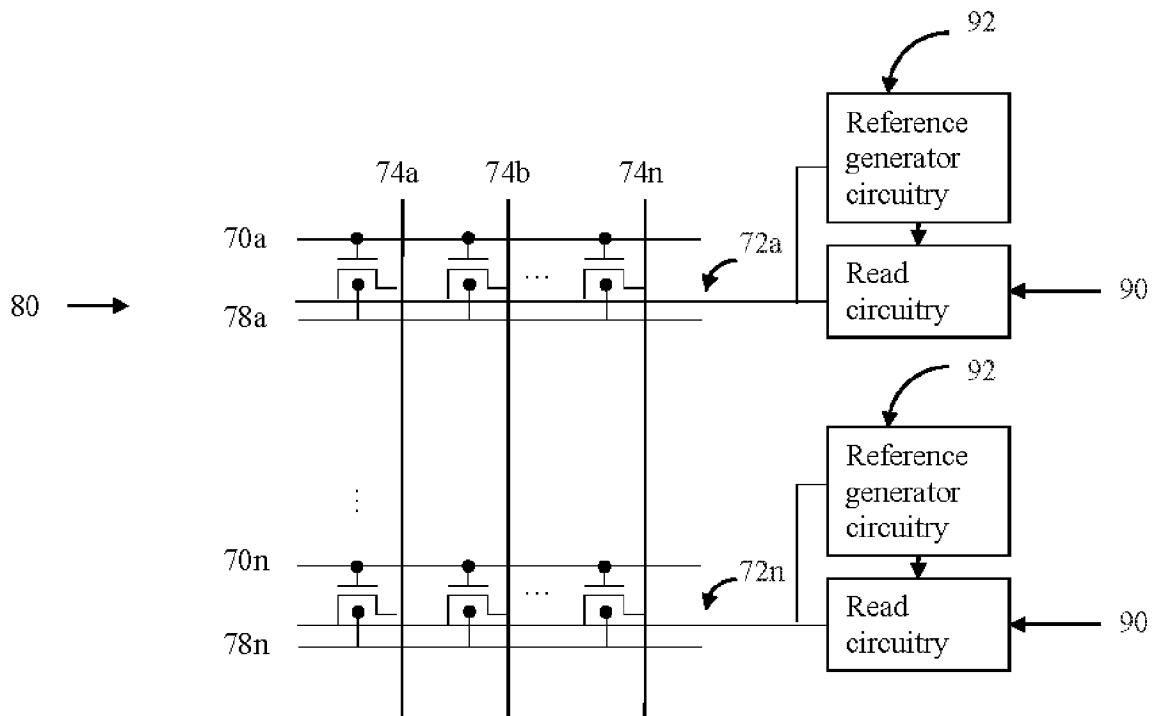


FIG. 16A

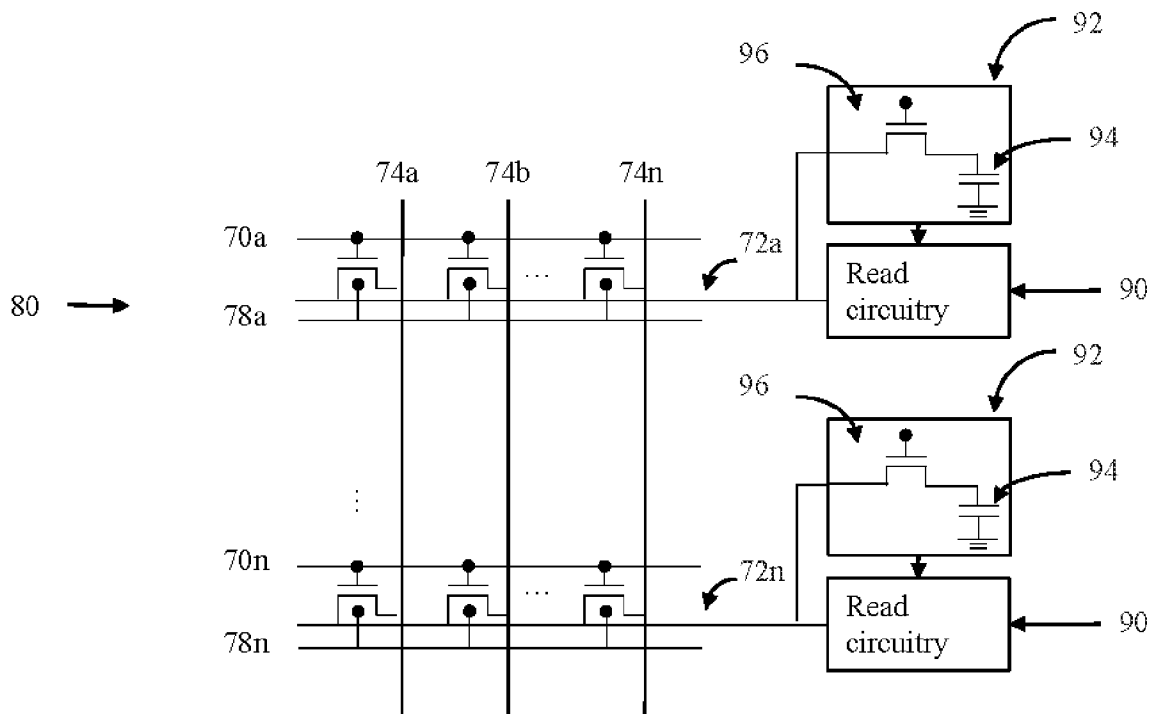


FIG. 16B

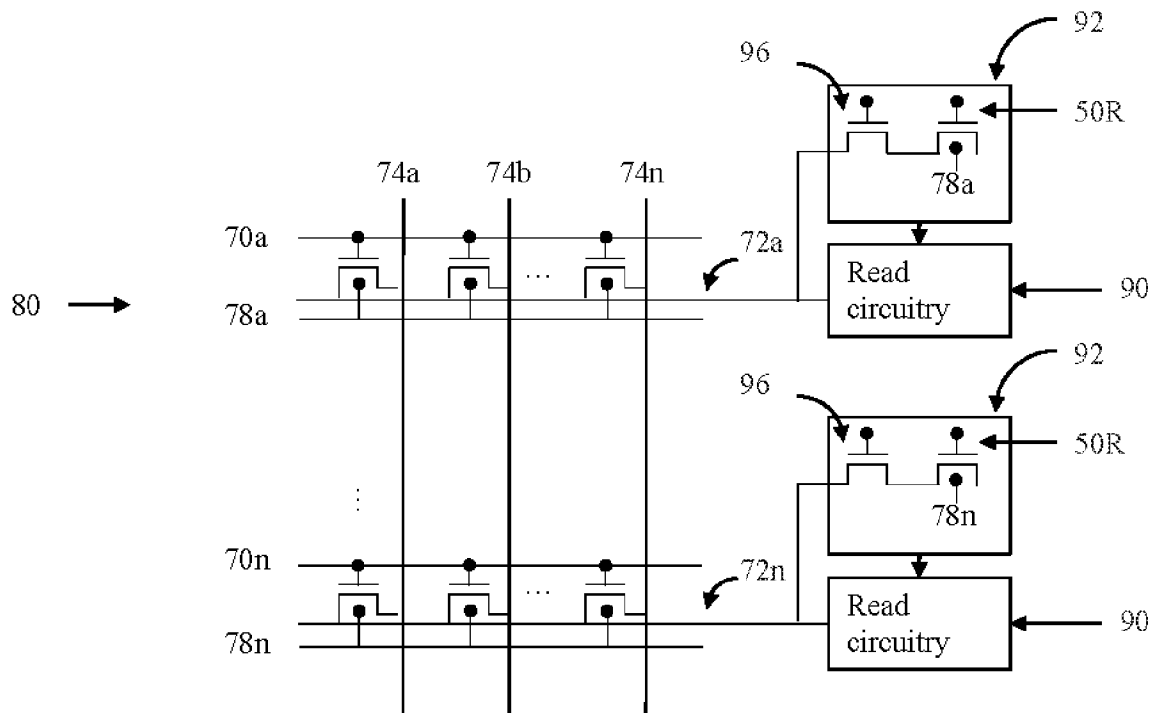


FIG. 16C

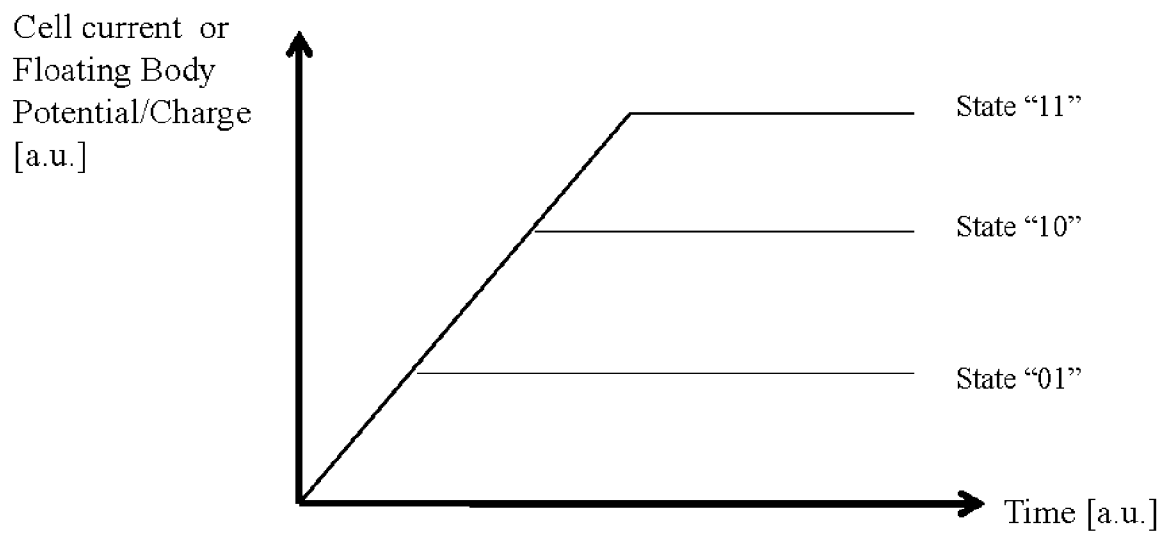


FIG. 17

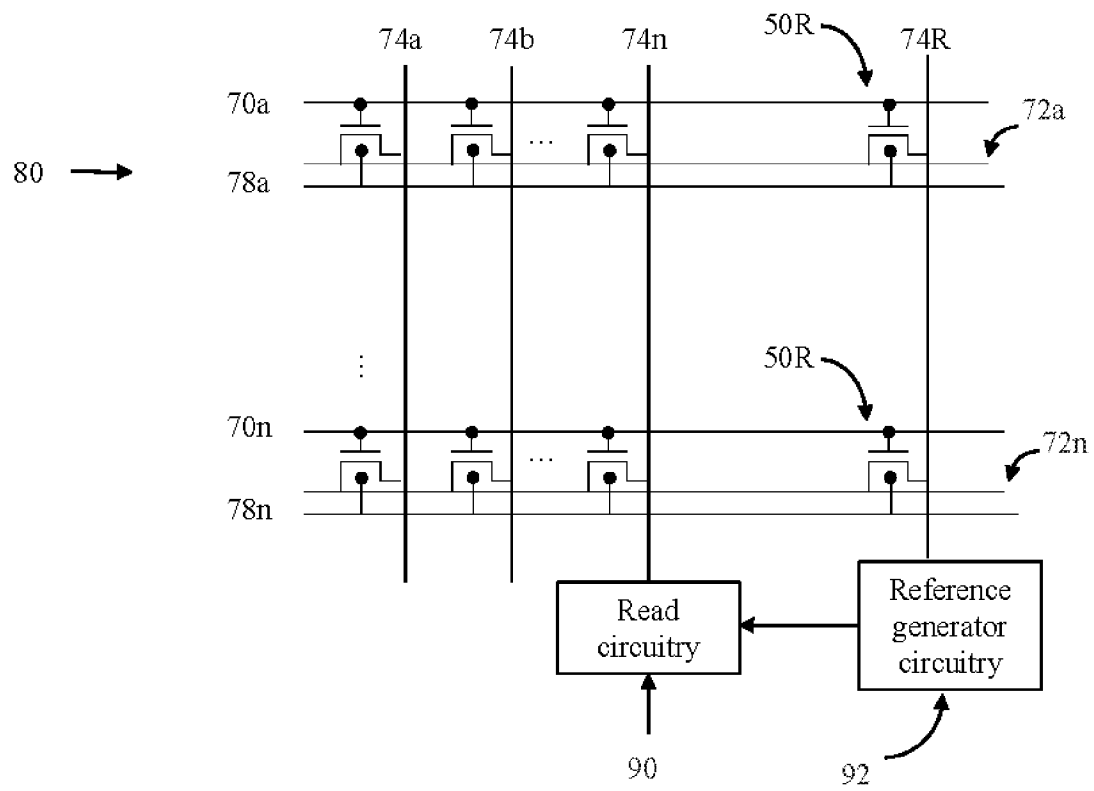


FIG. 18A

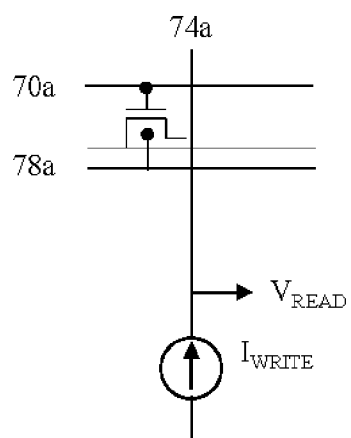


FIG. 18B

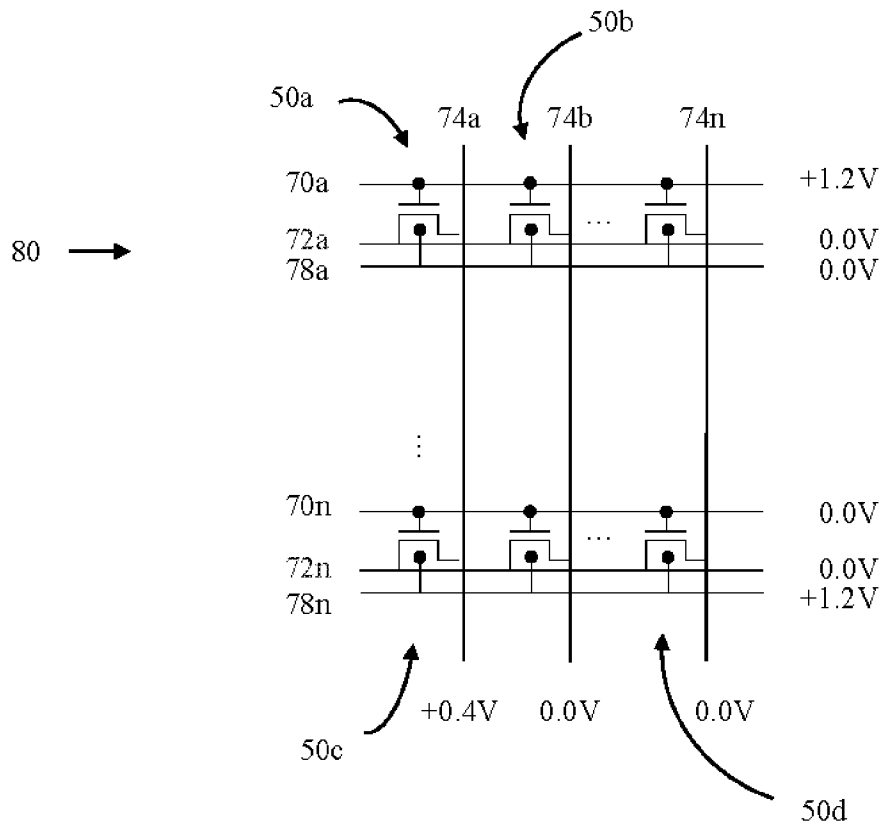


FIG. 19

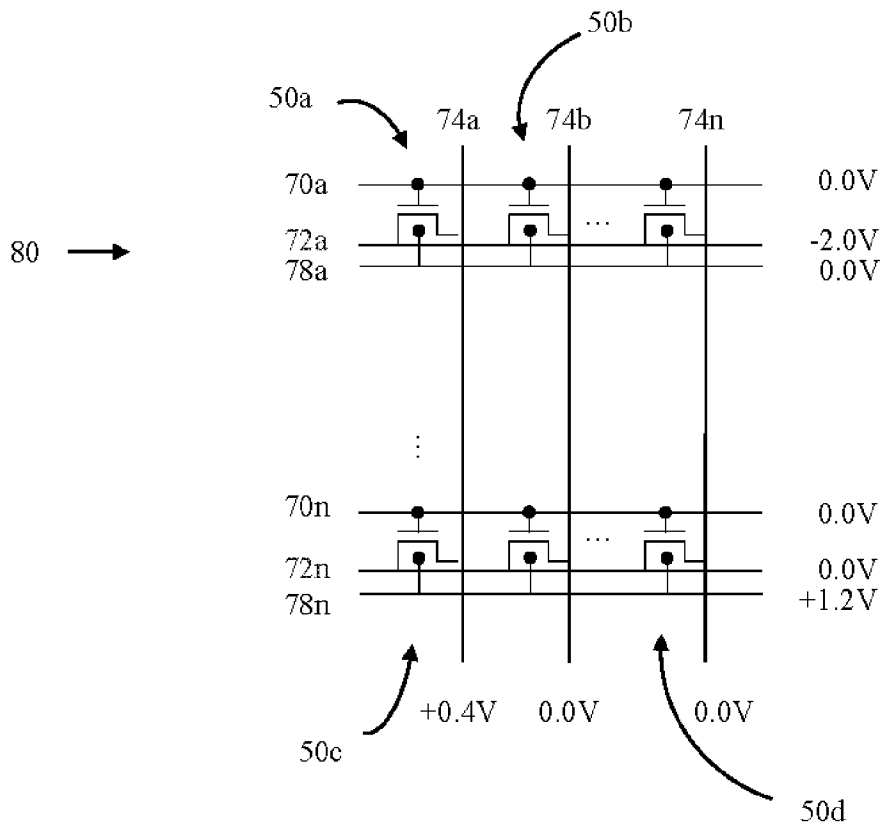


FIG. 20

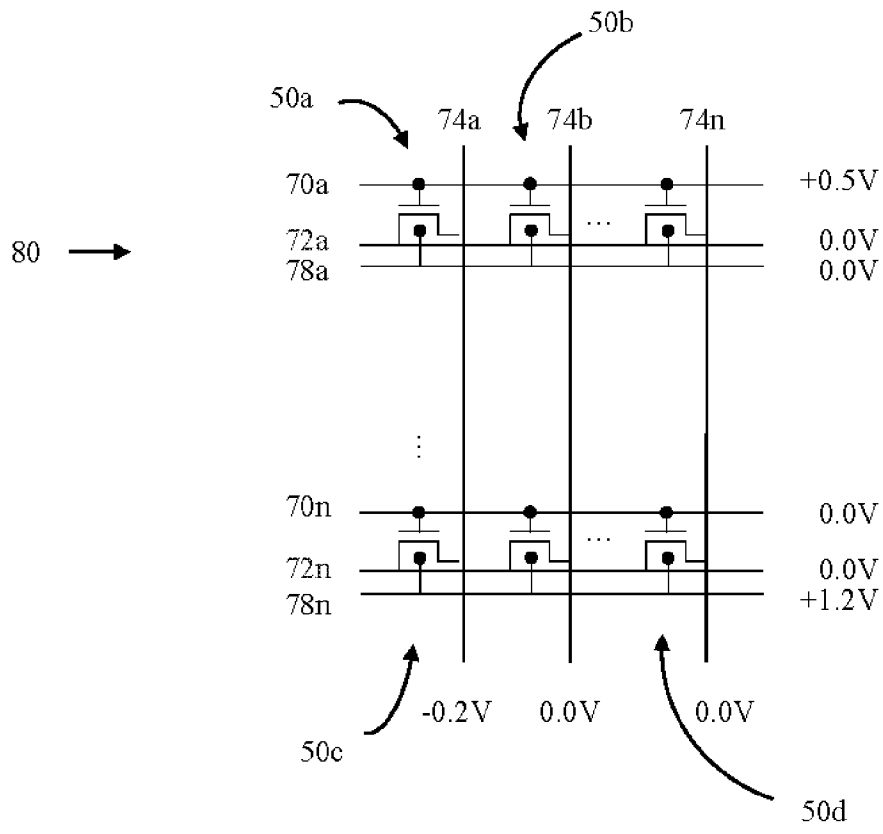


FIG. 21

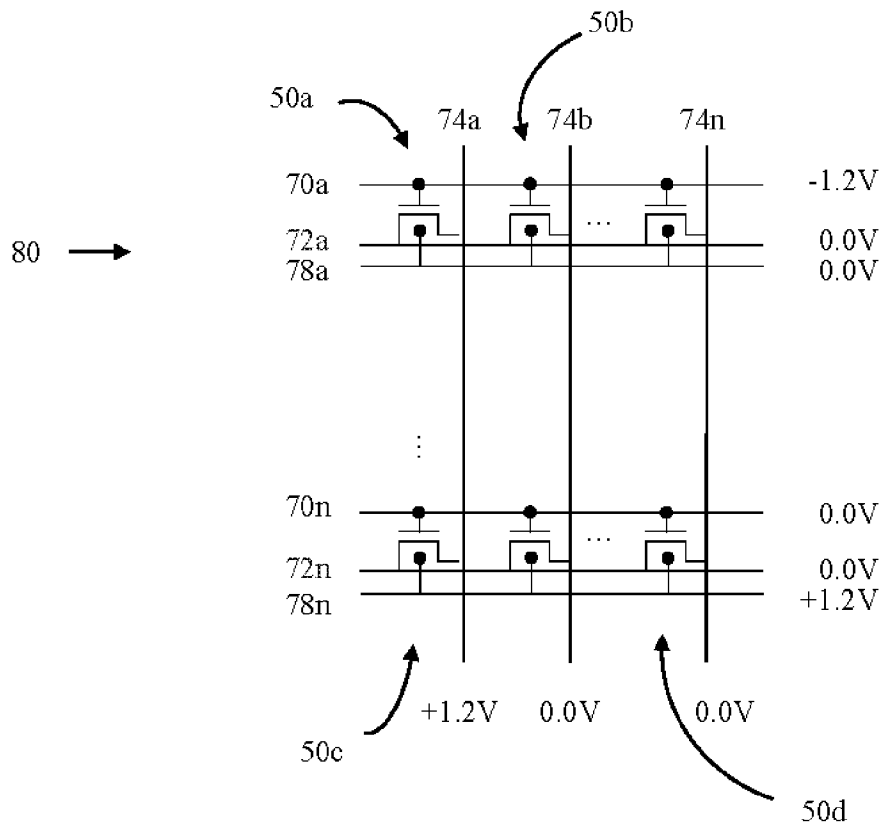


FIG. 22

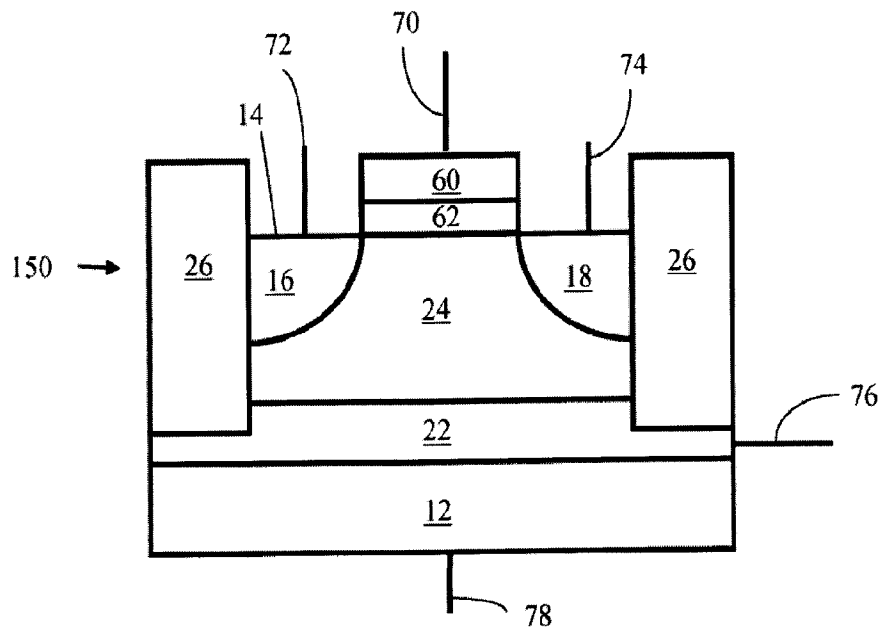


FIG. 23A

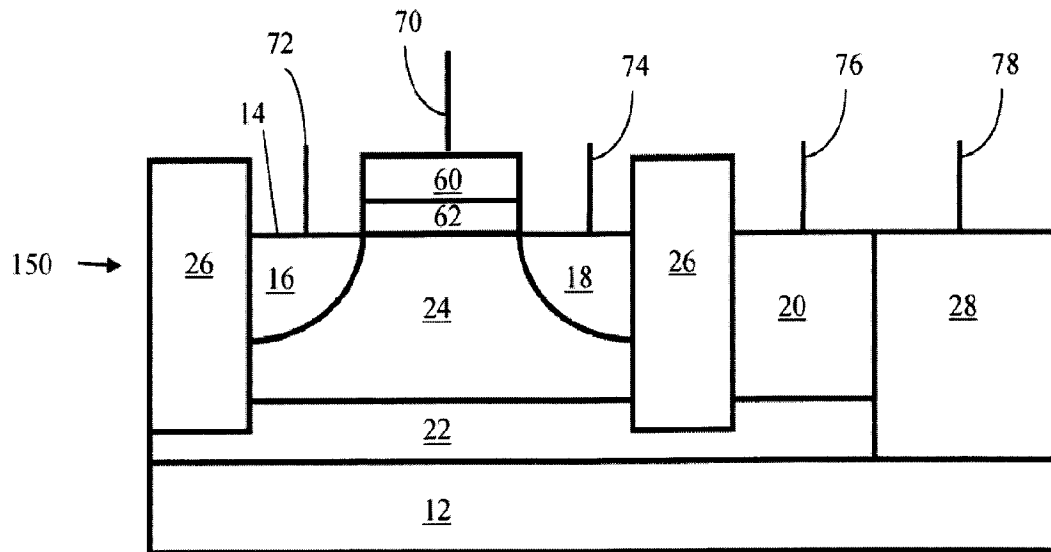


FIG. 23B

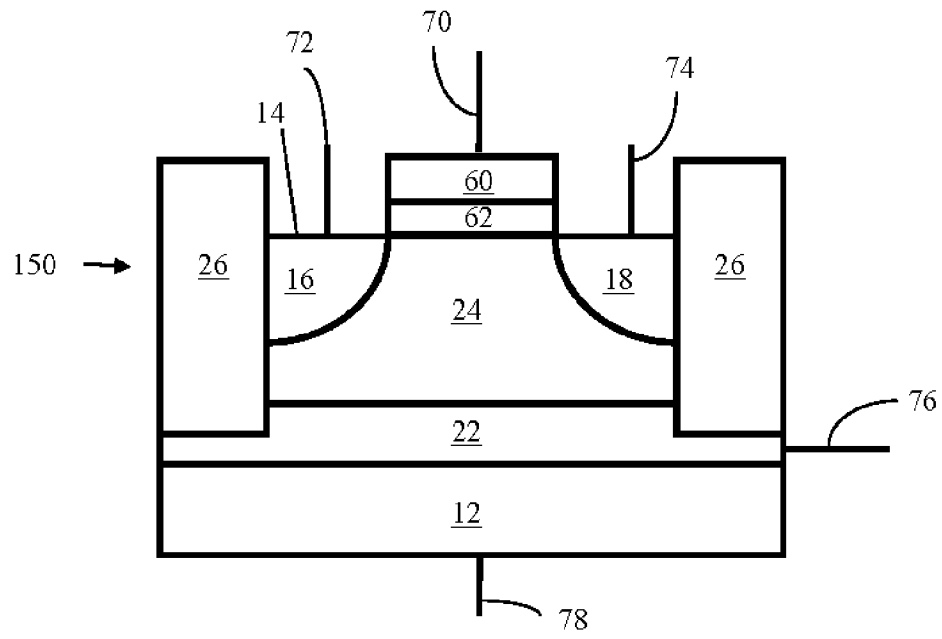


FIG. 23

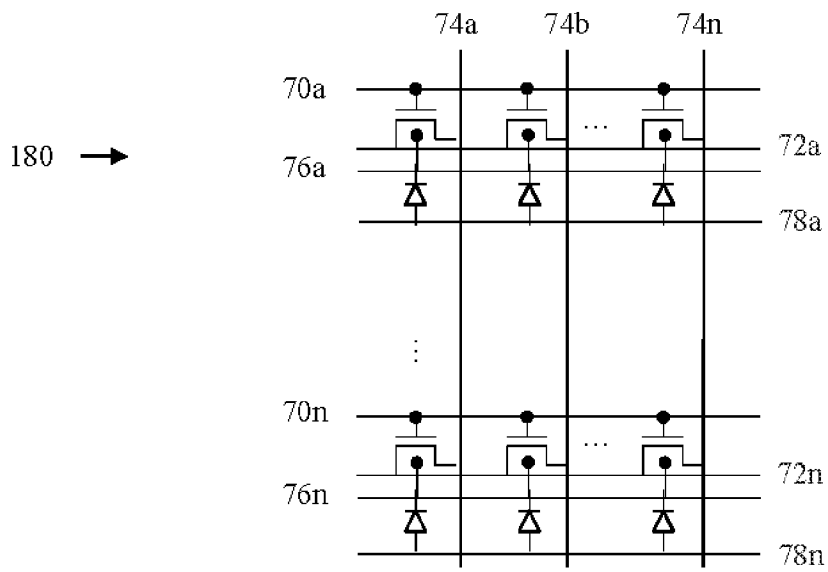


FIG. 24

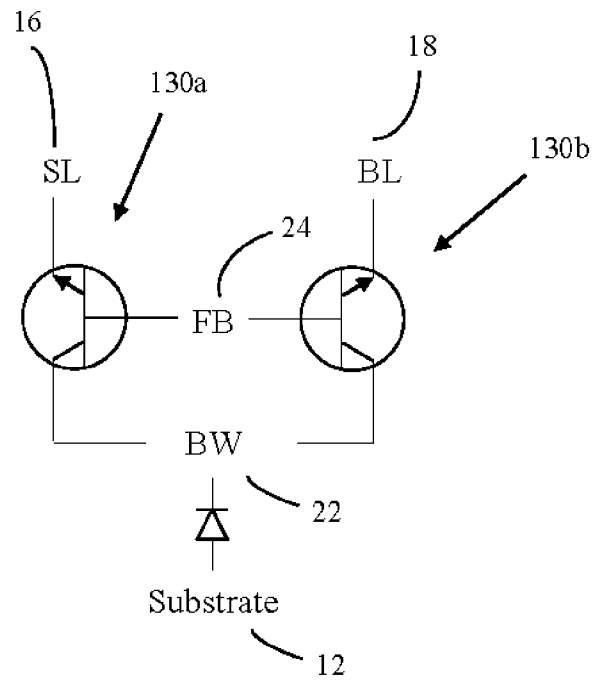


FIG. 25

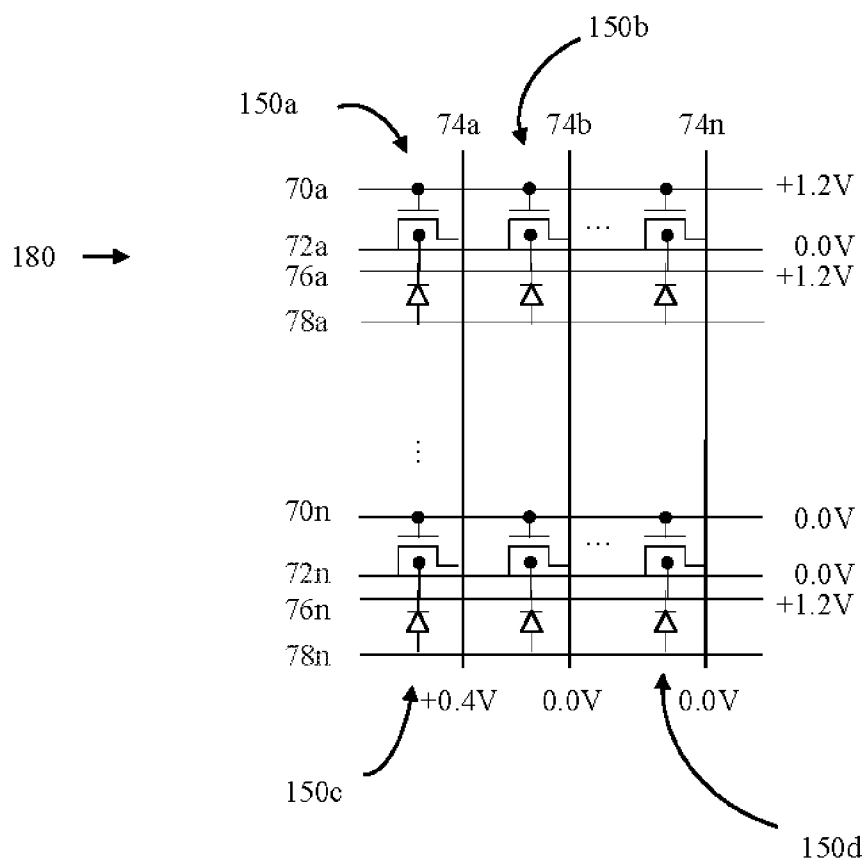


FIG. 26

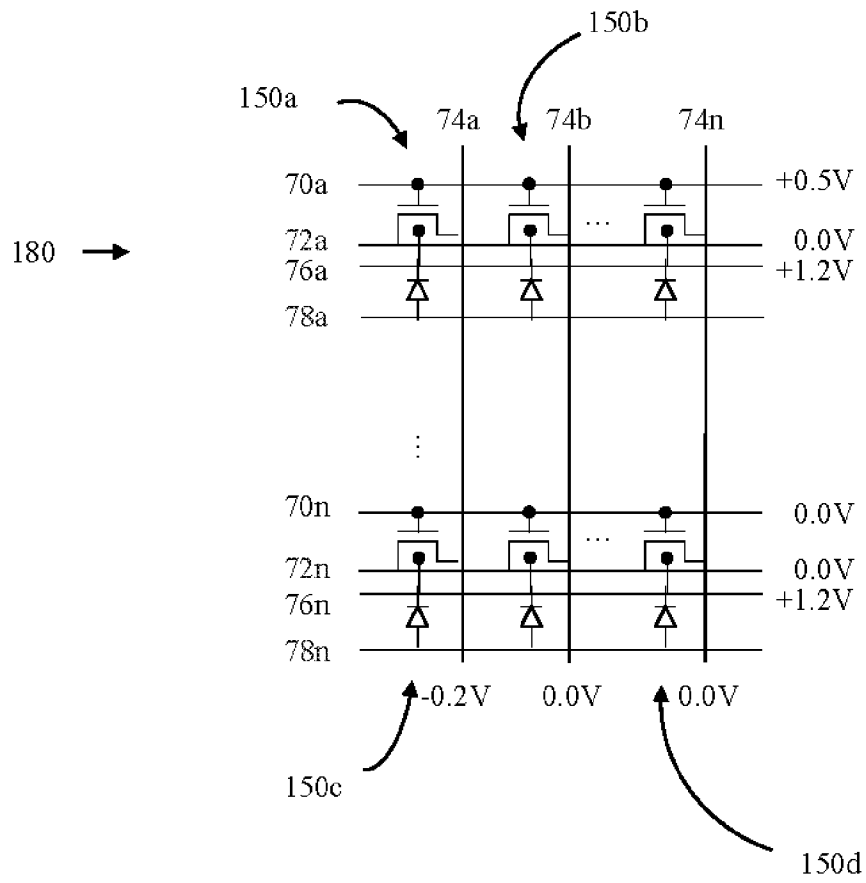


FIG. 27

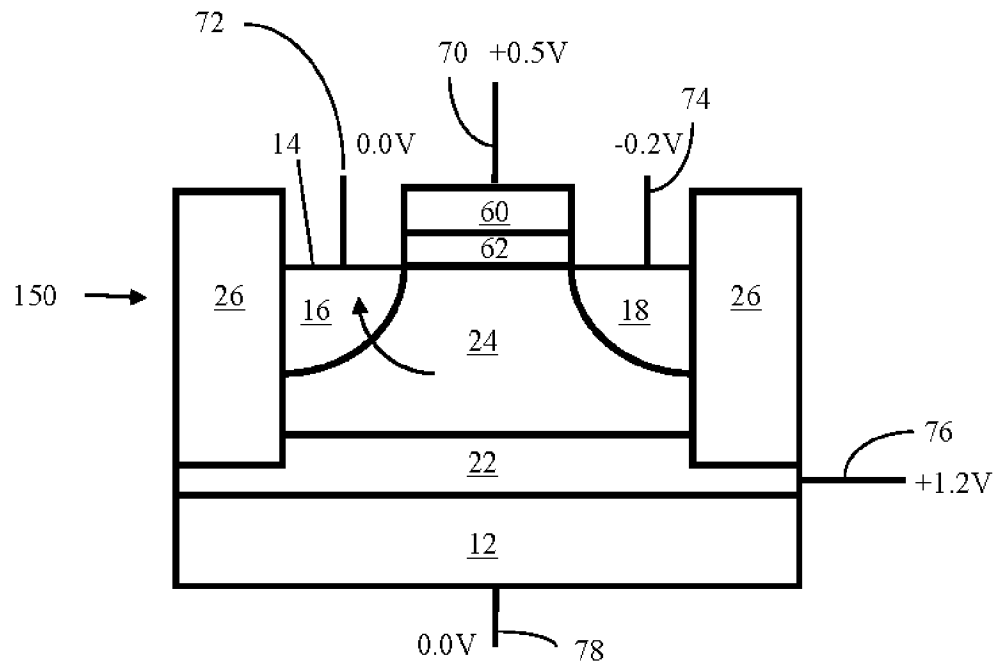


FIG. 28A

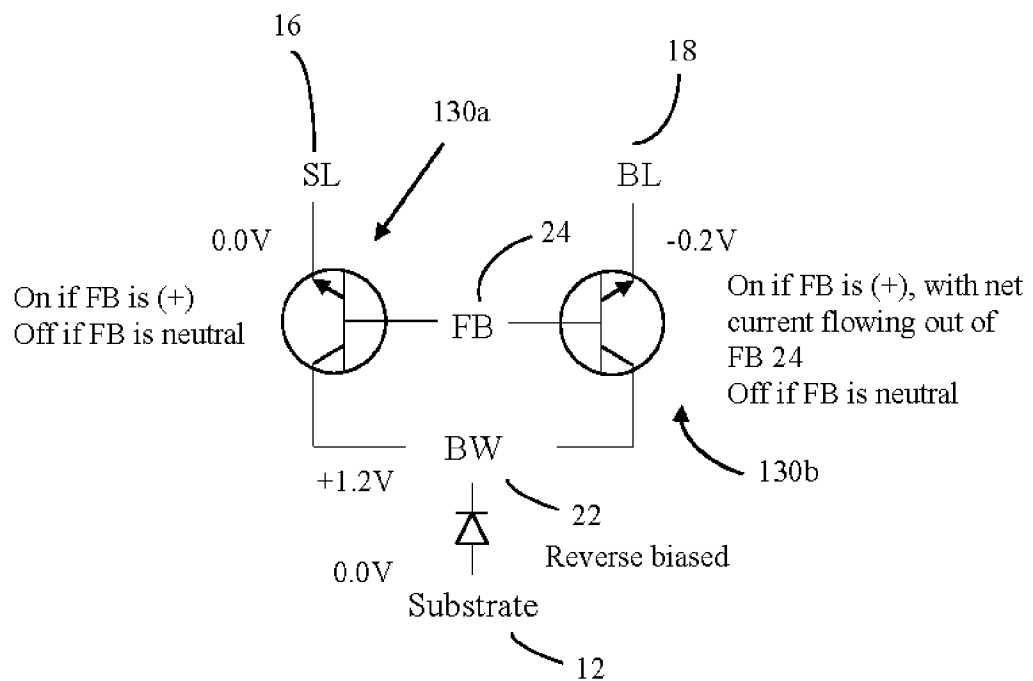


FIG. 28B

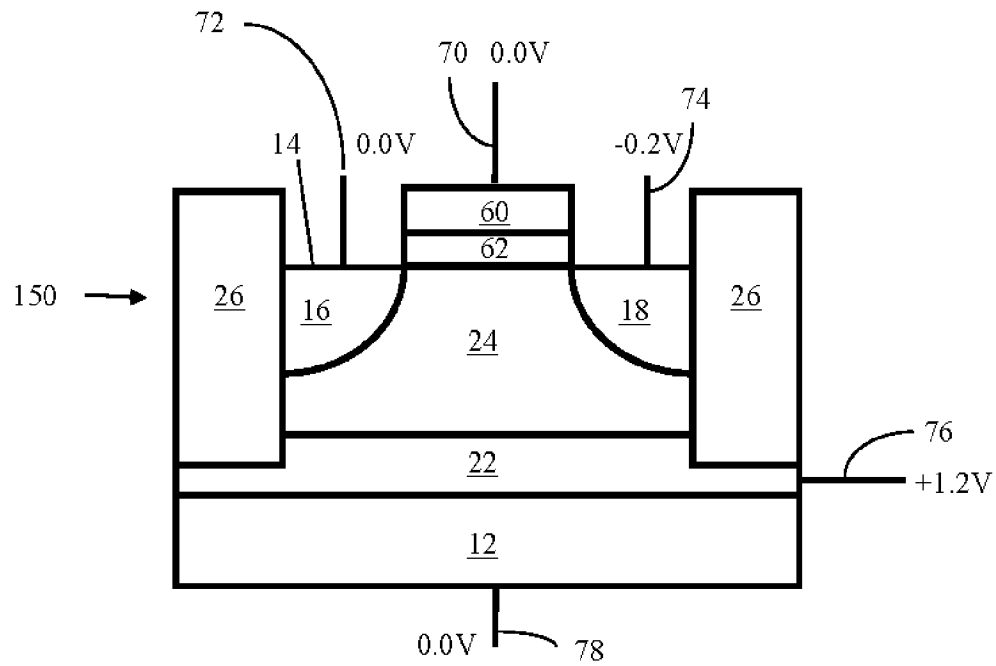


FIG. 28E

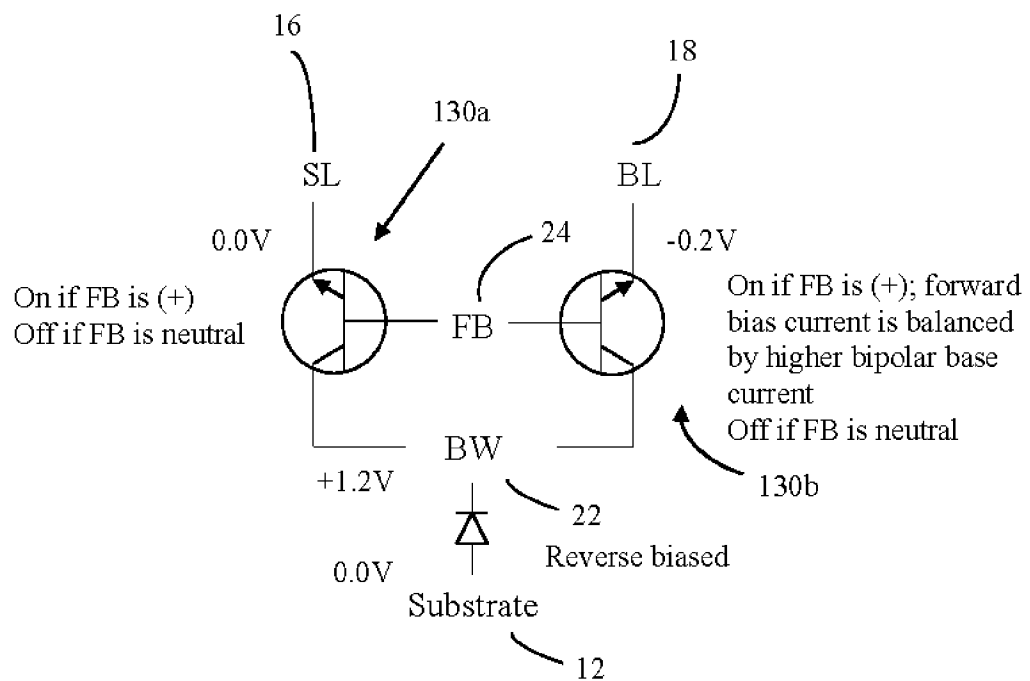


FIG. 28F

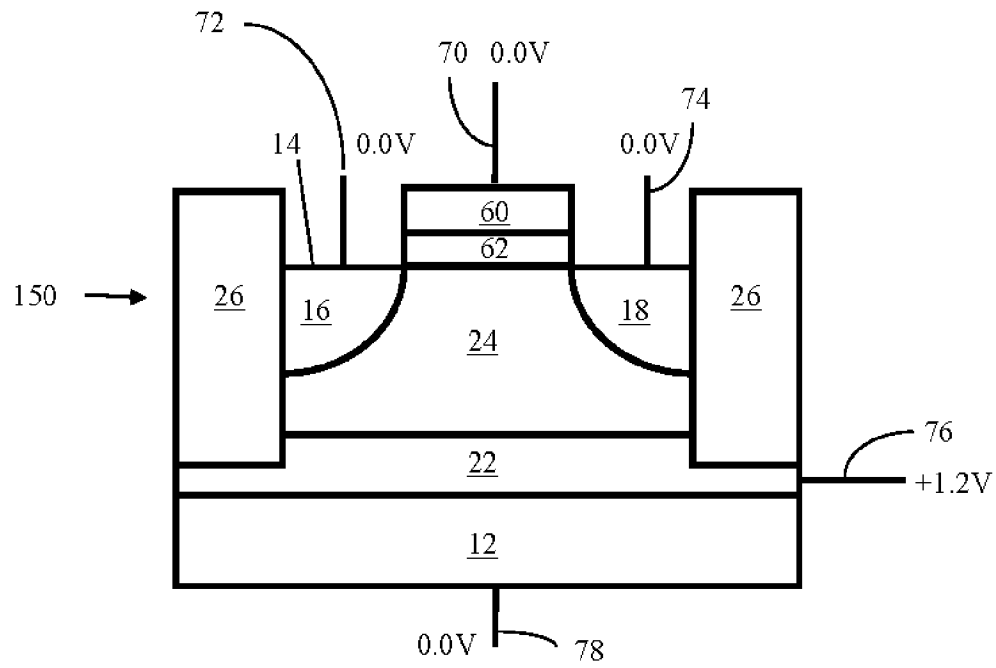


FIG. 28G

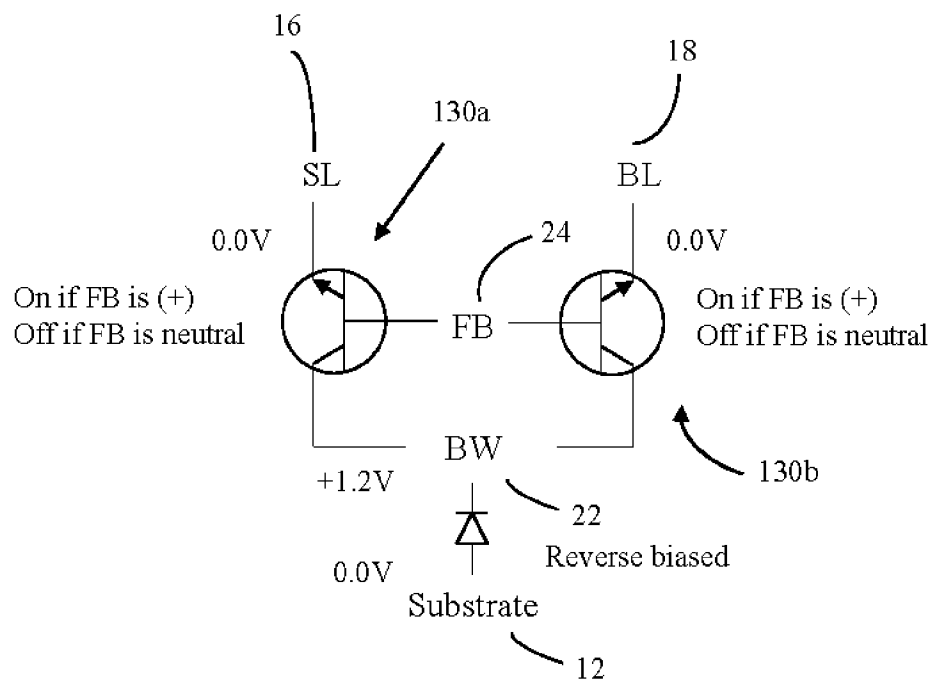


FIG. 28H

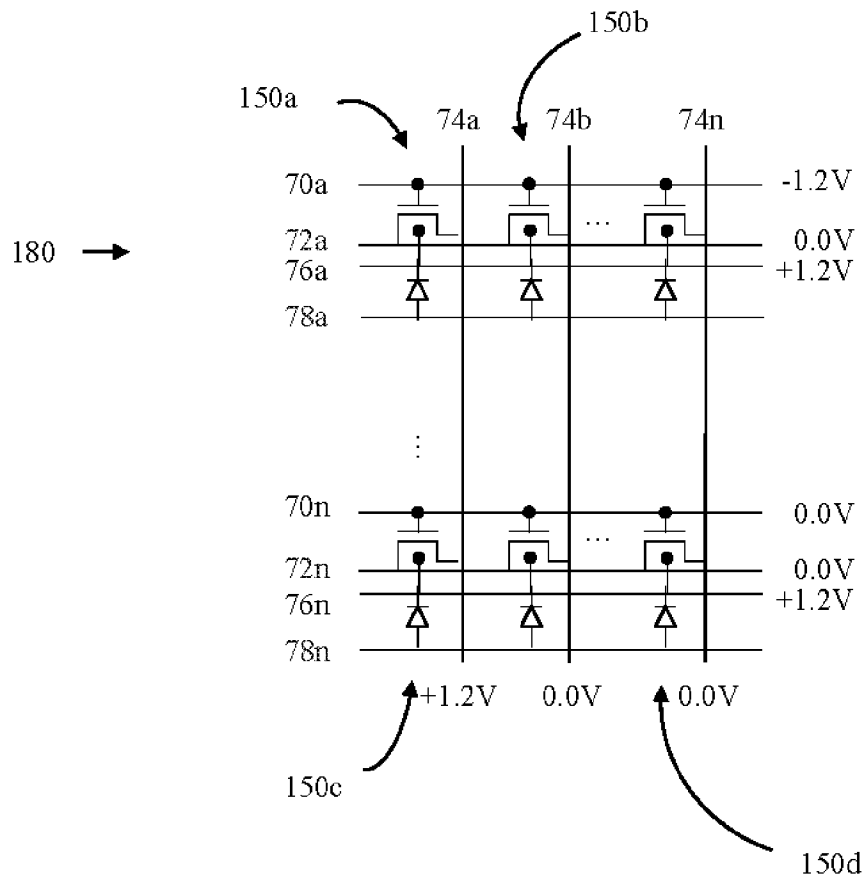


FIG. 29

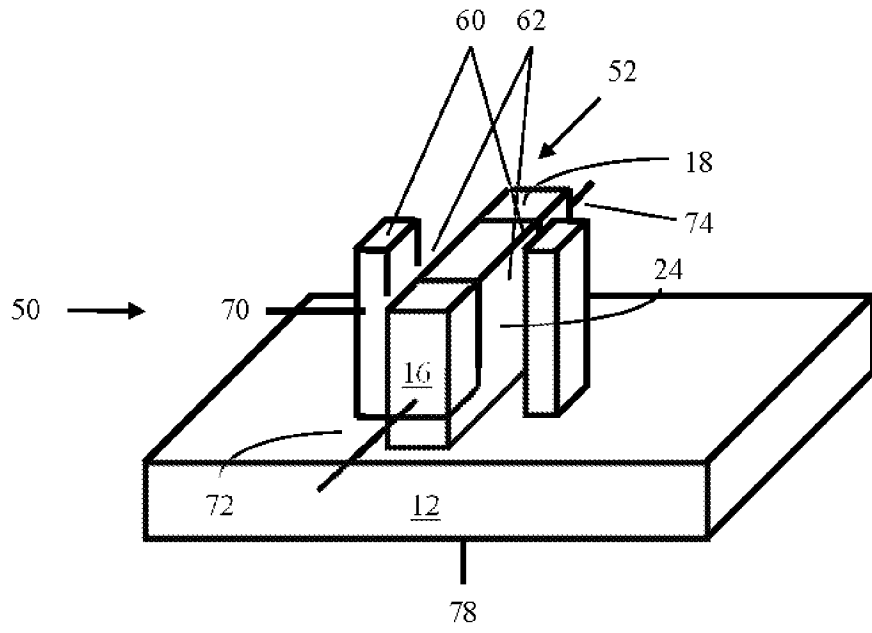


FIG. 30

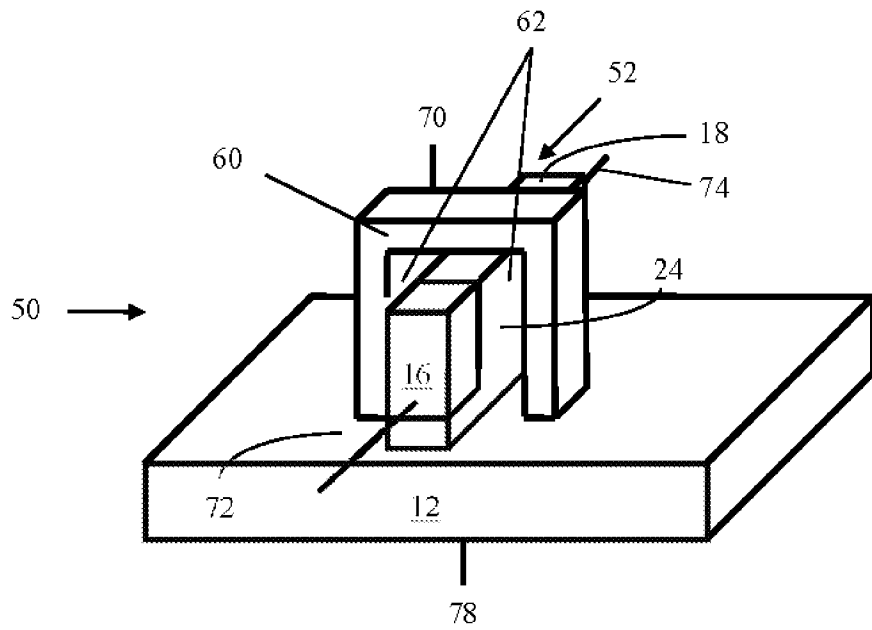


FIG. 31

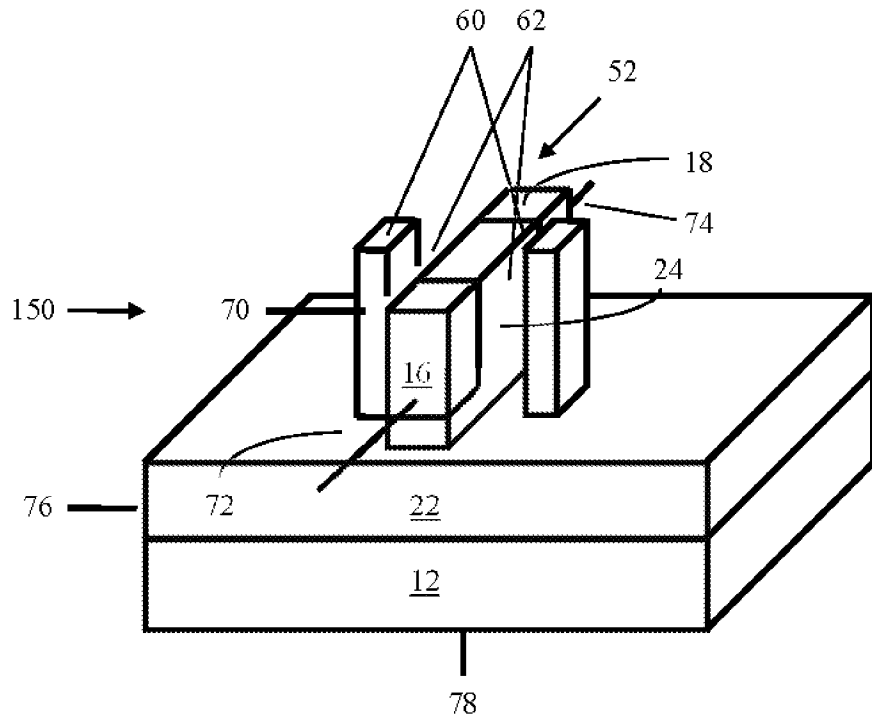


FIG. 32

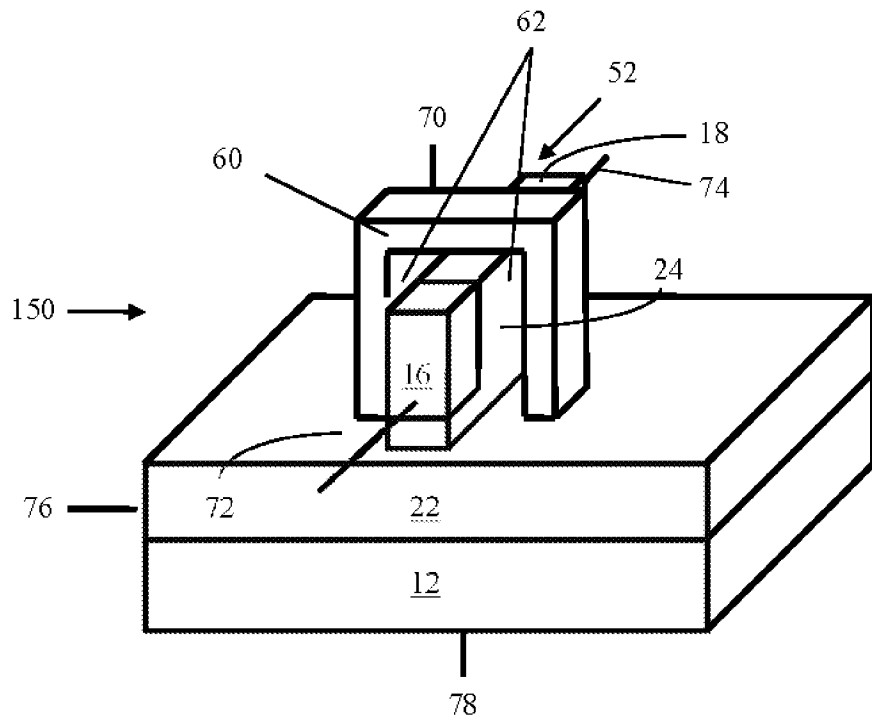


FIG. 33

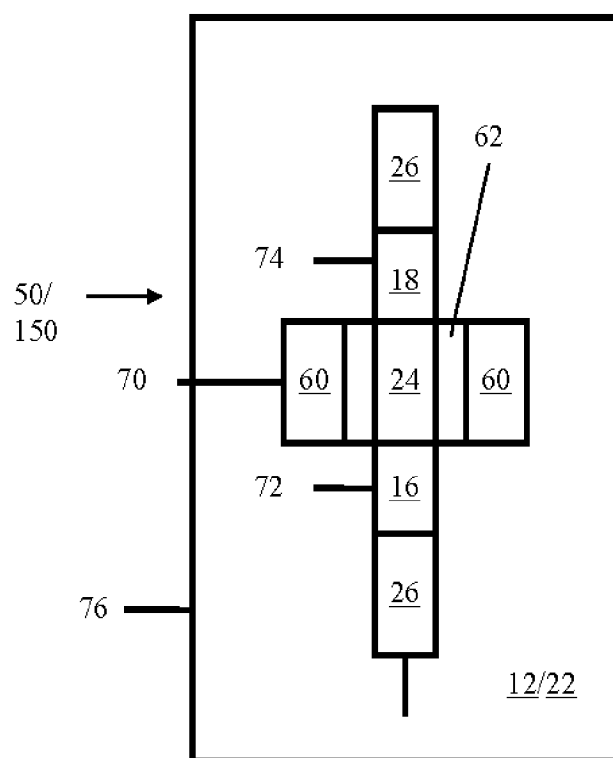


FIG. 34

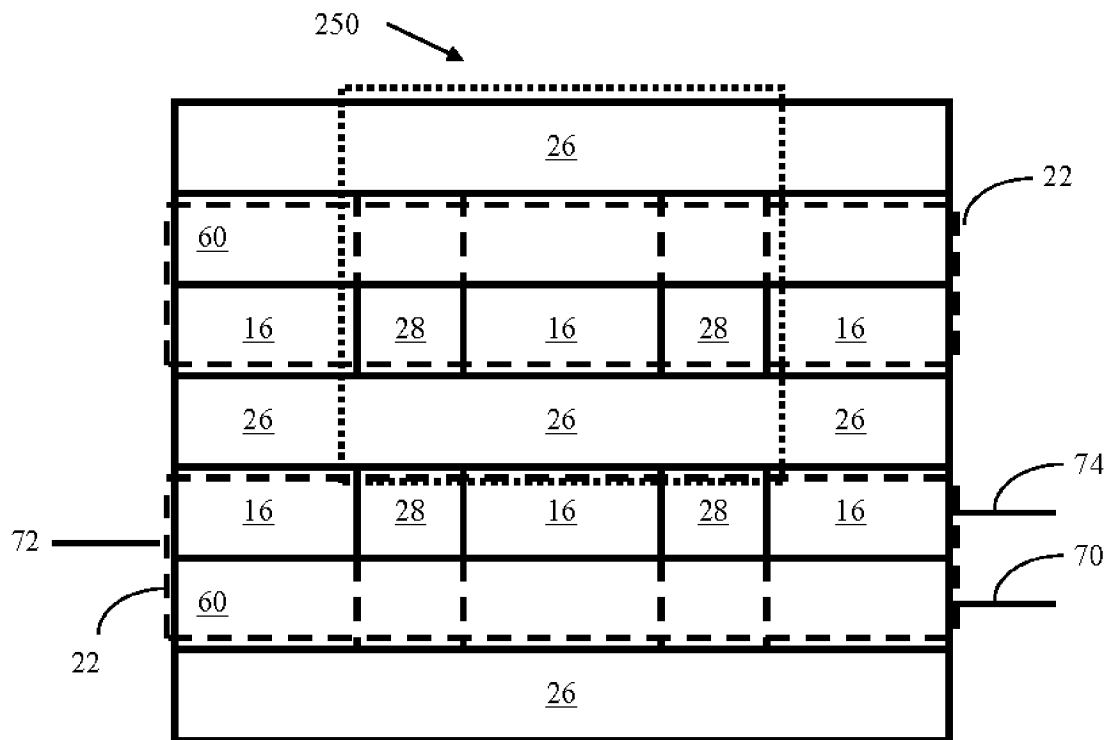


FIG. 35A

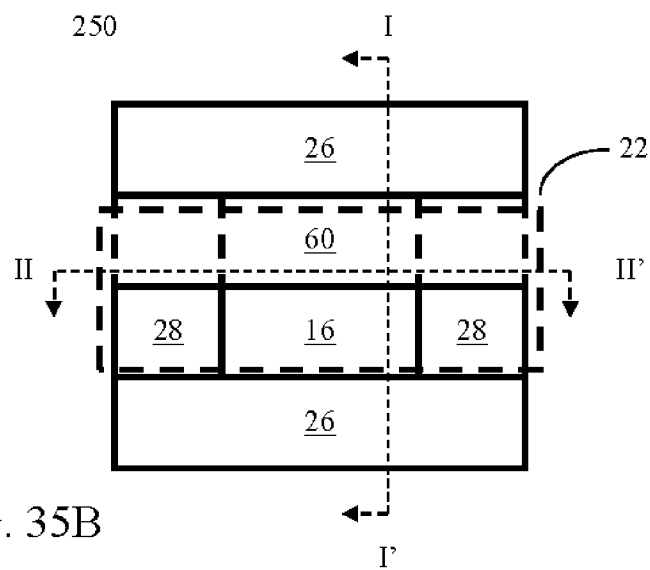


FIG. 35B

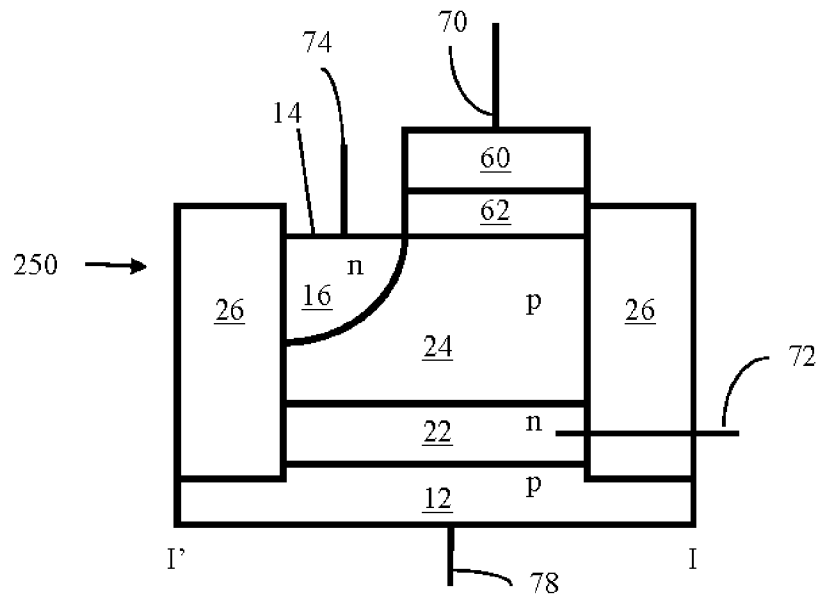


FIG. 35C

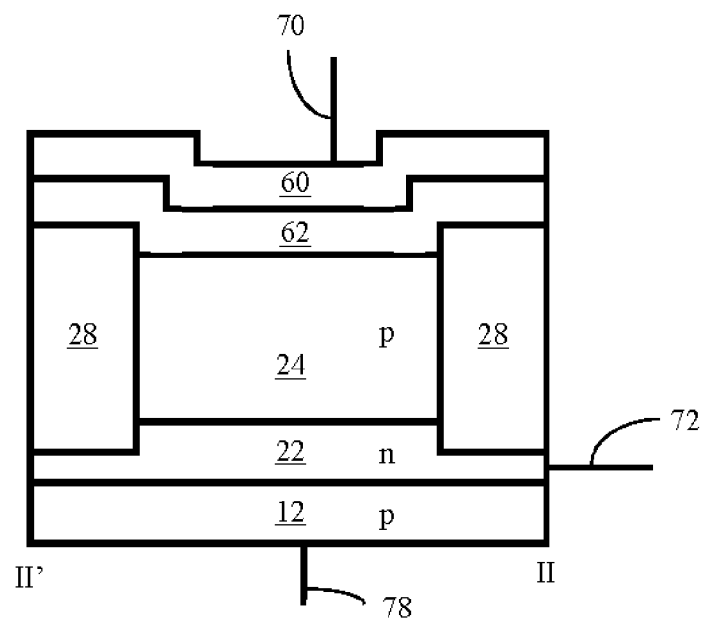


FIG. 35D

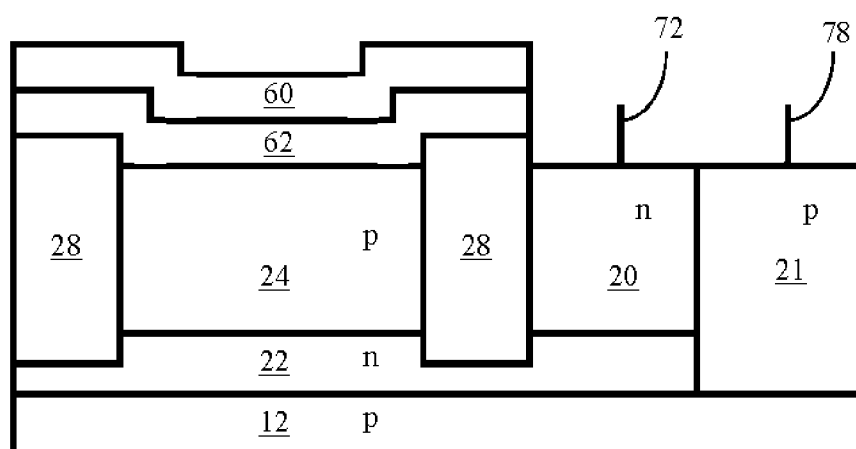


FIG. 35E

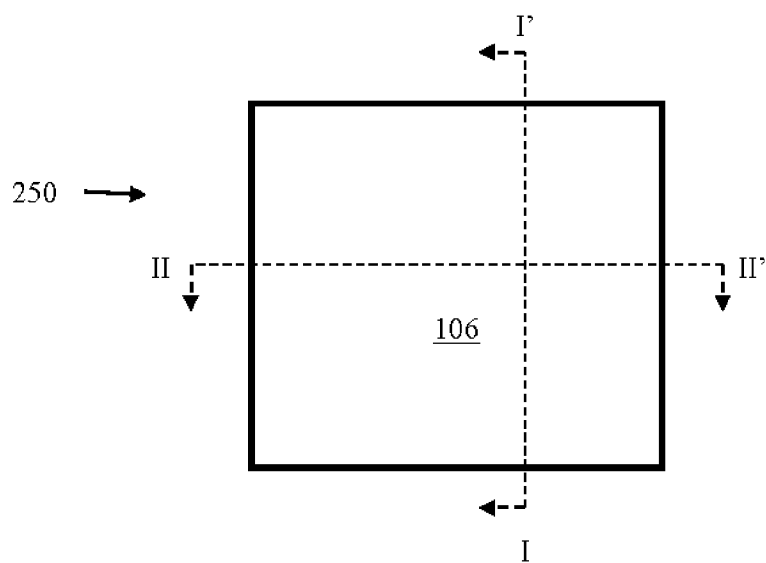


FIG. 36A

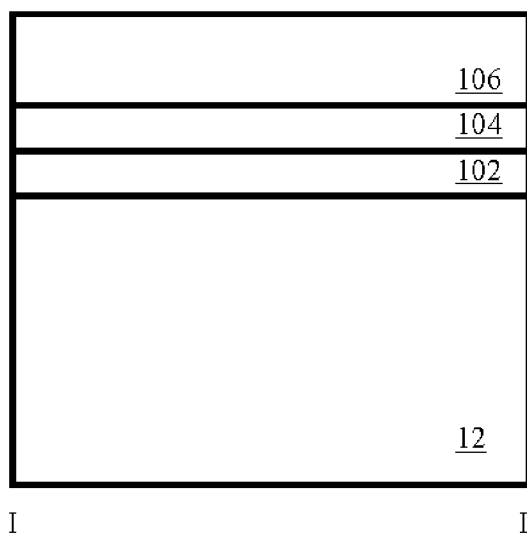


FIG. 36B

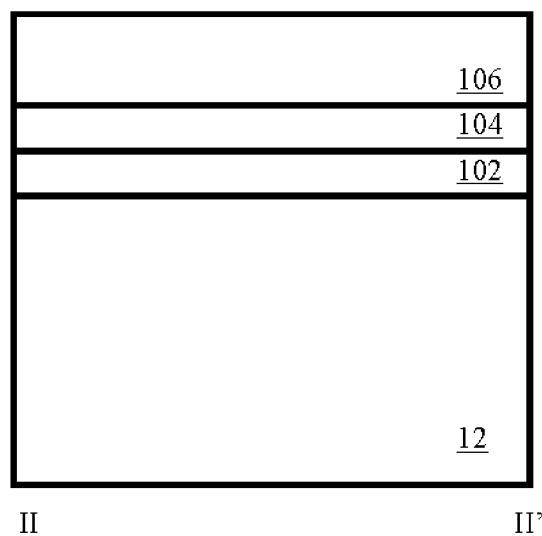


FIG. 36C

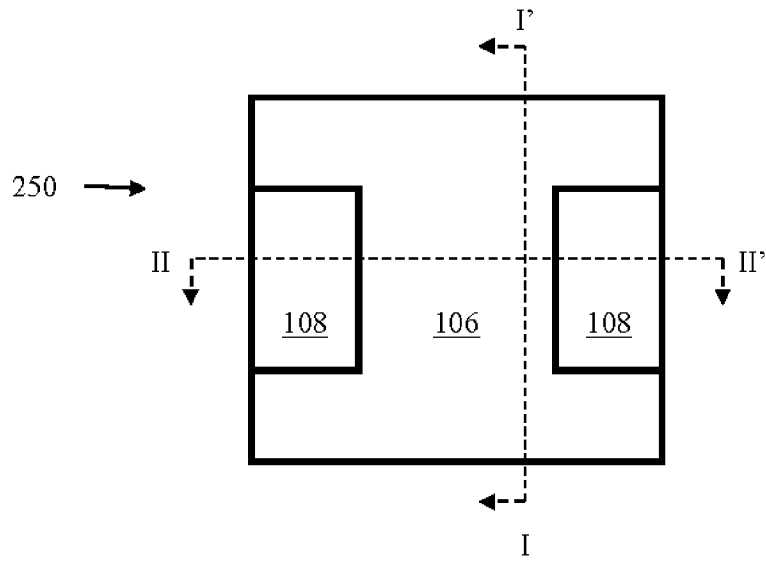


FIG. 36D

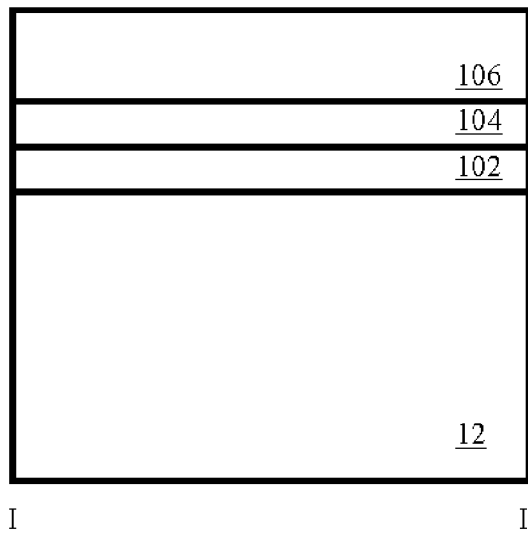


FIG. 36E

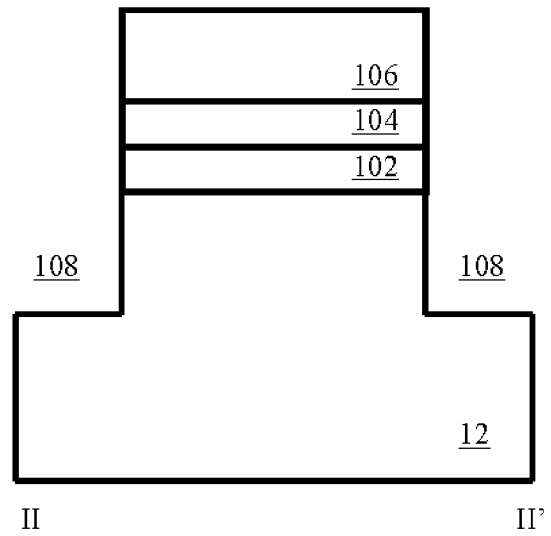


FIG. 36F

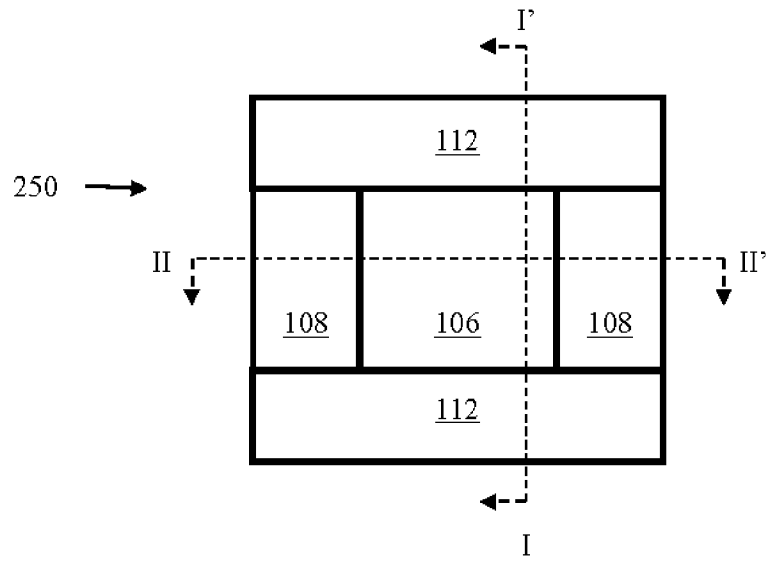


FIG. 36G

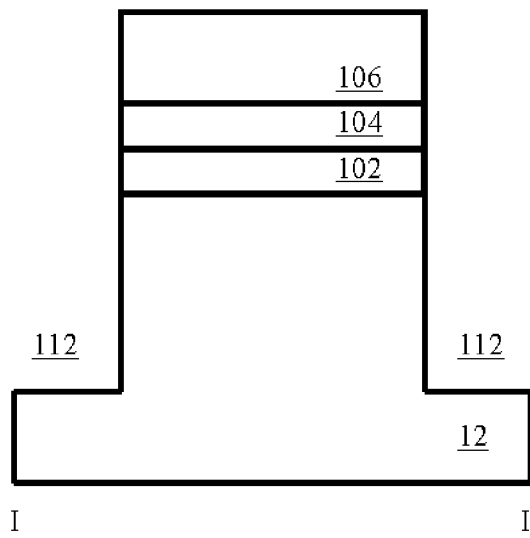


FIG. 36H

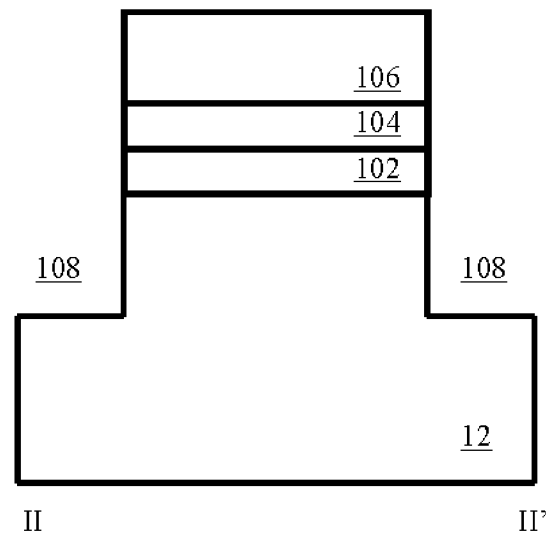


FIG. 36I

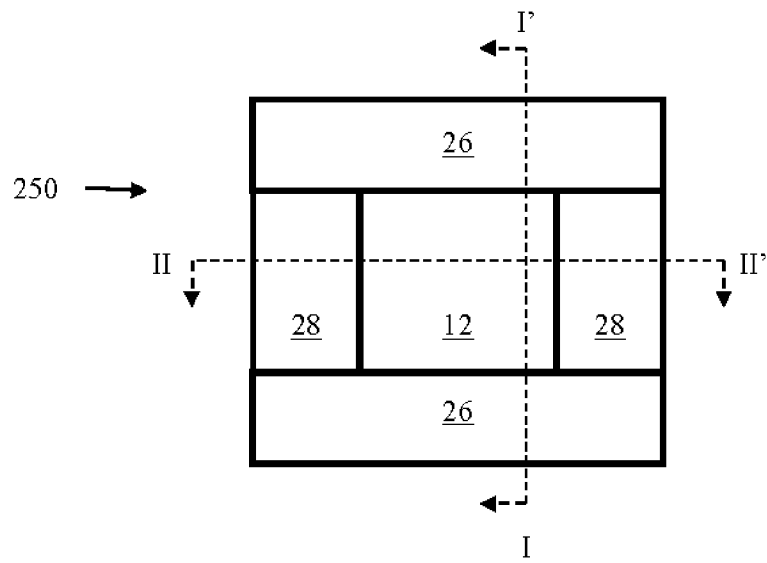


FIG. 36J

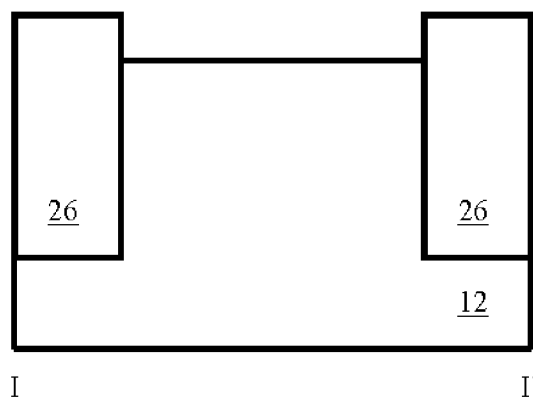


FIG. 36K

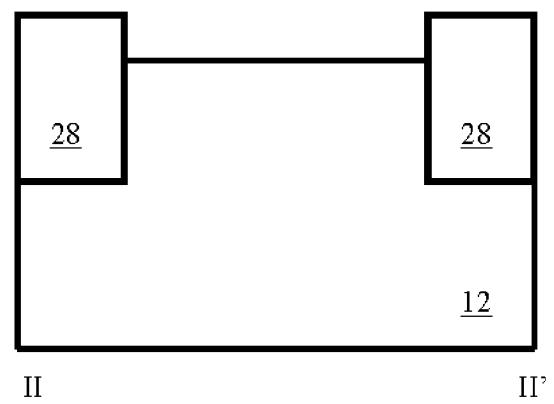


FIG. 36L

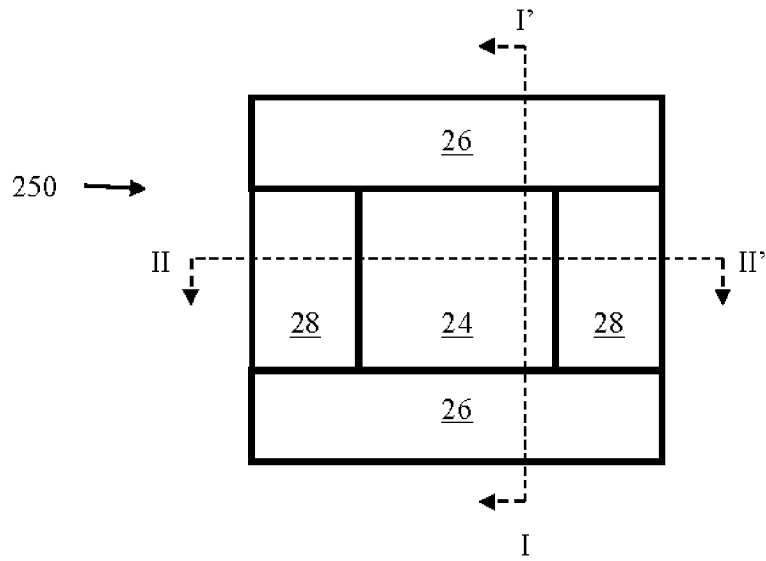


FIG. 36M

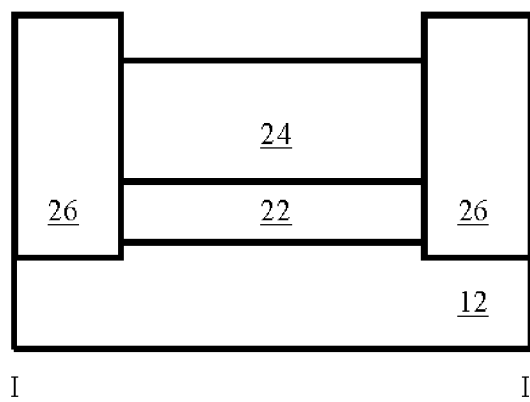


FIG. 36N

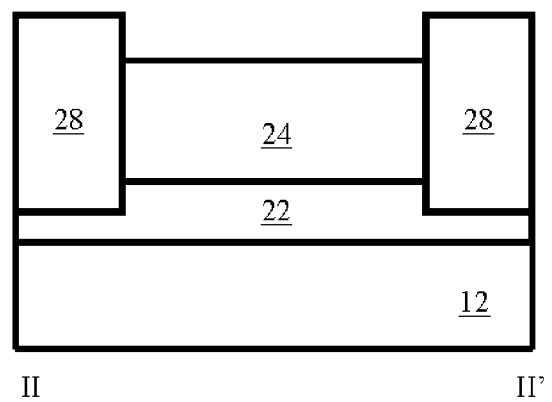


FIG. 36O

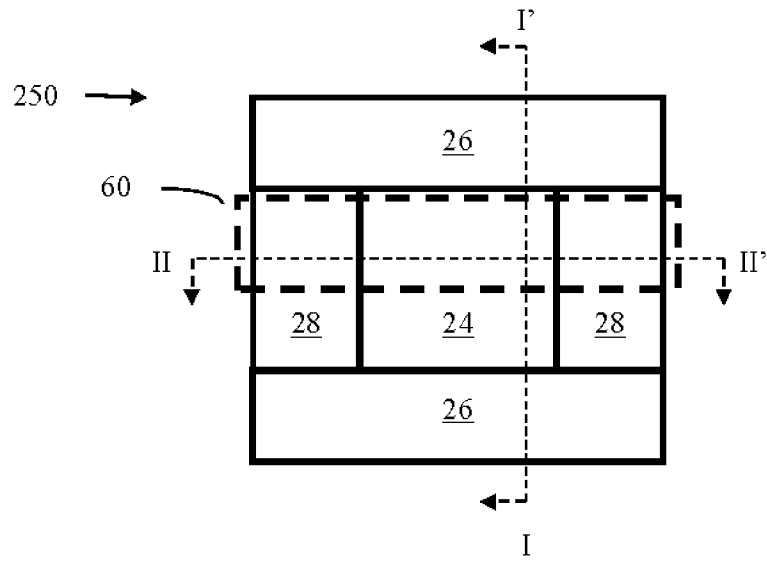


FIG. 36P

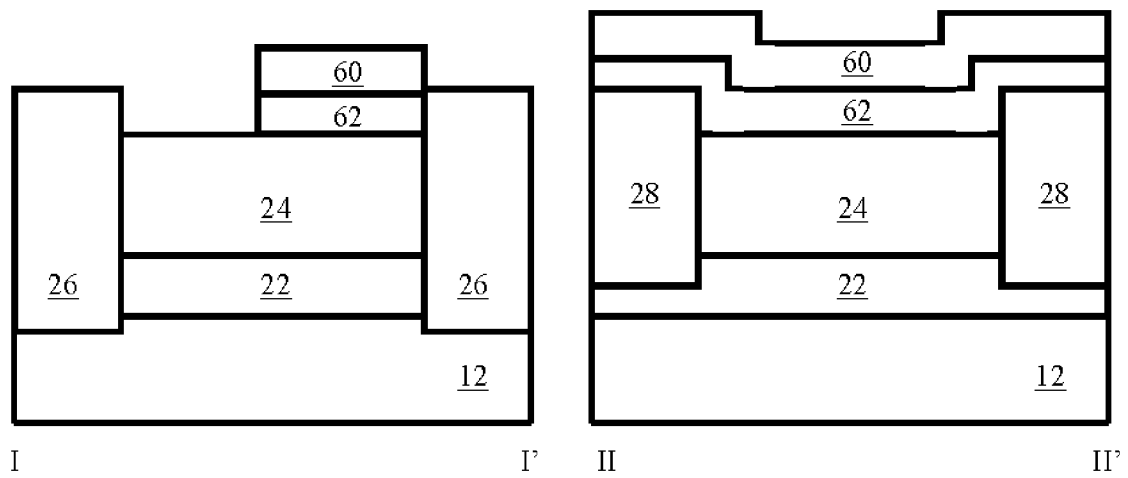


FIG. 36Q

FIG. 36R

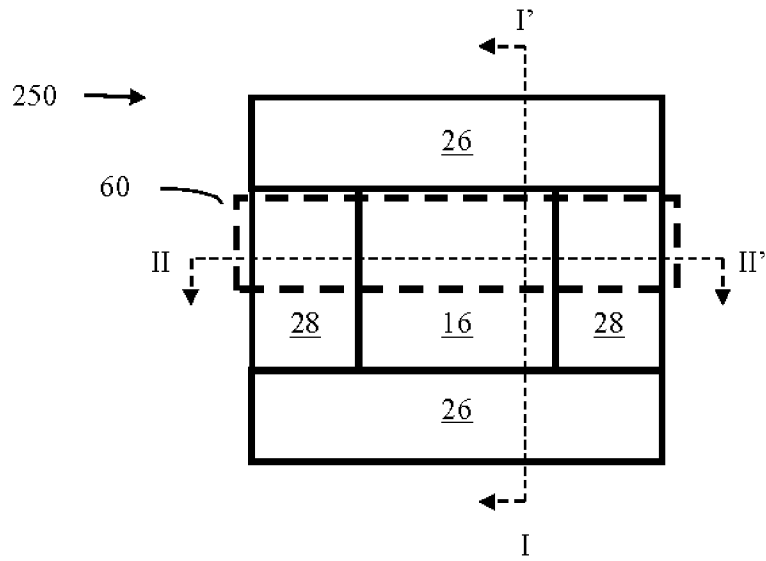


FIG. 36S

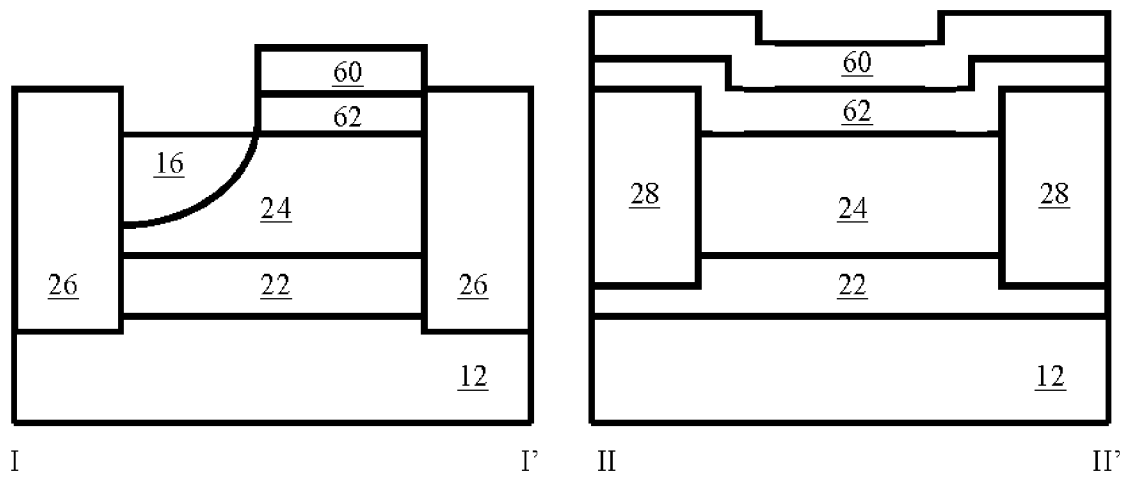


FIG. 36T

FIG. 36U

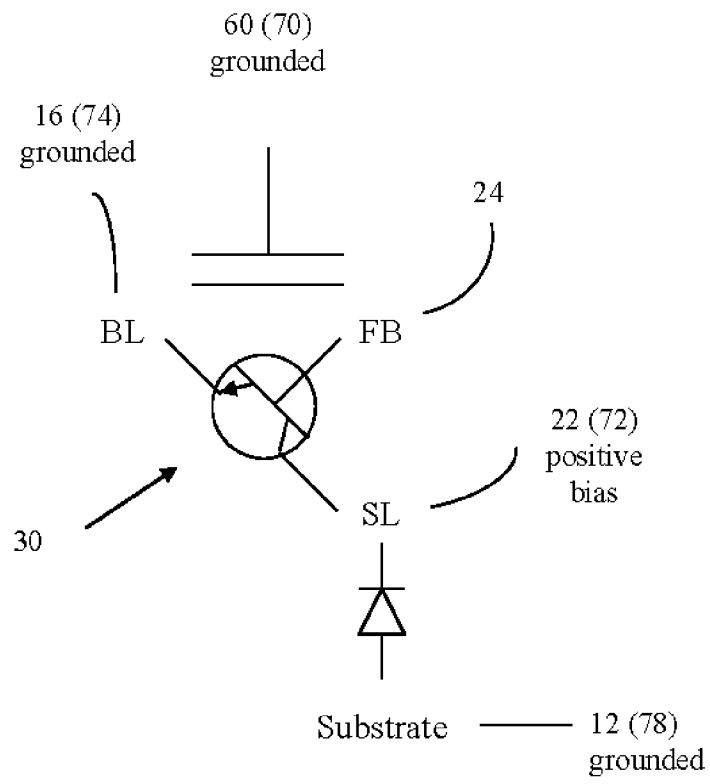


FIG. 37A

Floating Body 24 is positively charged and $V(\text{BL } 16) = 0.0\text{V}$

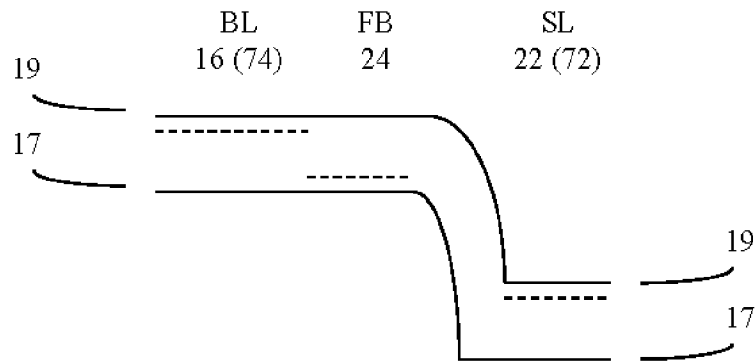


FIG. 37B

FB is neutrally charged; and $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

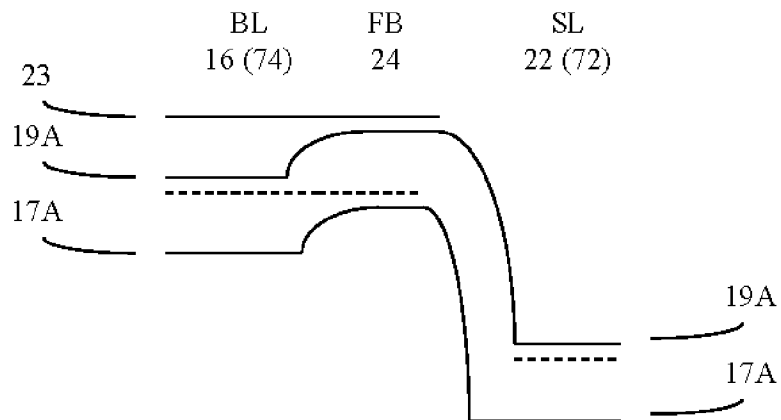


FIG. 37C

Exemplary Memory Array 280 with
Representative Memory Cells 250a, 250b, 250c and 250d

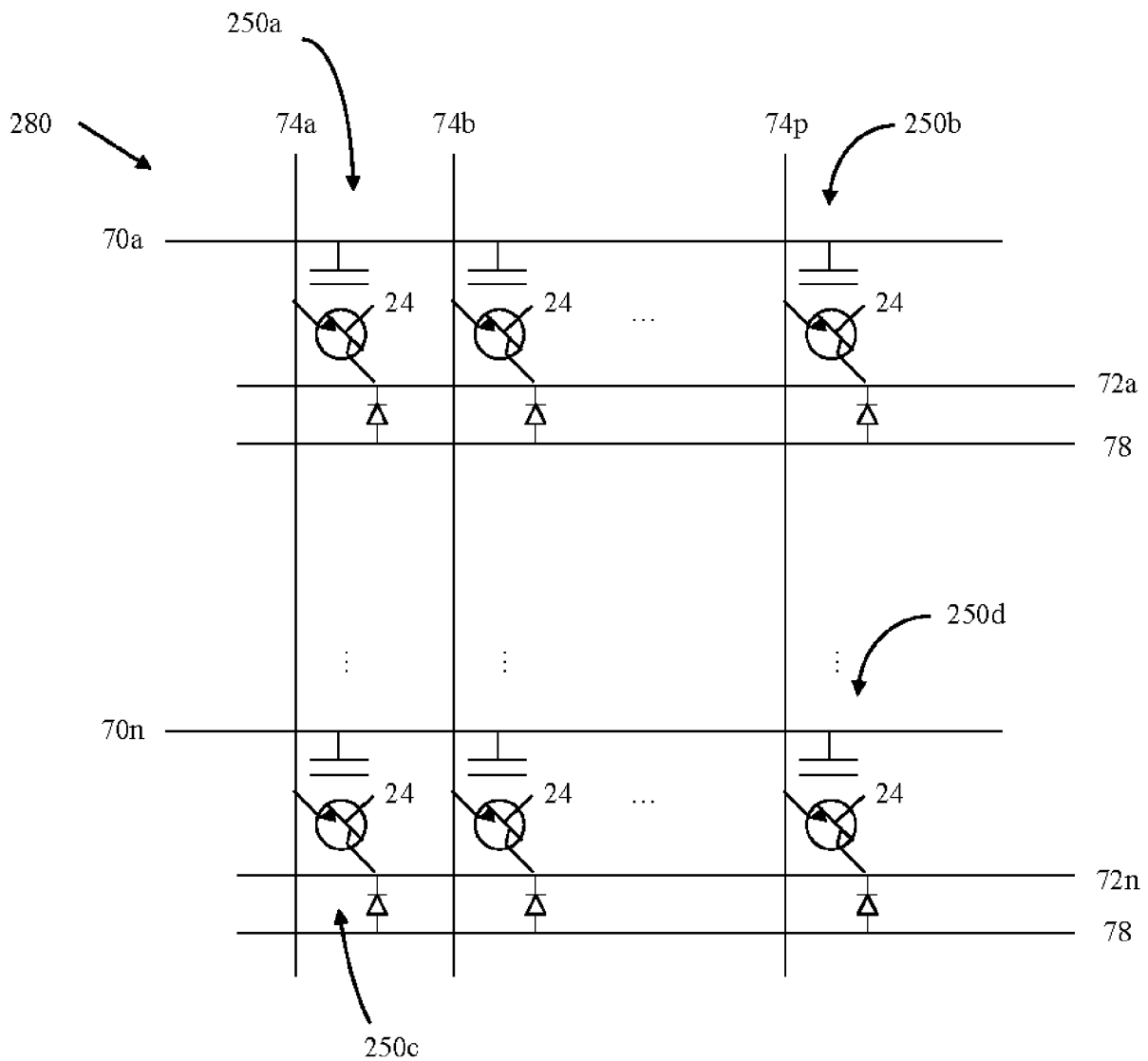


FIG. 38A

Array Hold Operation (All Memory Cells 250)

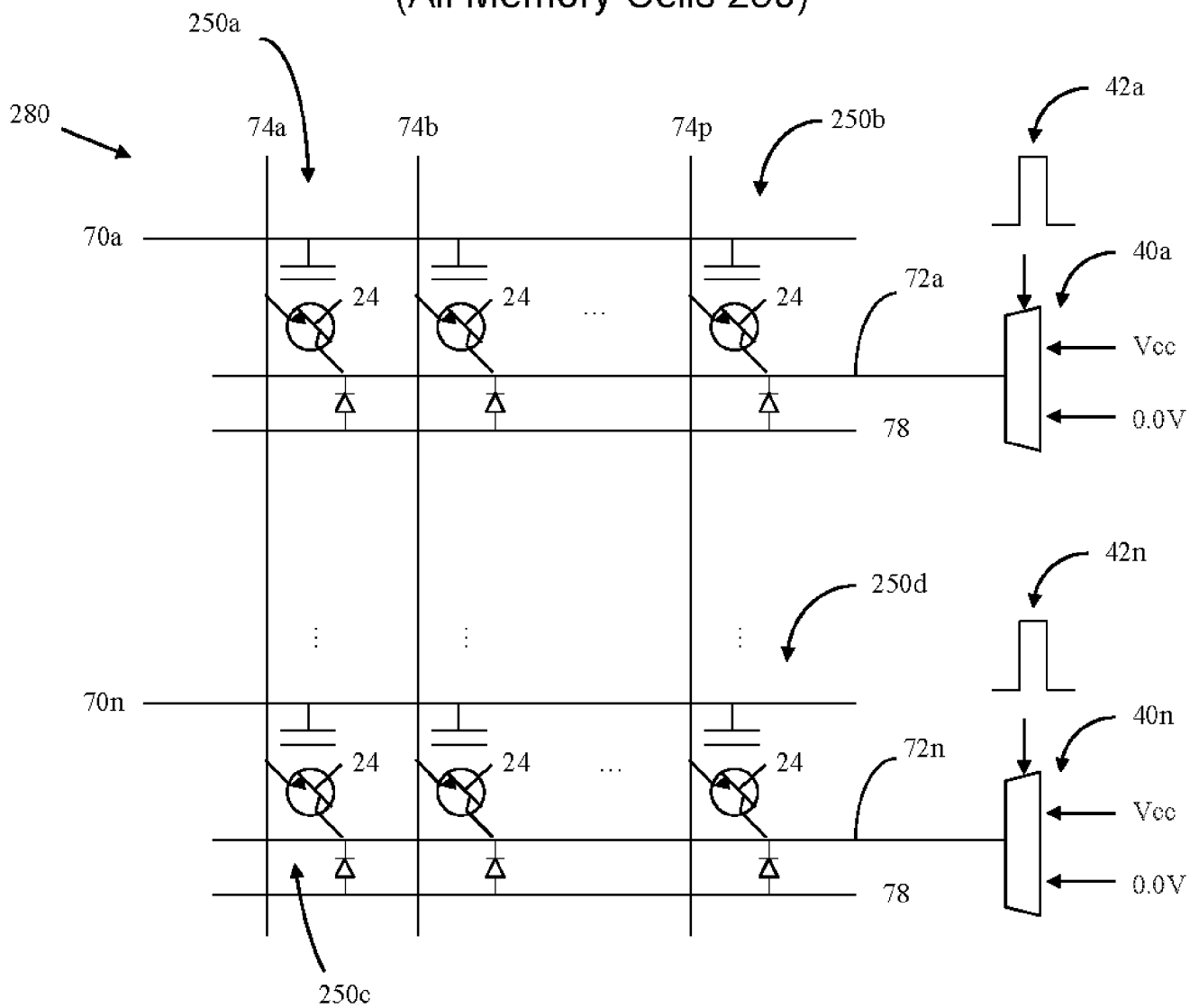


FIG. 38B

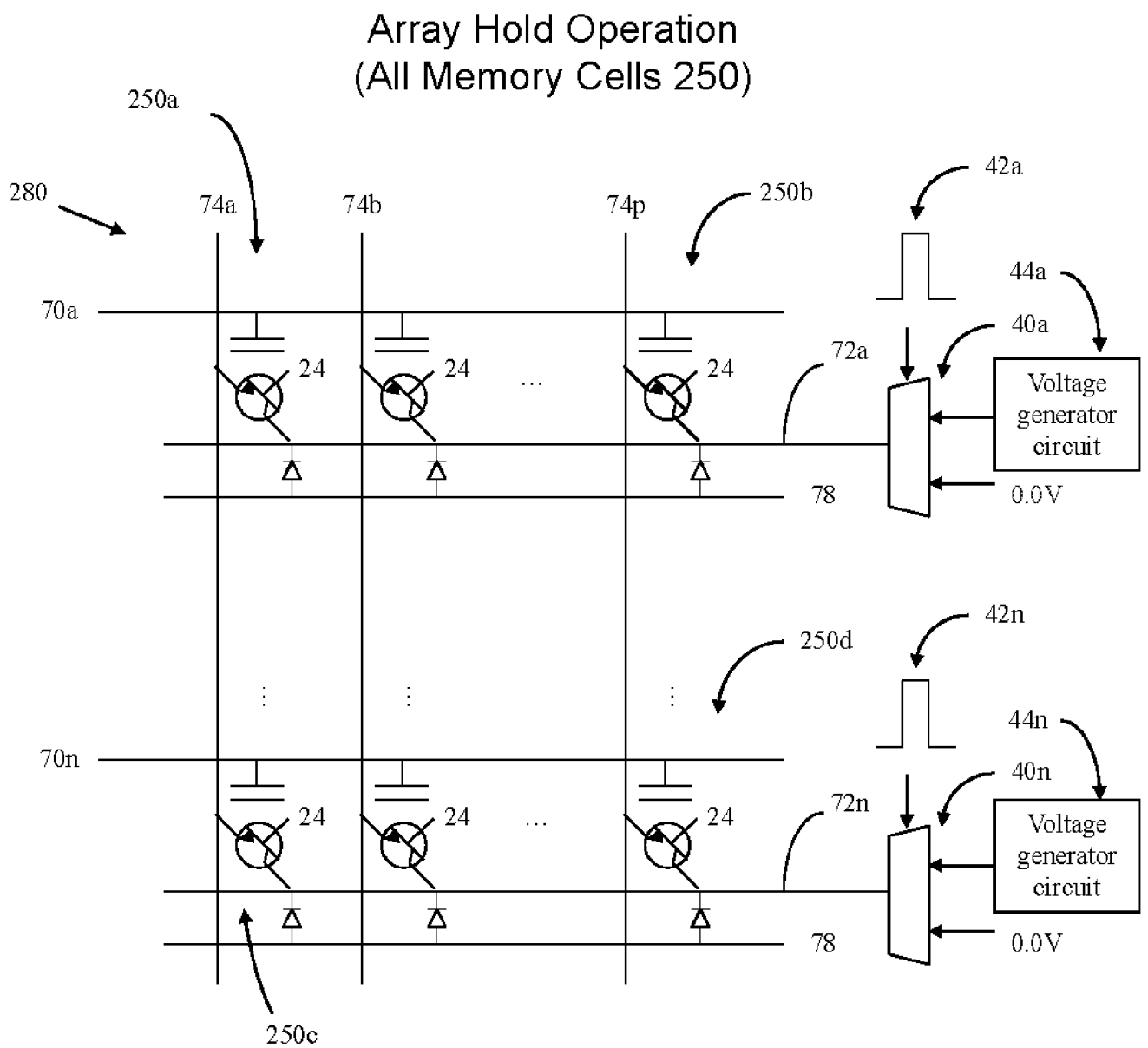


FIG. 38C

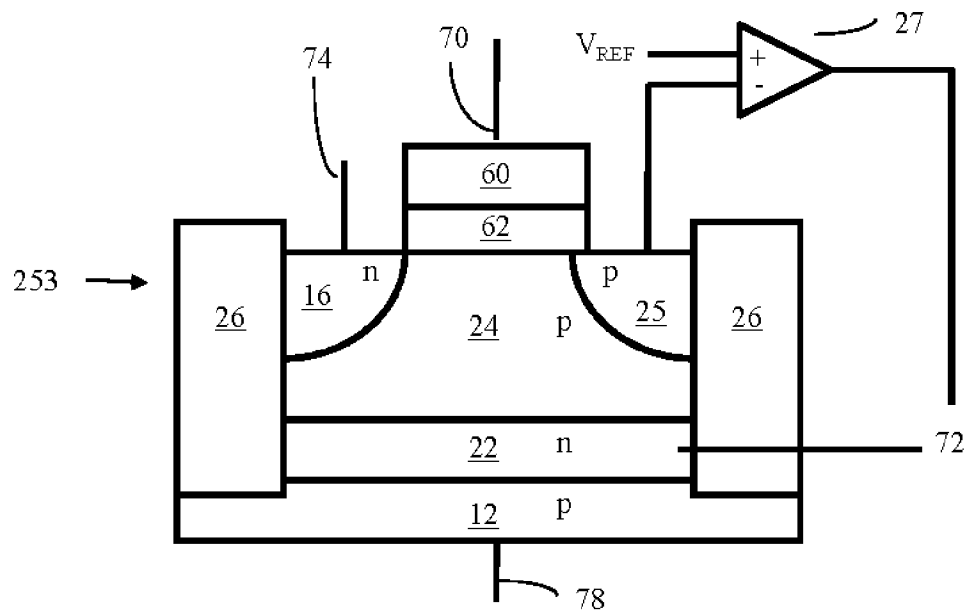


FIG. 38D

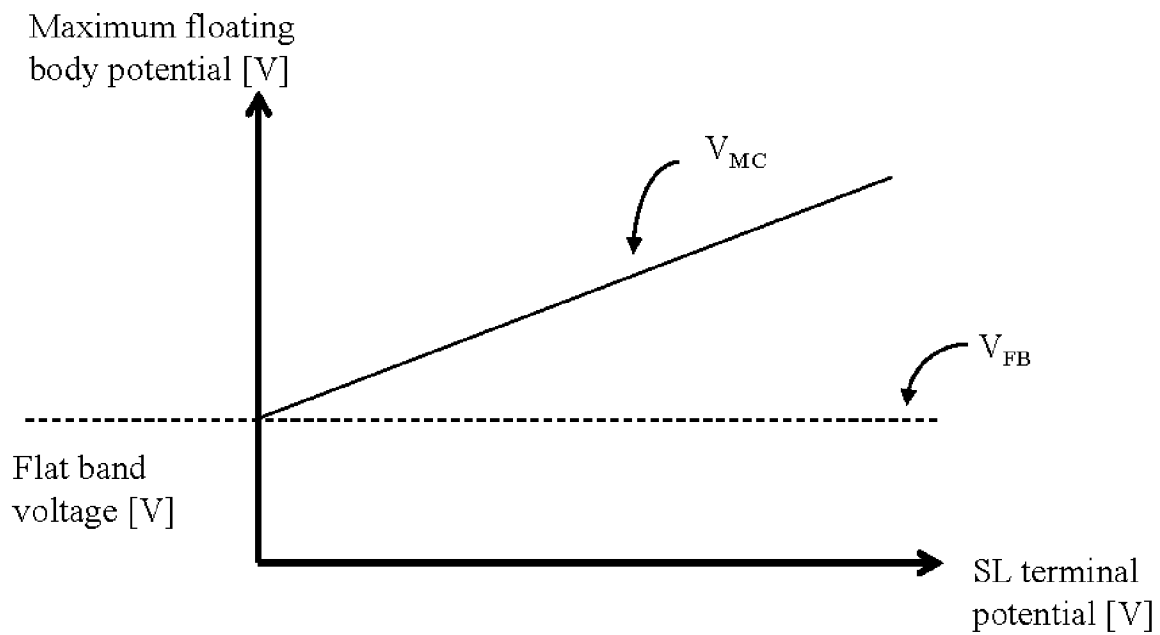


FIG. 39

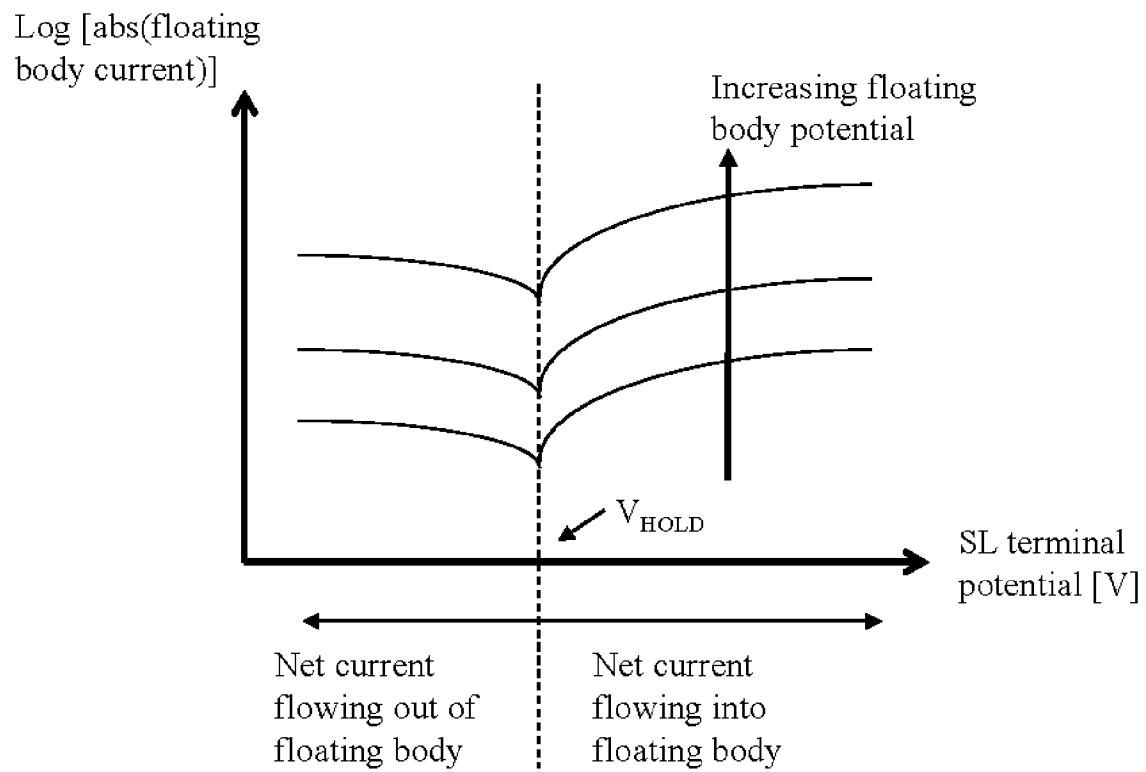


FIG. 40

Read Operation
(Memory Cell 250a)

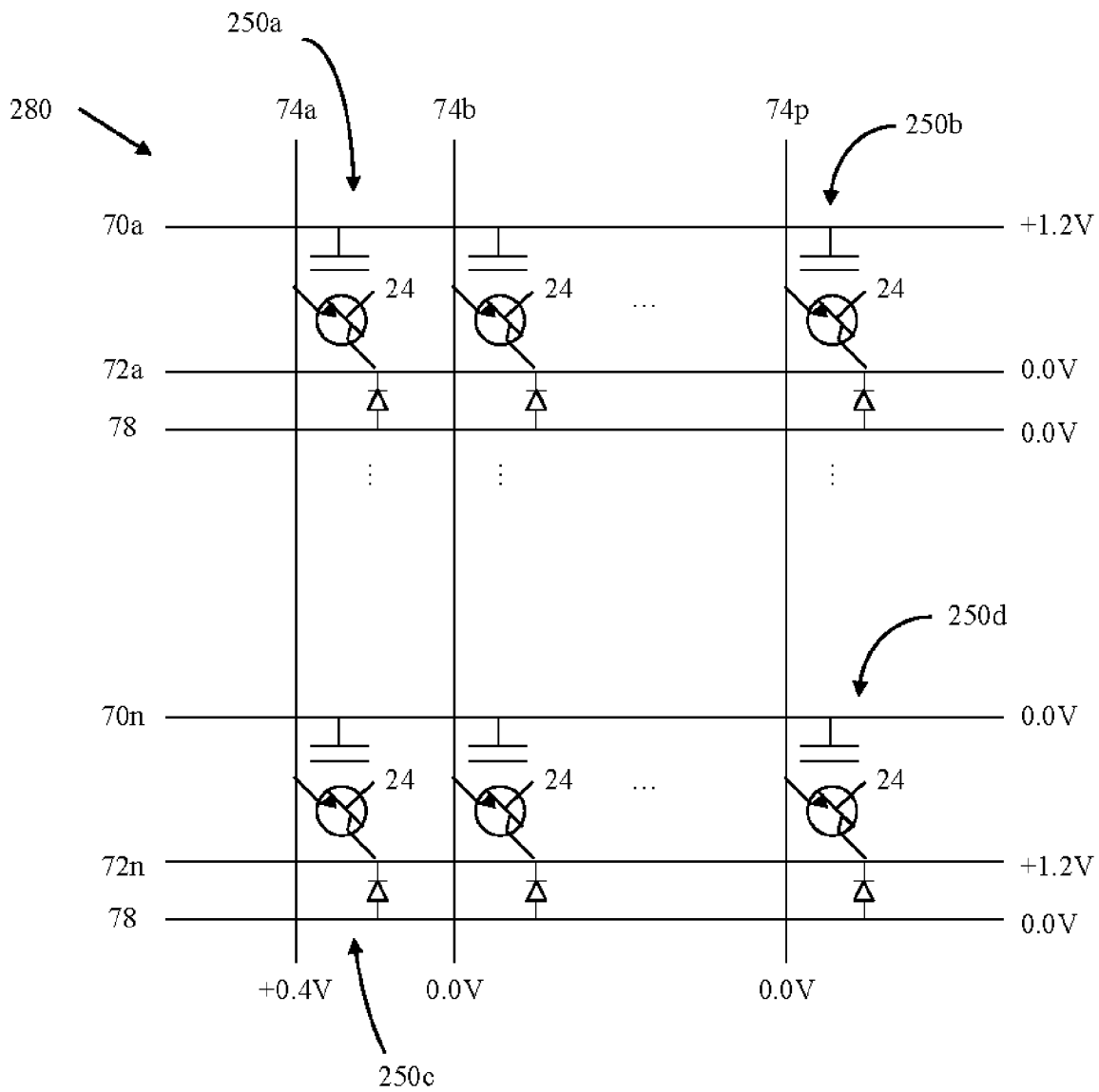


FIG. 41

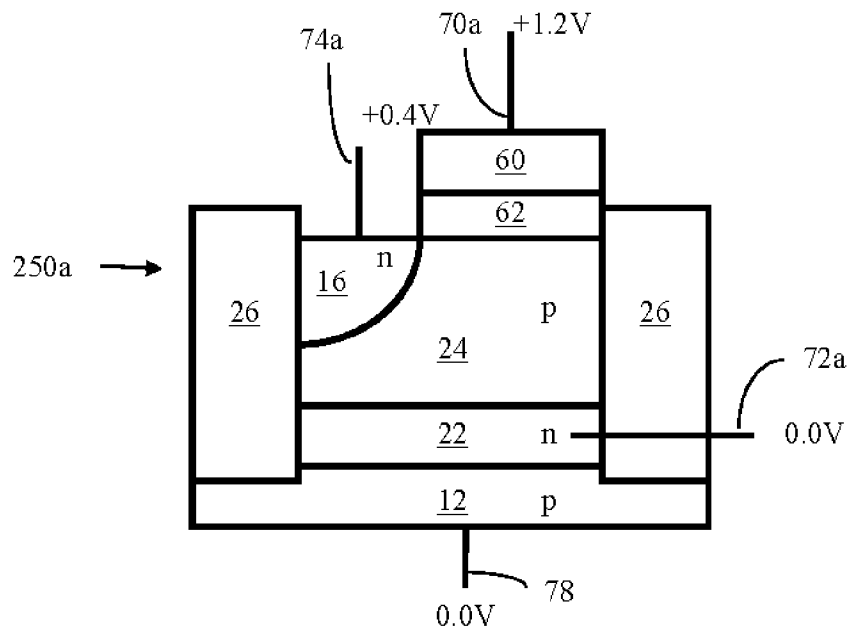


FIG. 42A

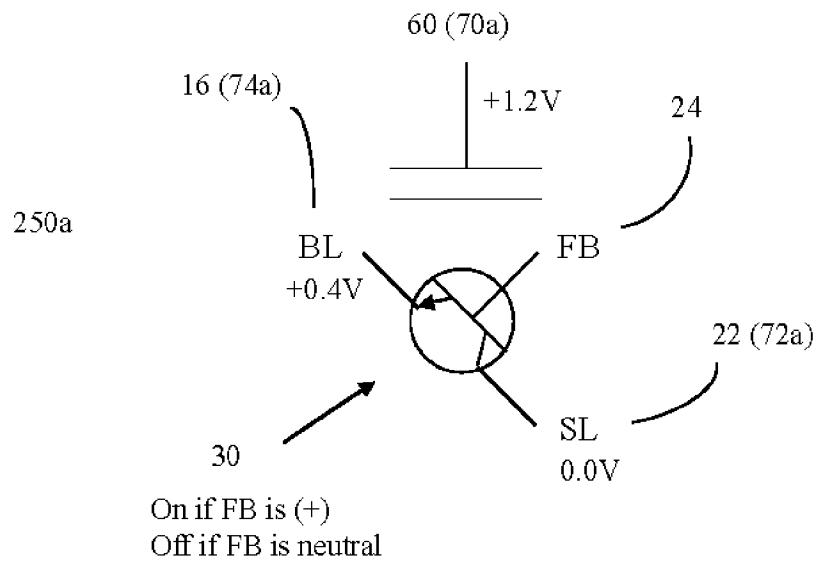


FIG. 42B

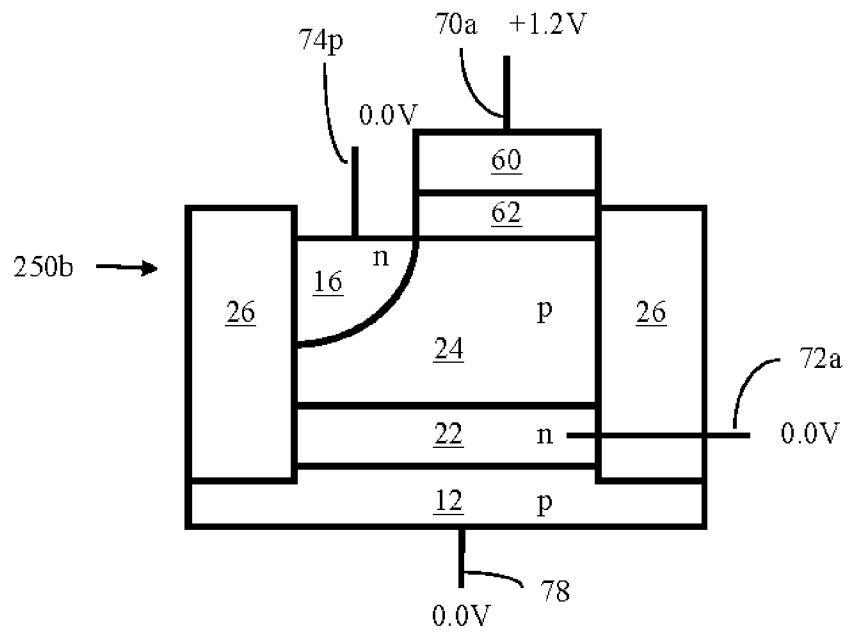


FIG. 42C

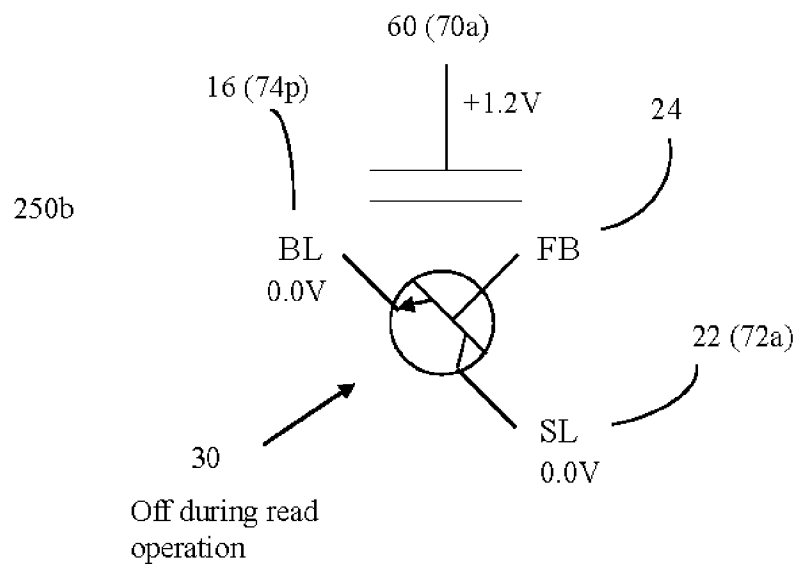


FIG. 42D

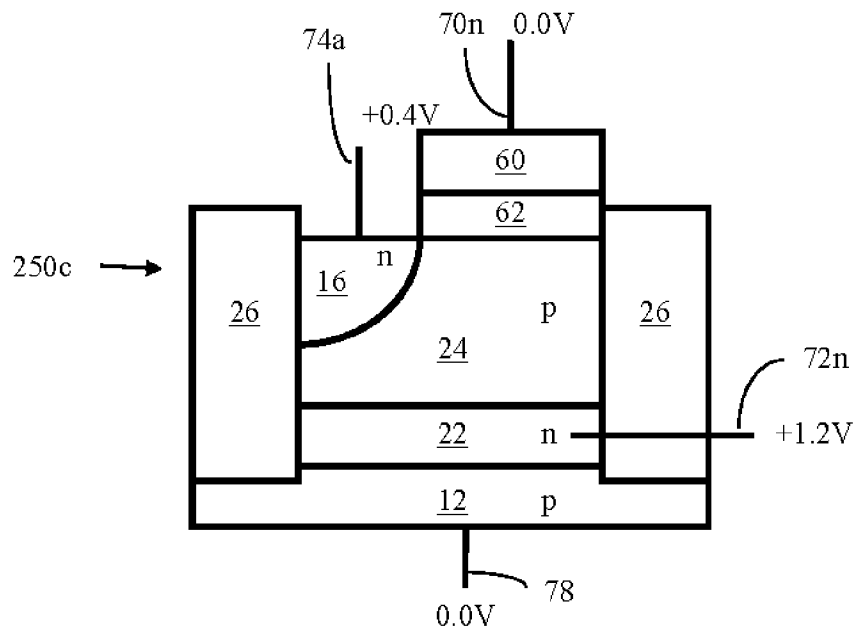


FIG. 42E

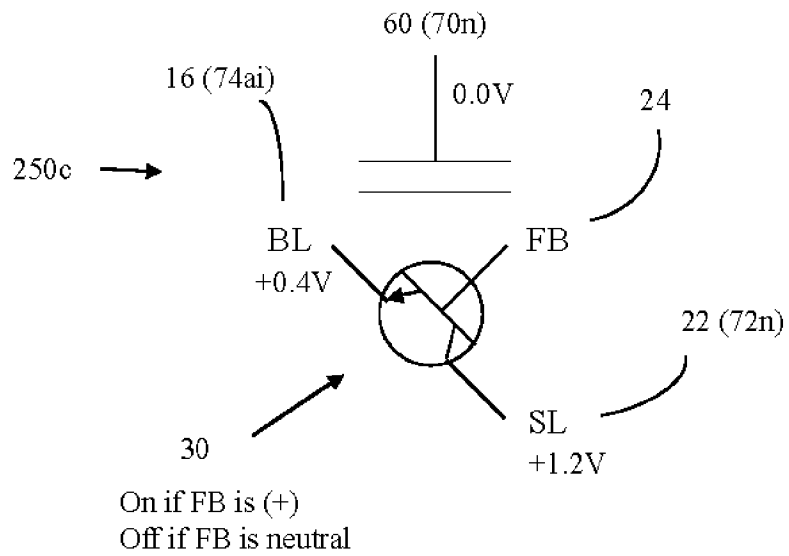


FIG. 42F

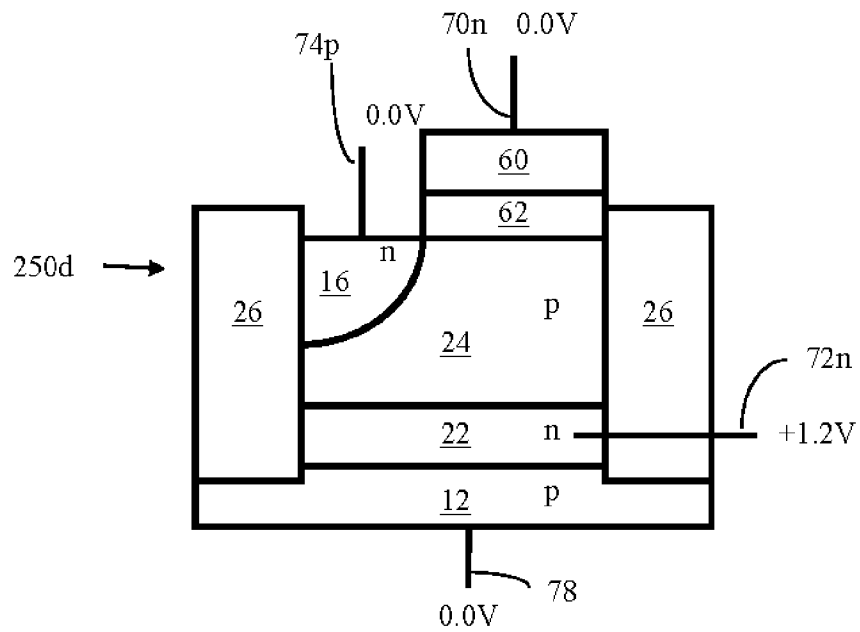


FIG. 42G

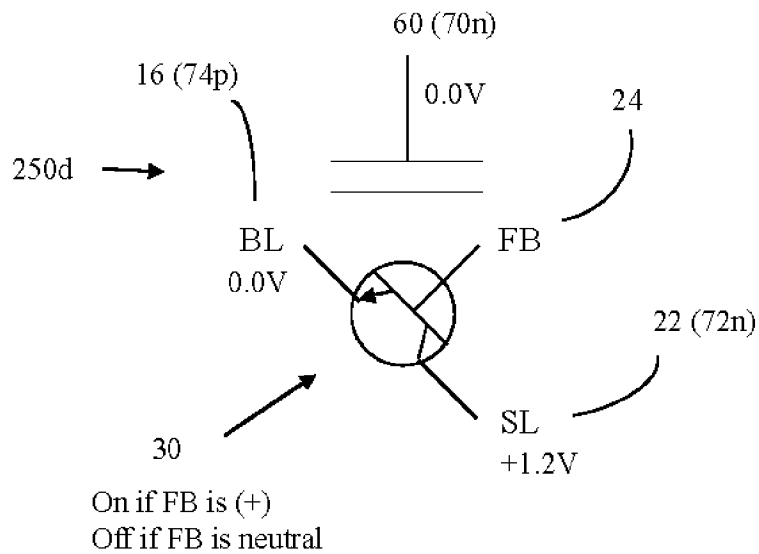


FIG. 42H

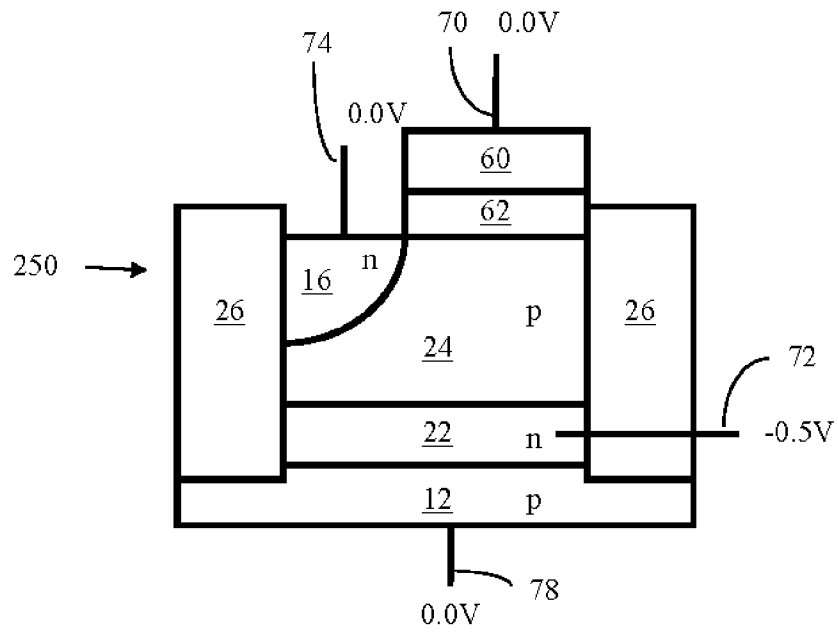


FIG. 43A

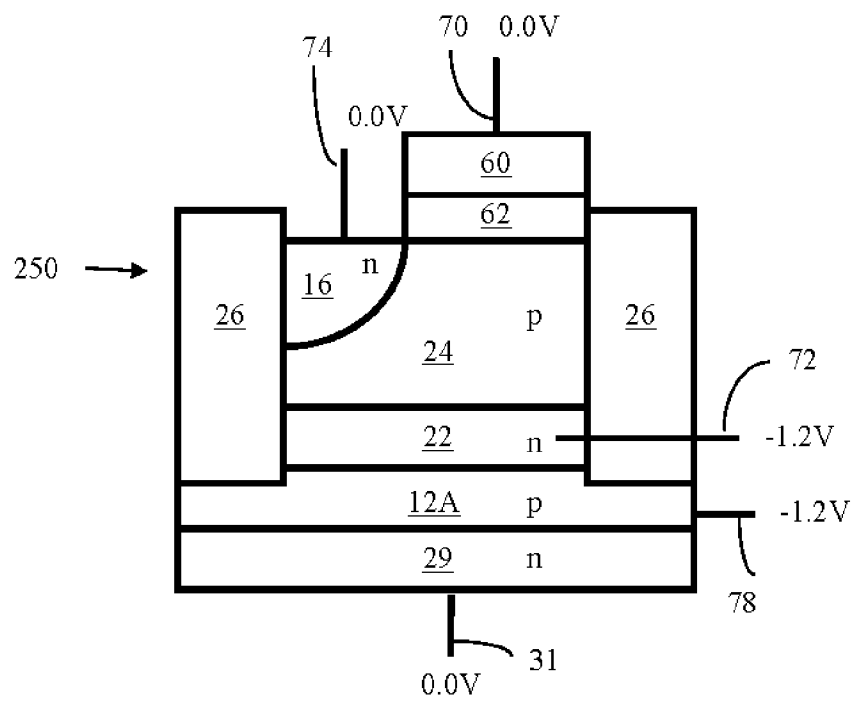


FIG. 43B

Row Write Logic-0 Operation (Memory Cells 250a and 250b)

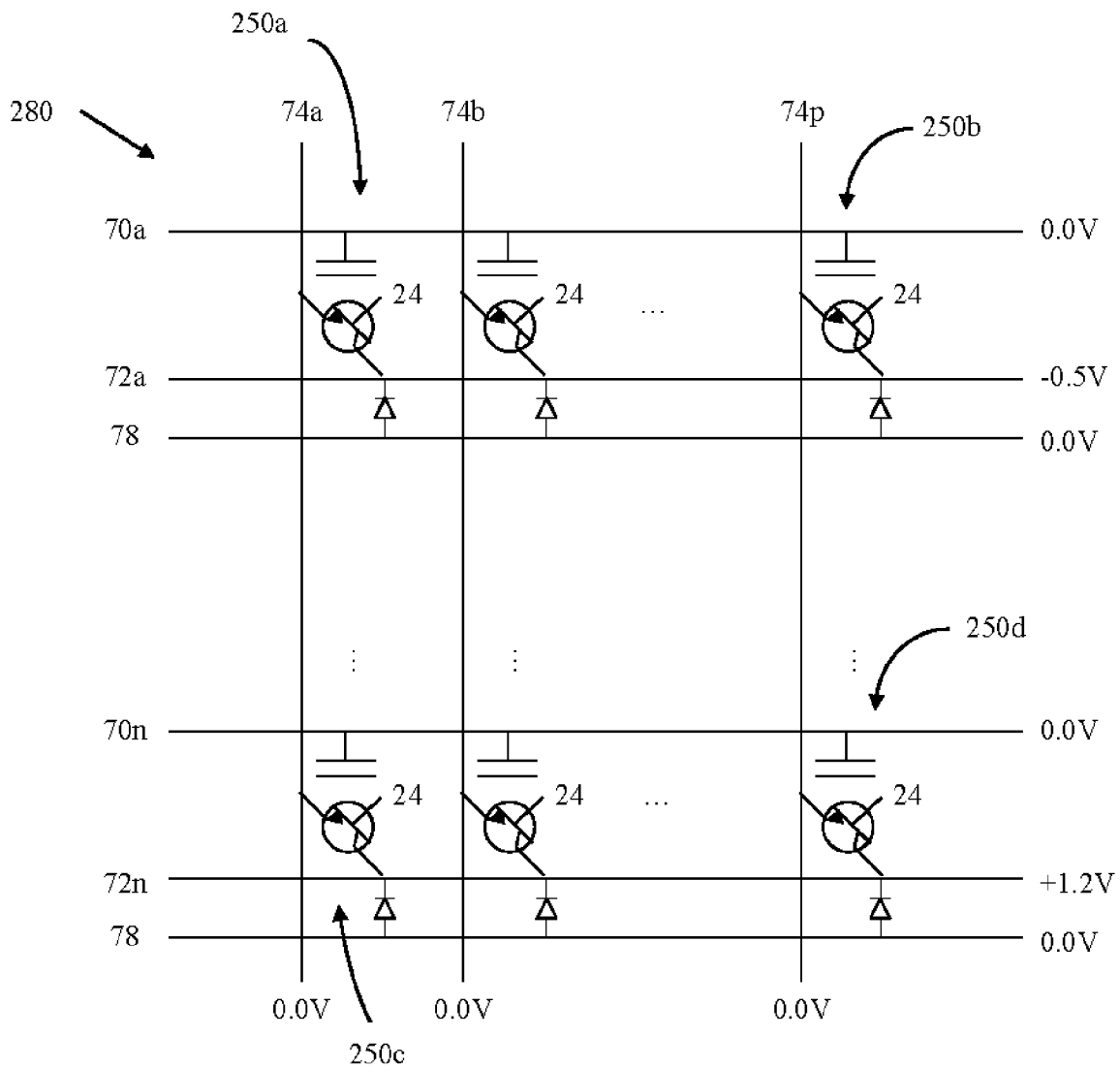


FIG. 44

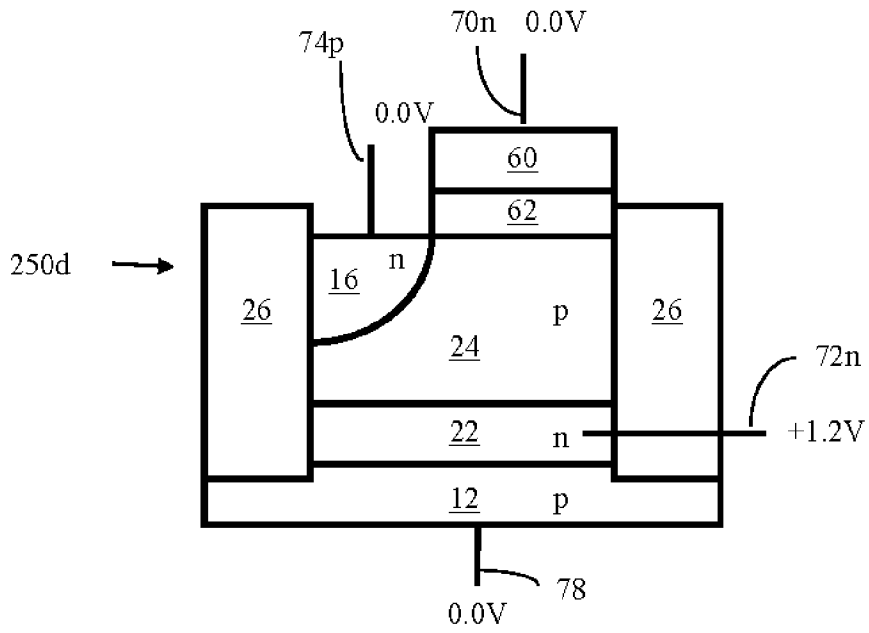


FIG. 45A

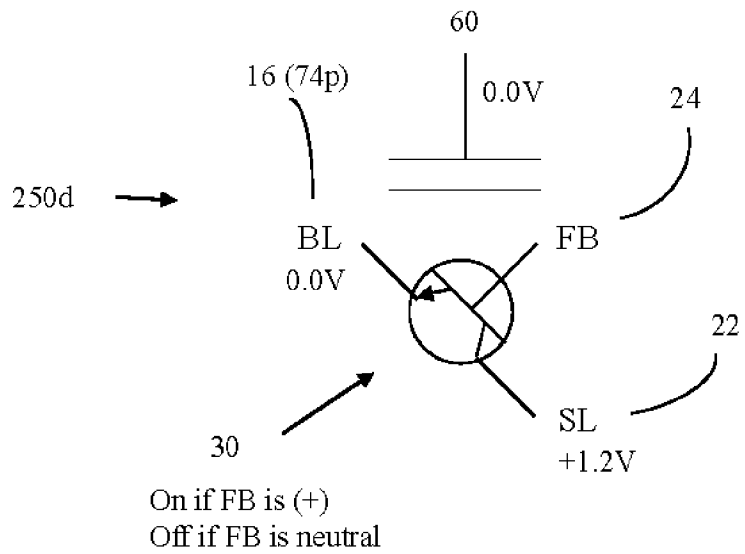


FIG. 45B

Column Write Logic-0 Operation (Memory Cells 250a and 250c)

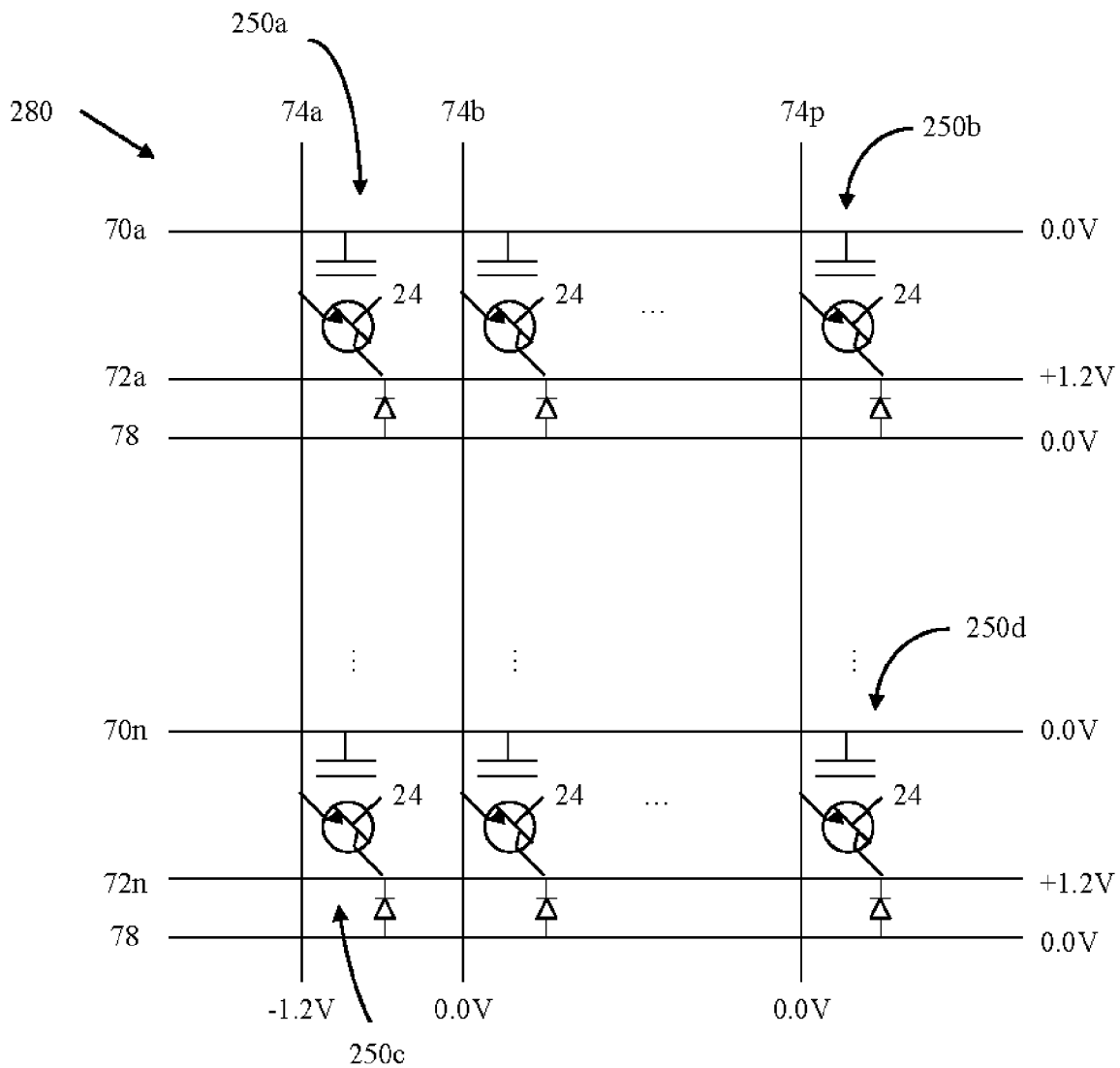


FIG. 46

Write Logic-0 Operation (Single Memory Cell 250a)

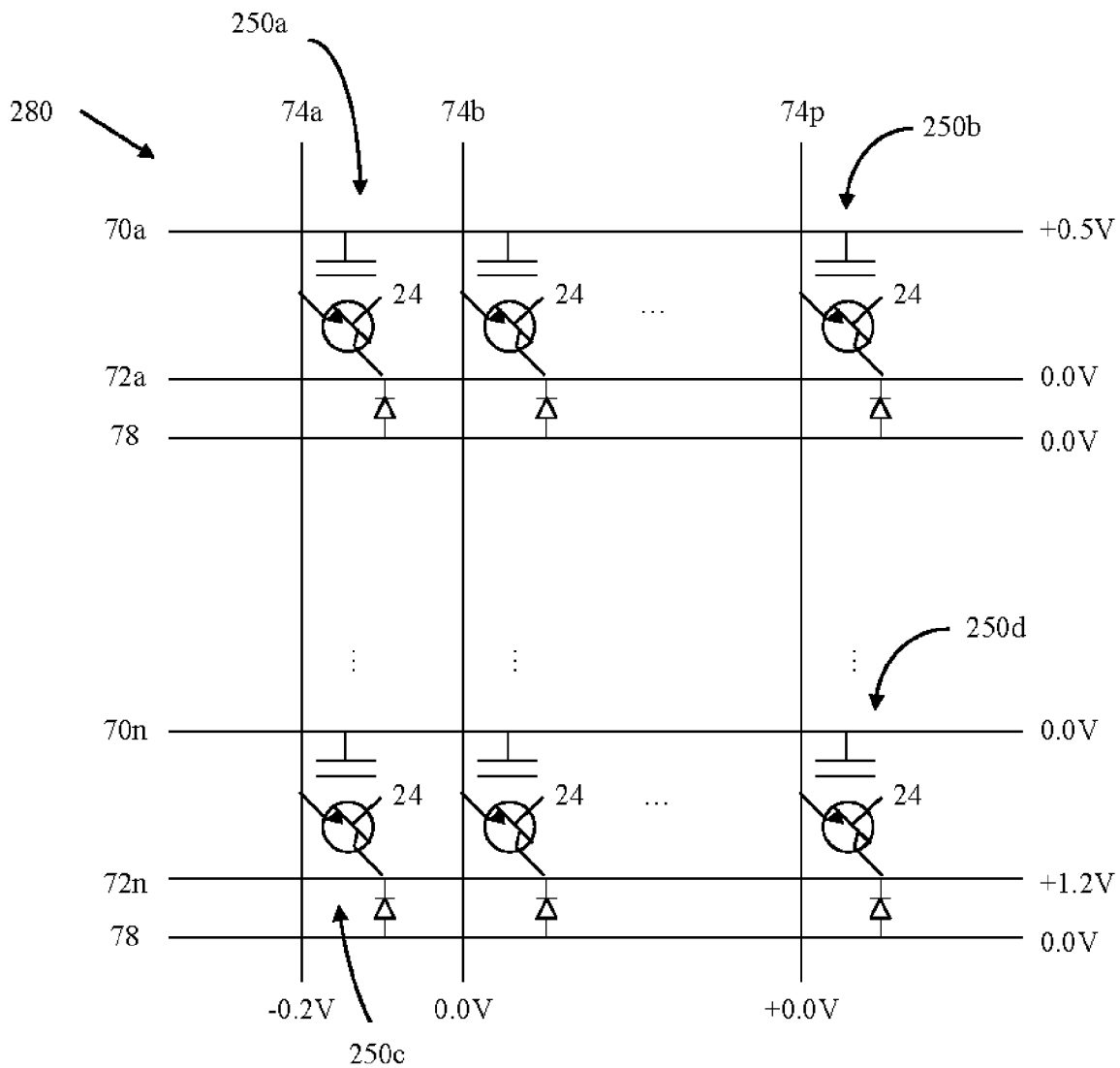


FIG. 47

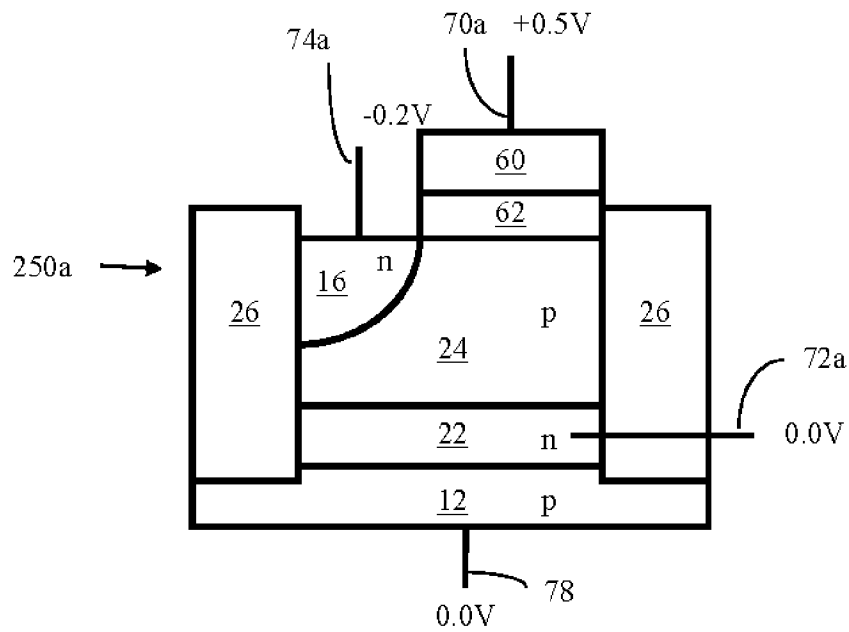


FIG. 48A

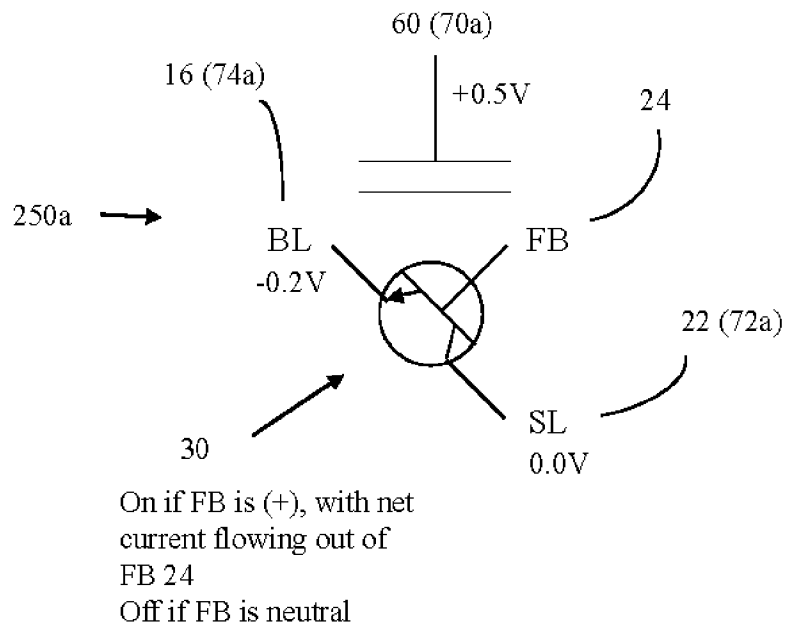


FIG. 48B

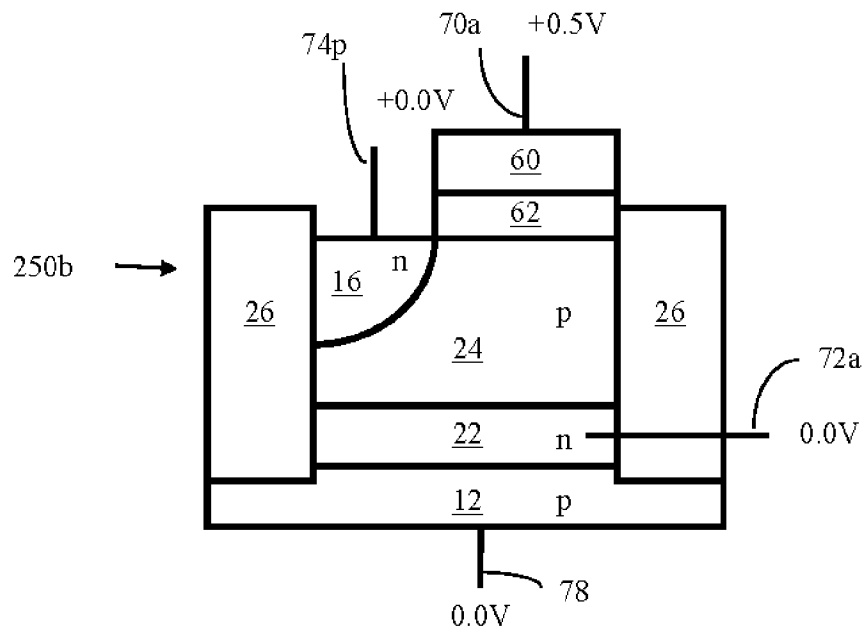


FIG. 48C

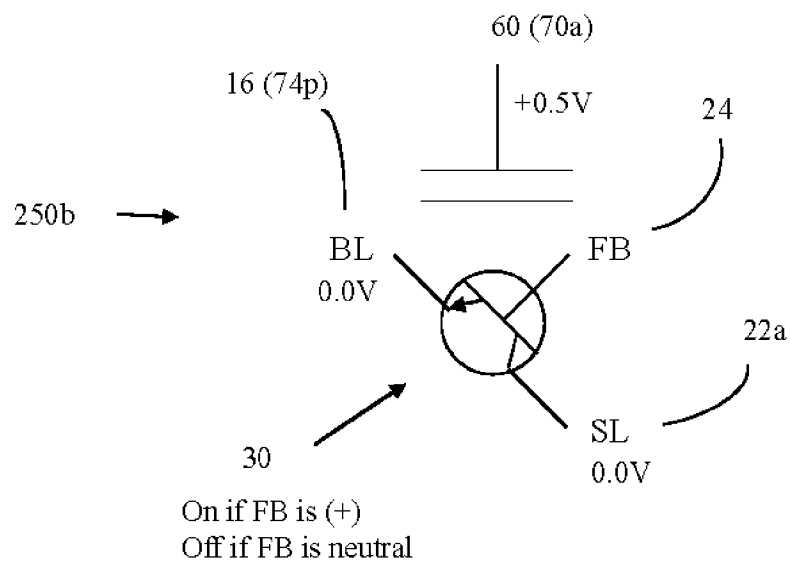


FIG. 48D

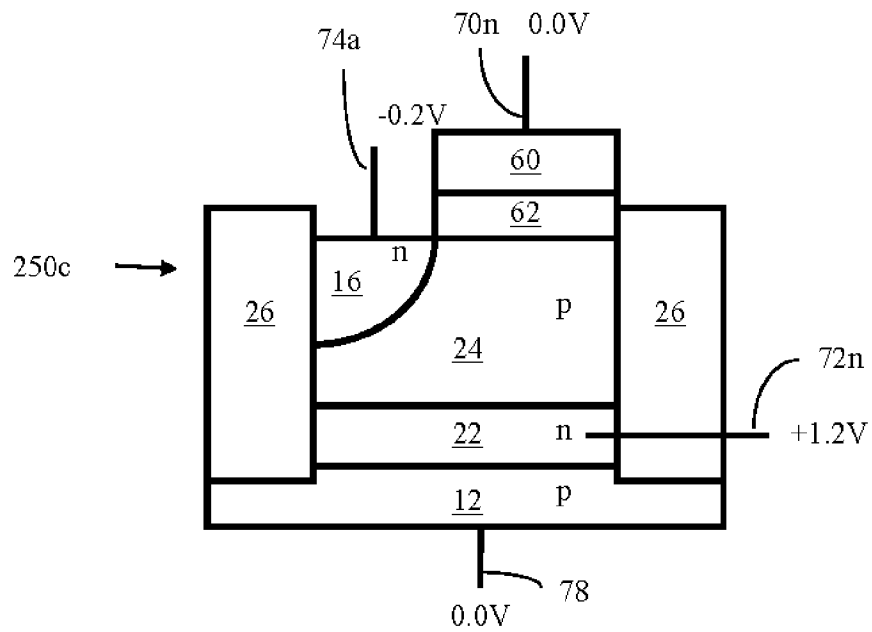
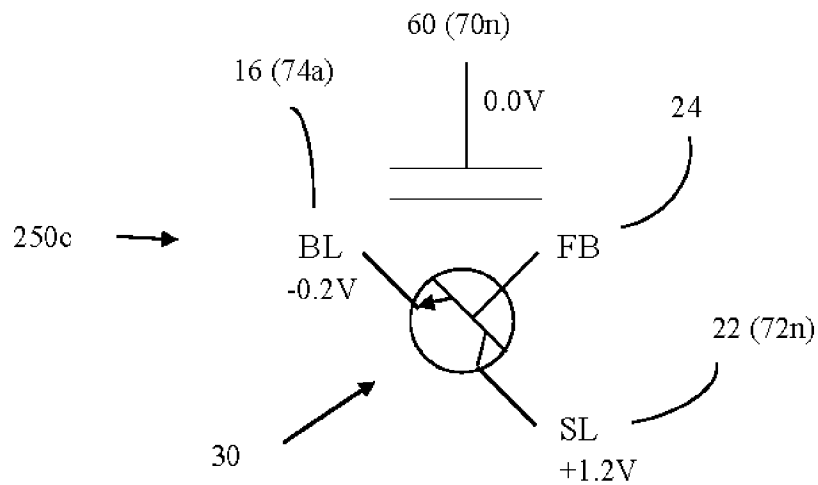


FIG. 48E



On if FB is (+); forward
bias current is balanced
by higher bipolar base
current
Off if FB is neutral

FIG. 48F

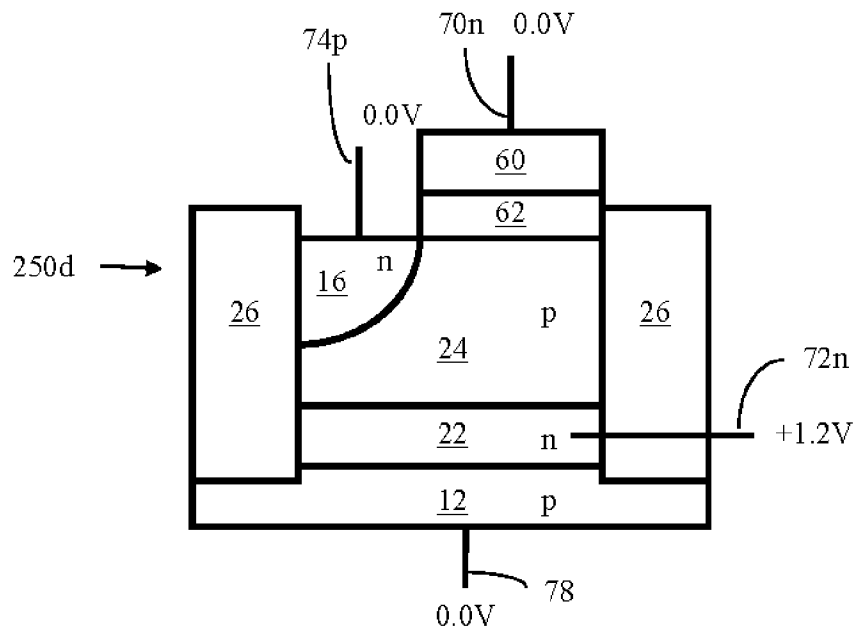


FIG. 48G

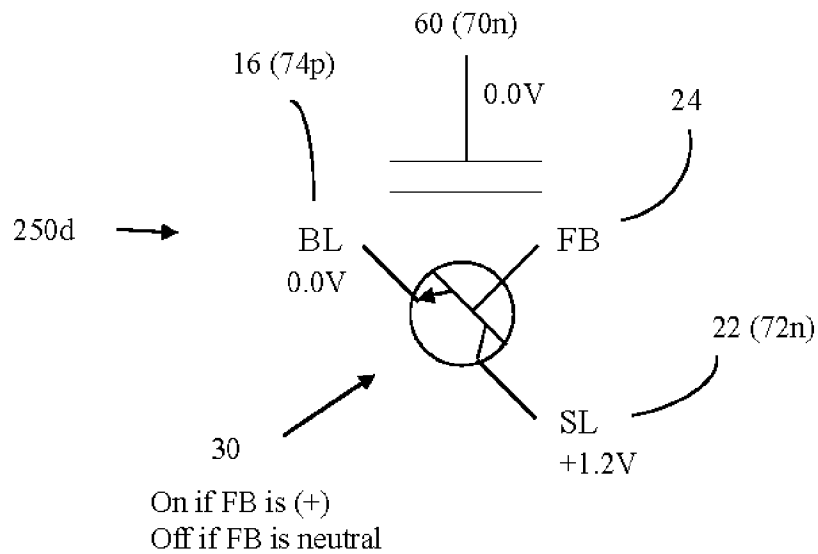


FIG. 48H

Write Logic-1 Operation – GIDL

(Single Memory Cell 250a)

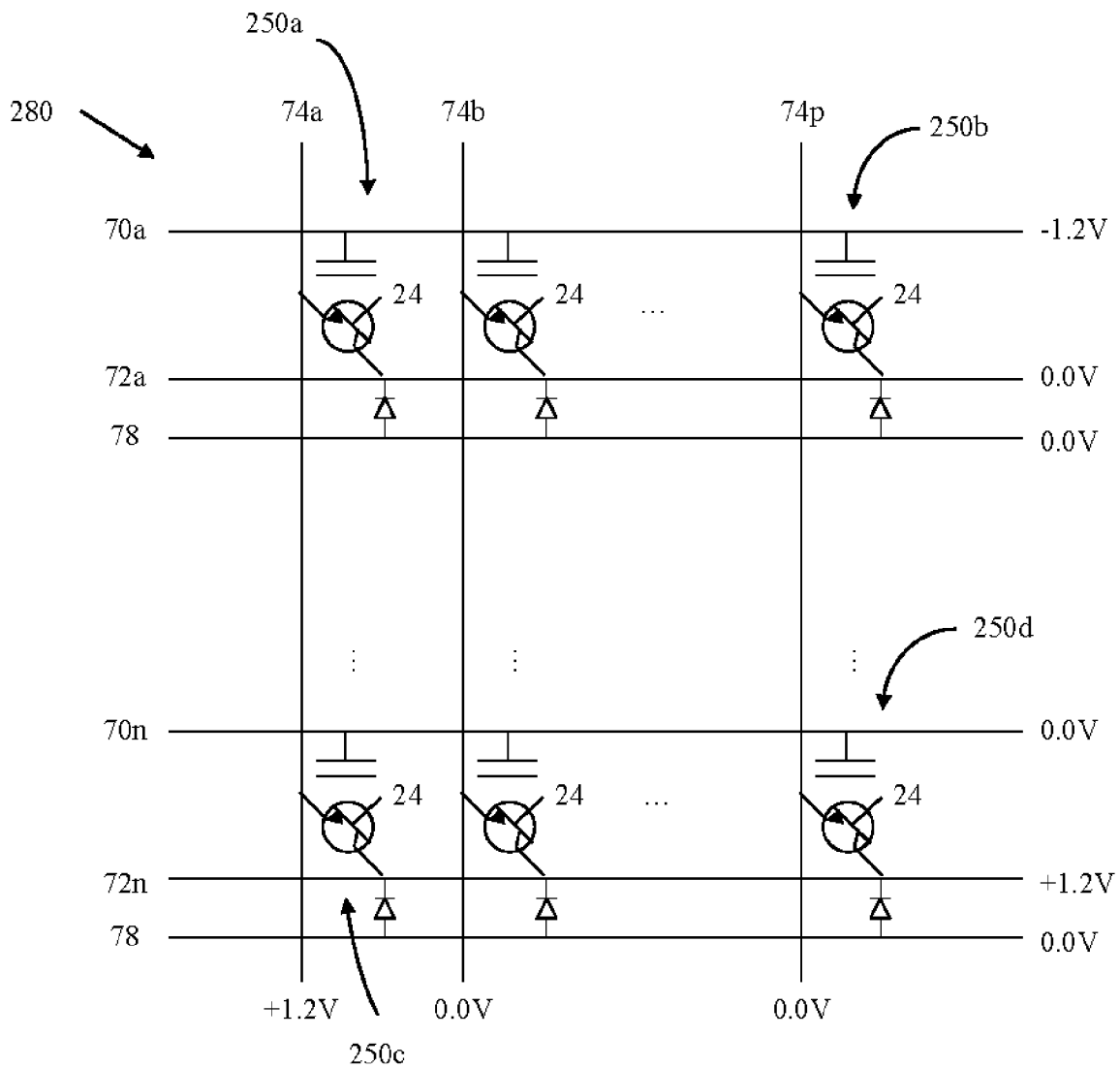


FIG. 49

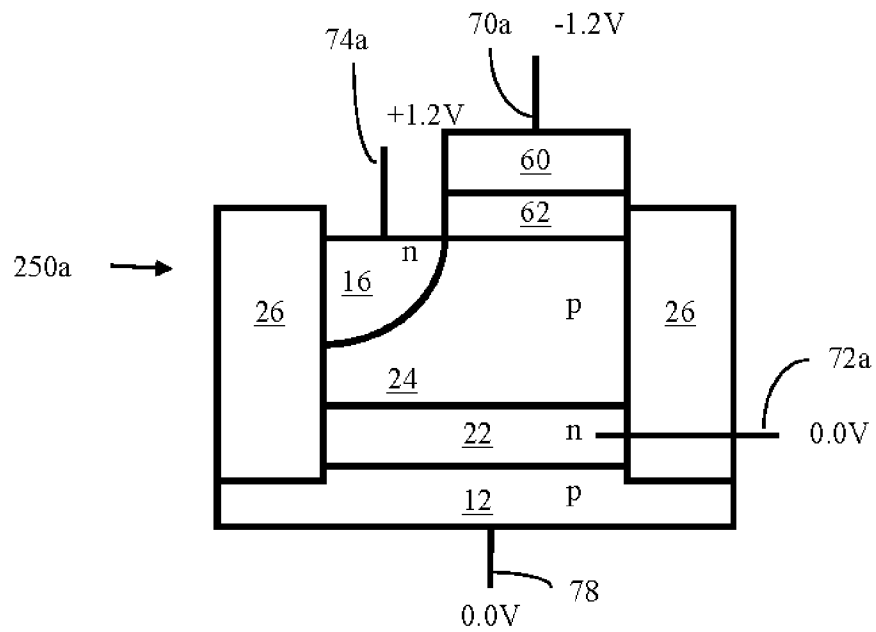


FIG. 50A

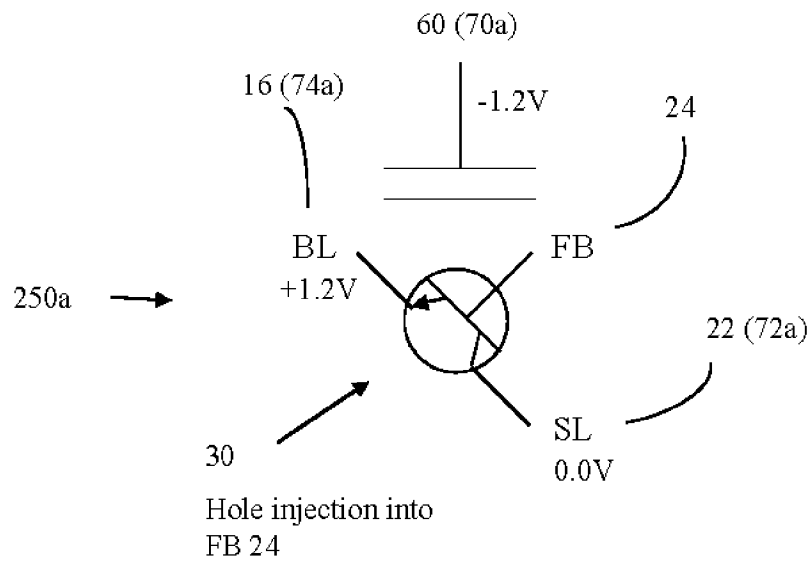


FIG. 50B

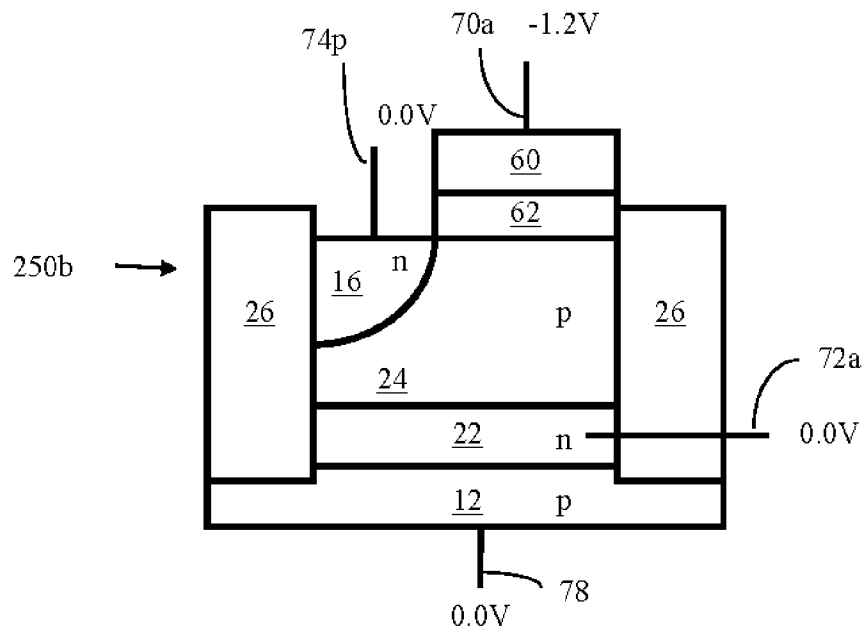


FIG. 50C

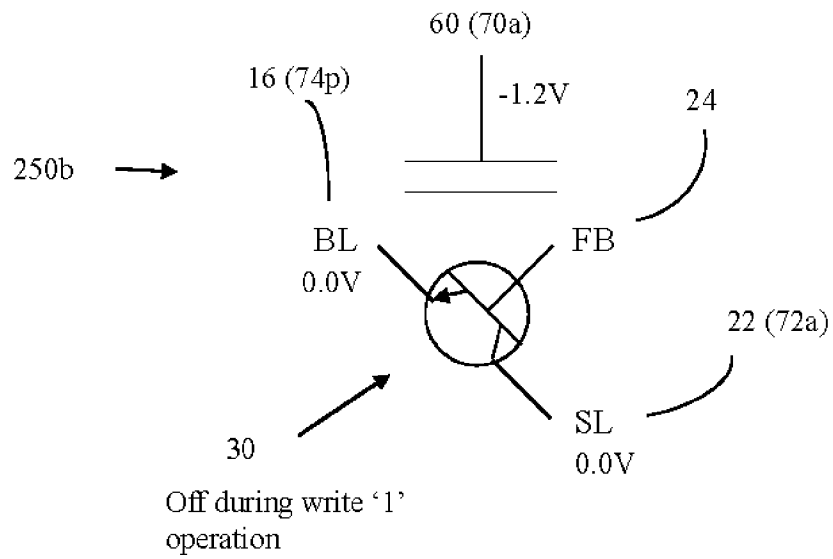


FIG. 50D

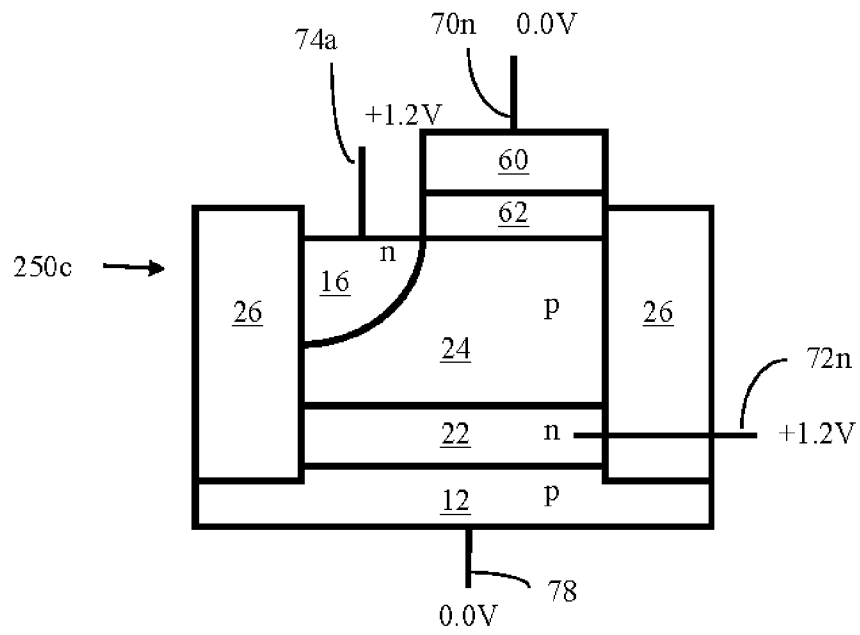


FIG. 50E

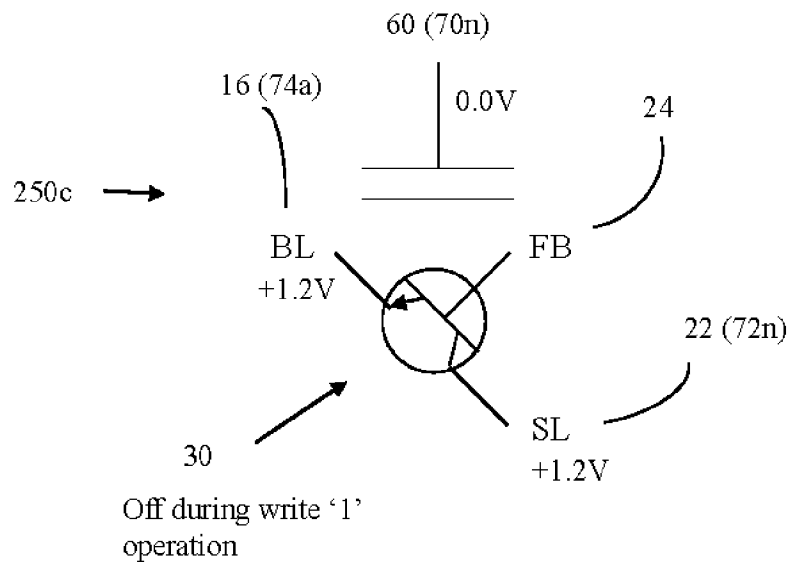


FIG. 50F

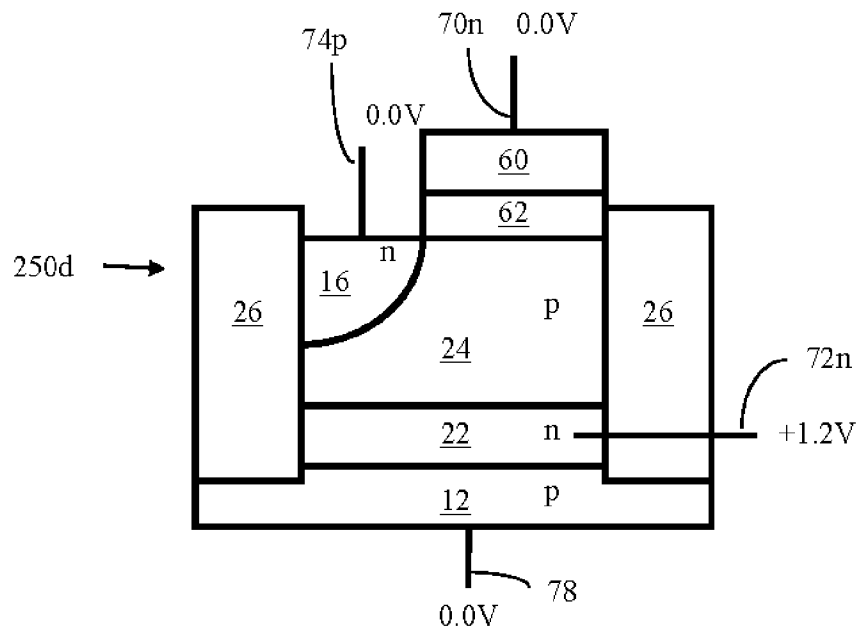


FIG. 50G

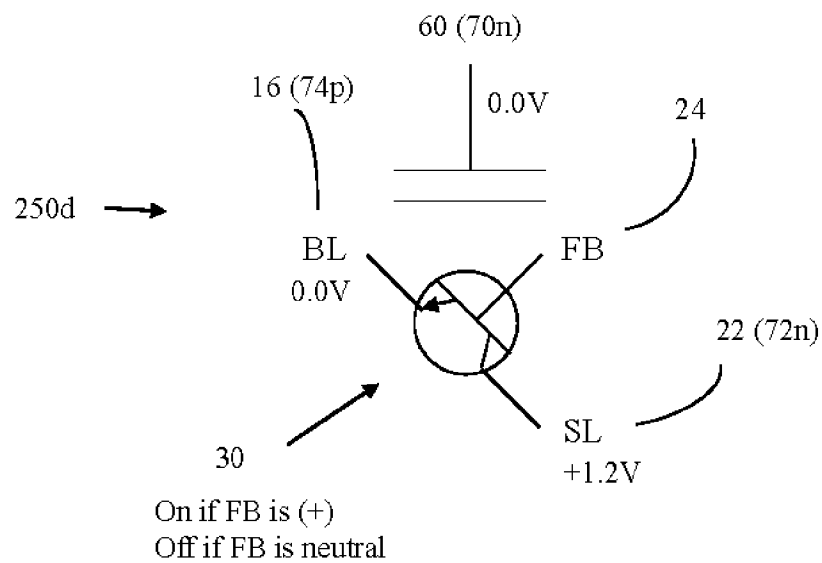


FIG. 50H

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 250a)

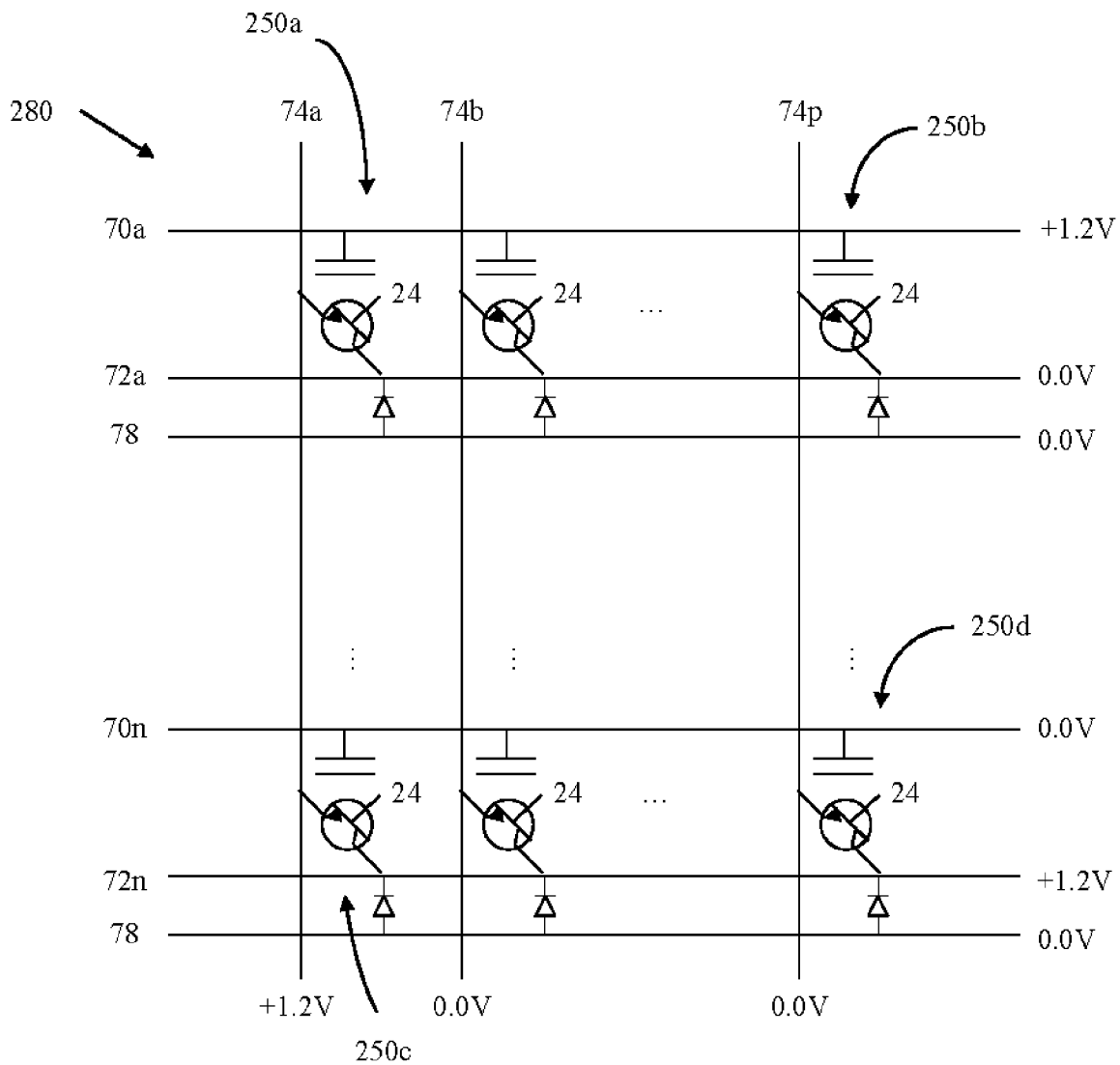


FIG. 51

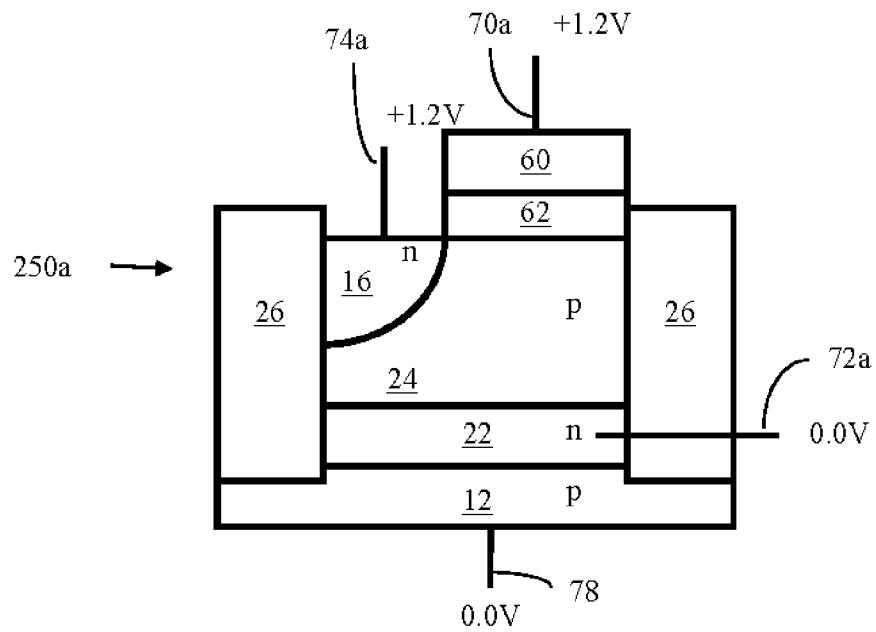


FIG. 52A

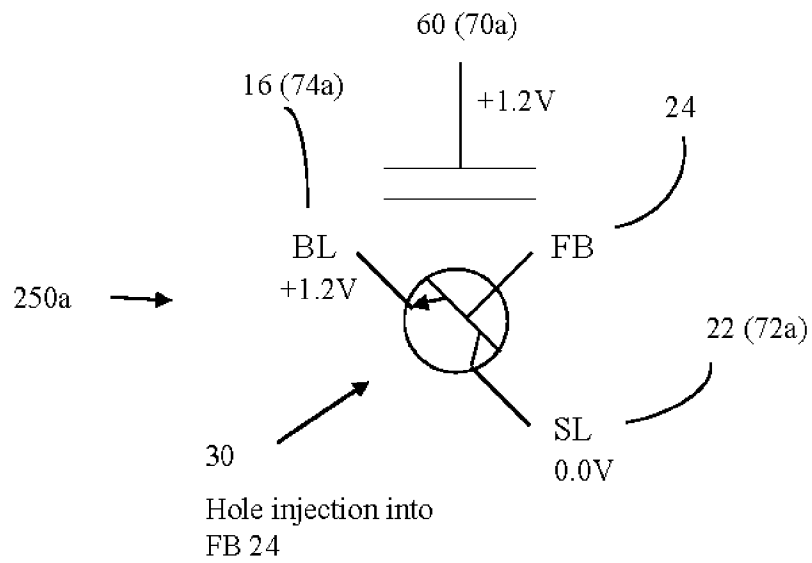


FIG. 52B

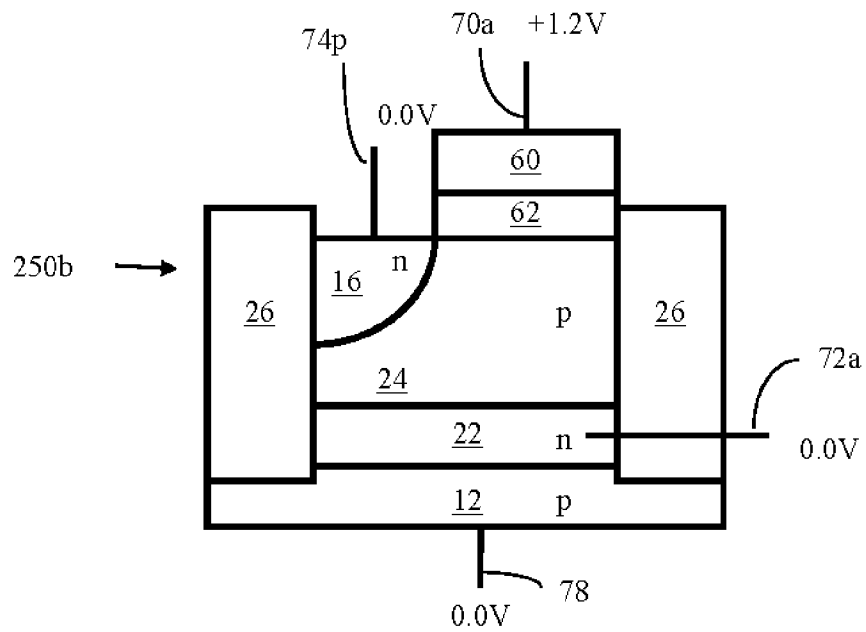


FIG. 52C

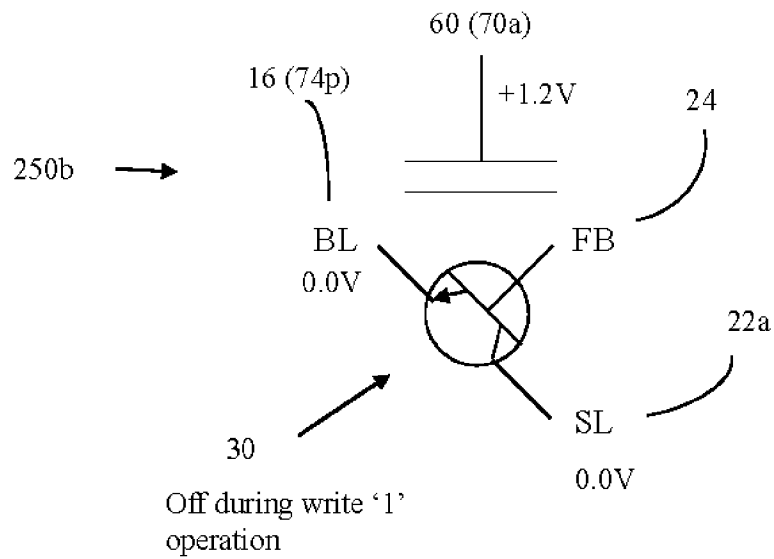


FIG. 52D

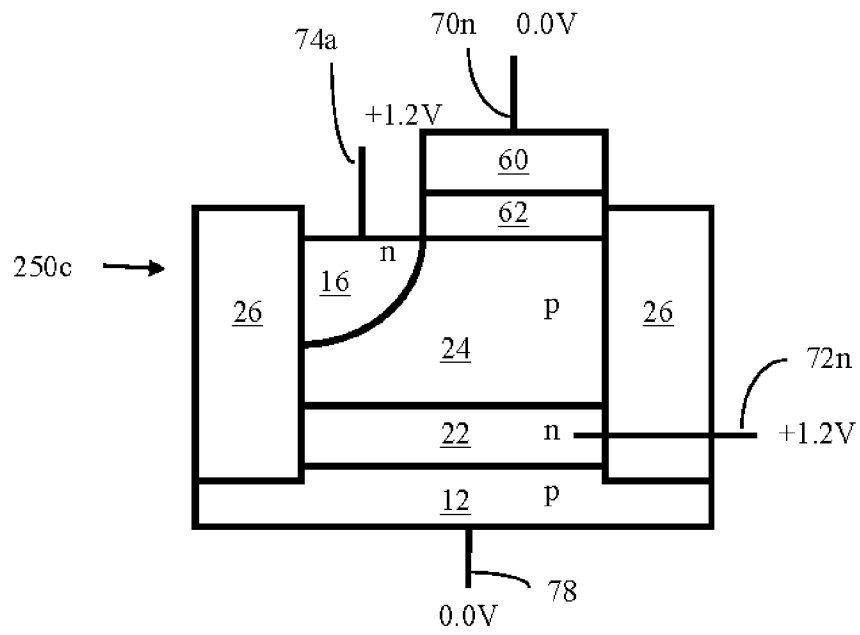


FIG. 52E

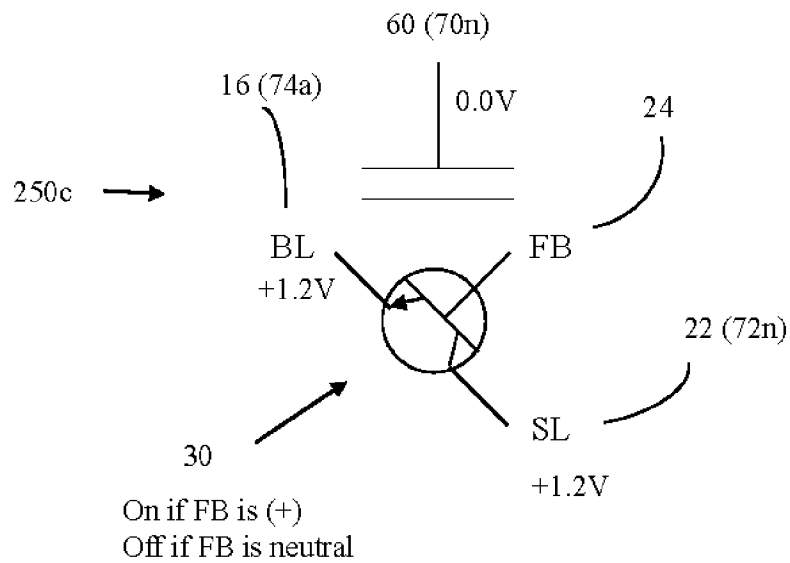


FIG. 52F

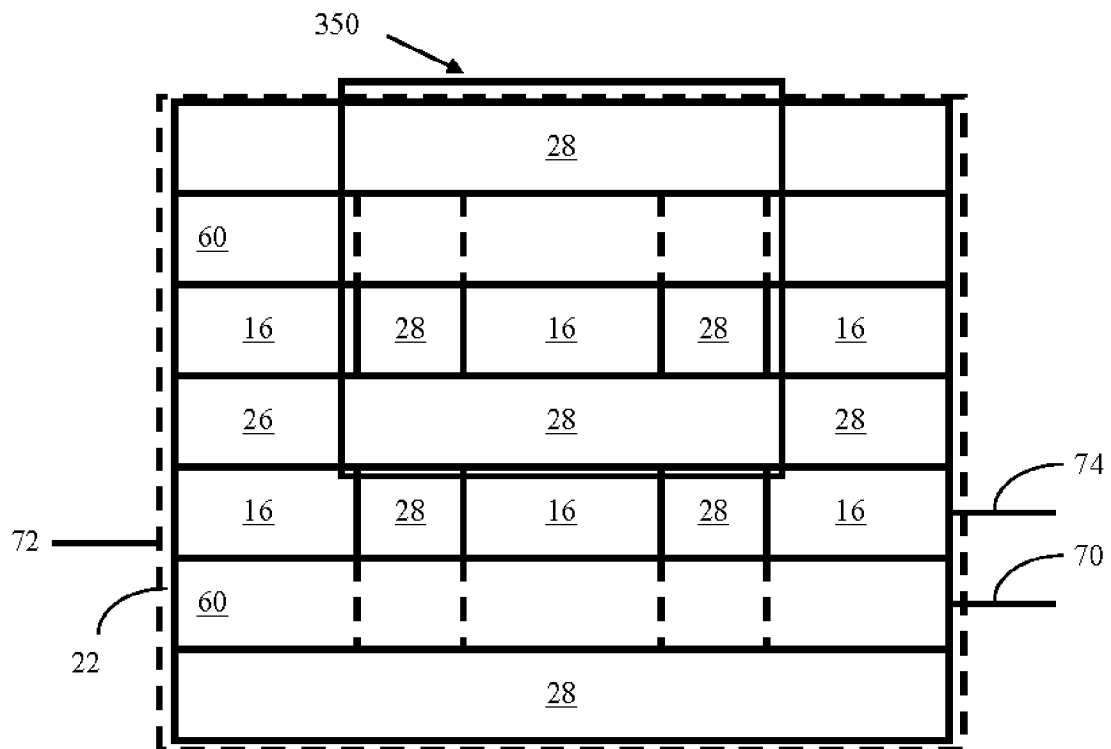


FIG. 53A

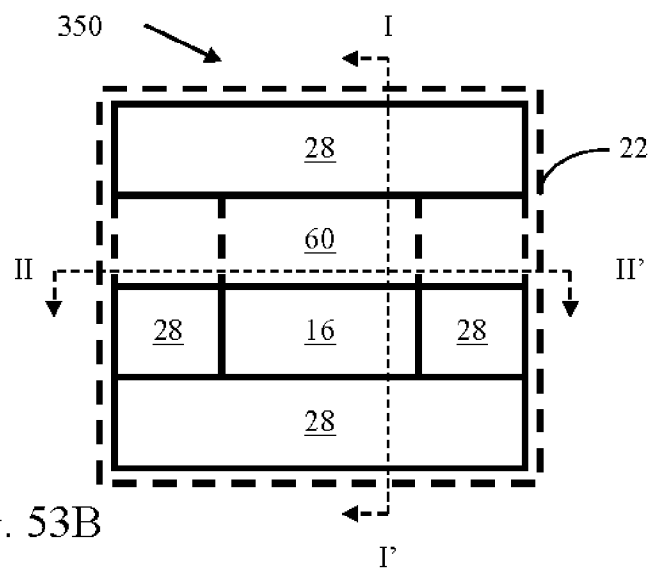


FIG. 53B

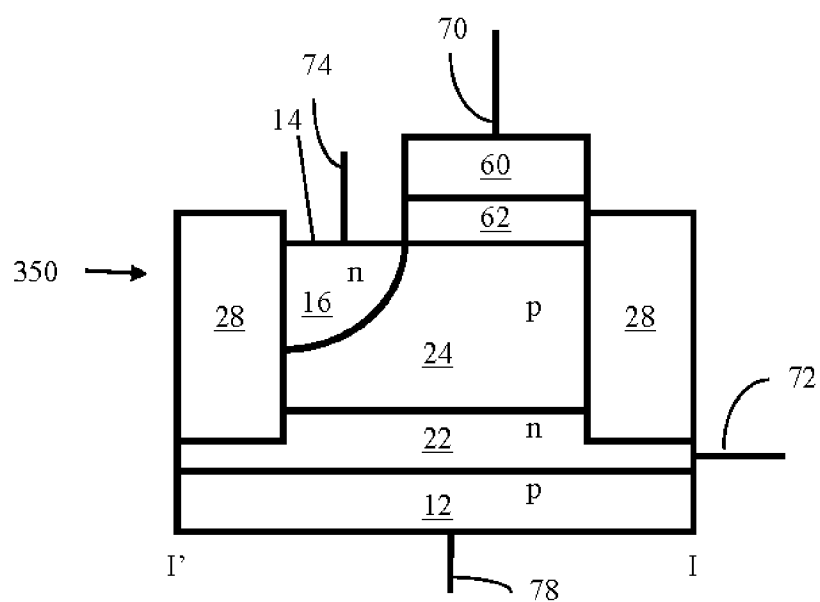


FIG. 53C

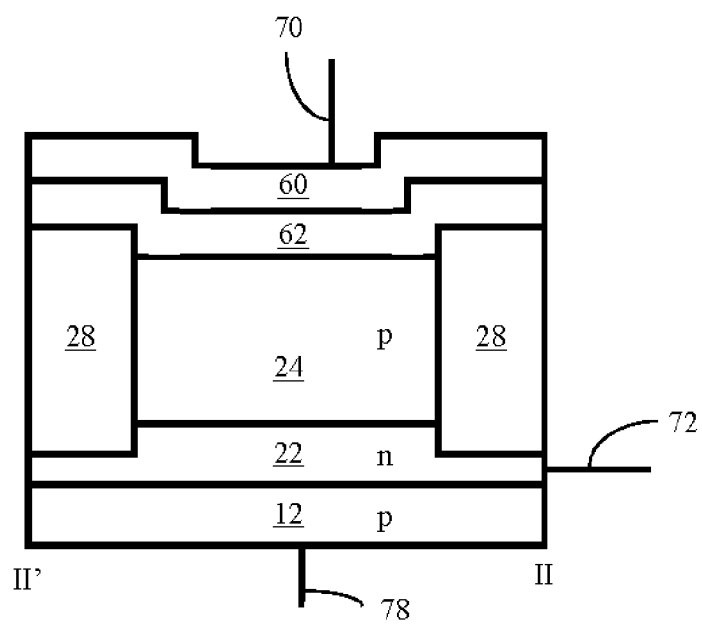


FIG. 53D

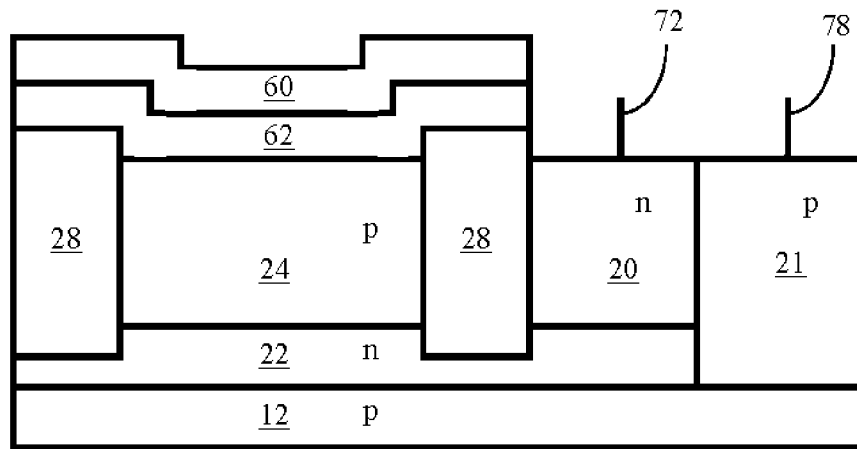


FIG. 53E

Exemplary Memory Array 380 with Representative
Memory Cells 350a, 350b, 350c and 350d

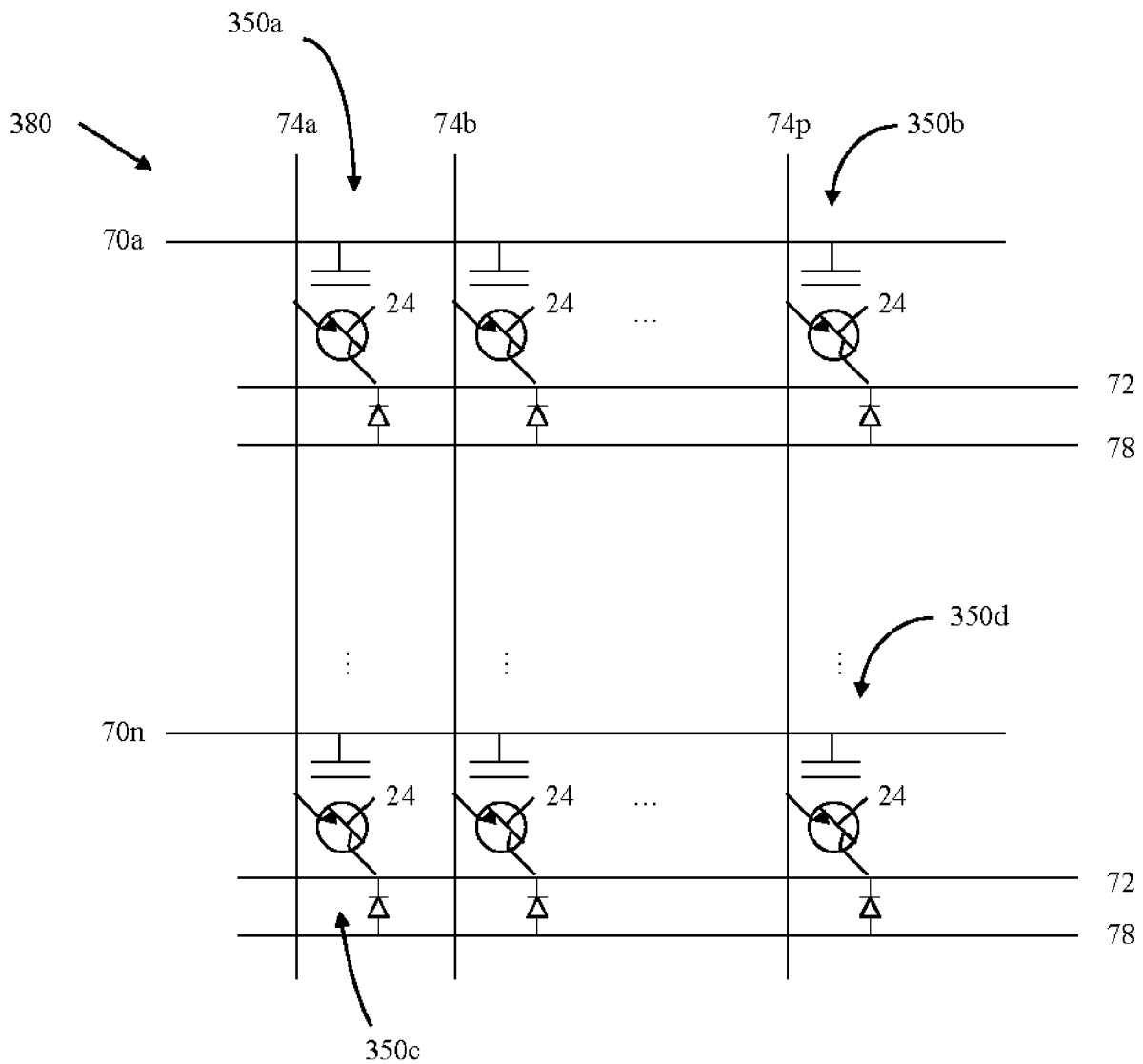


FIG. 54A

Array Hold Operation
(All Memory Cells 350)

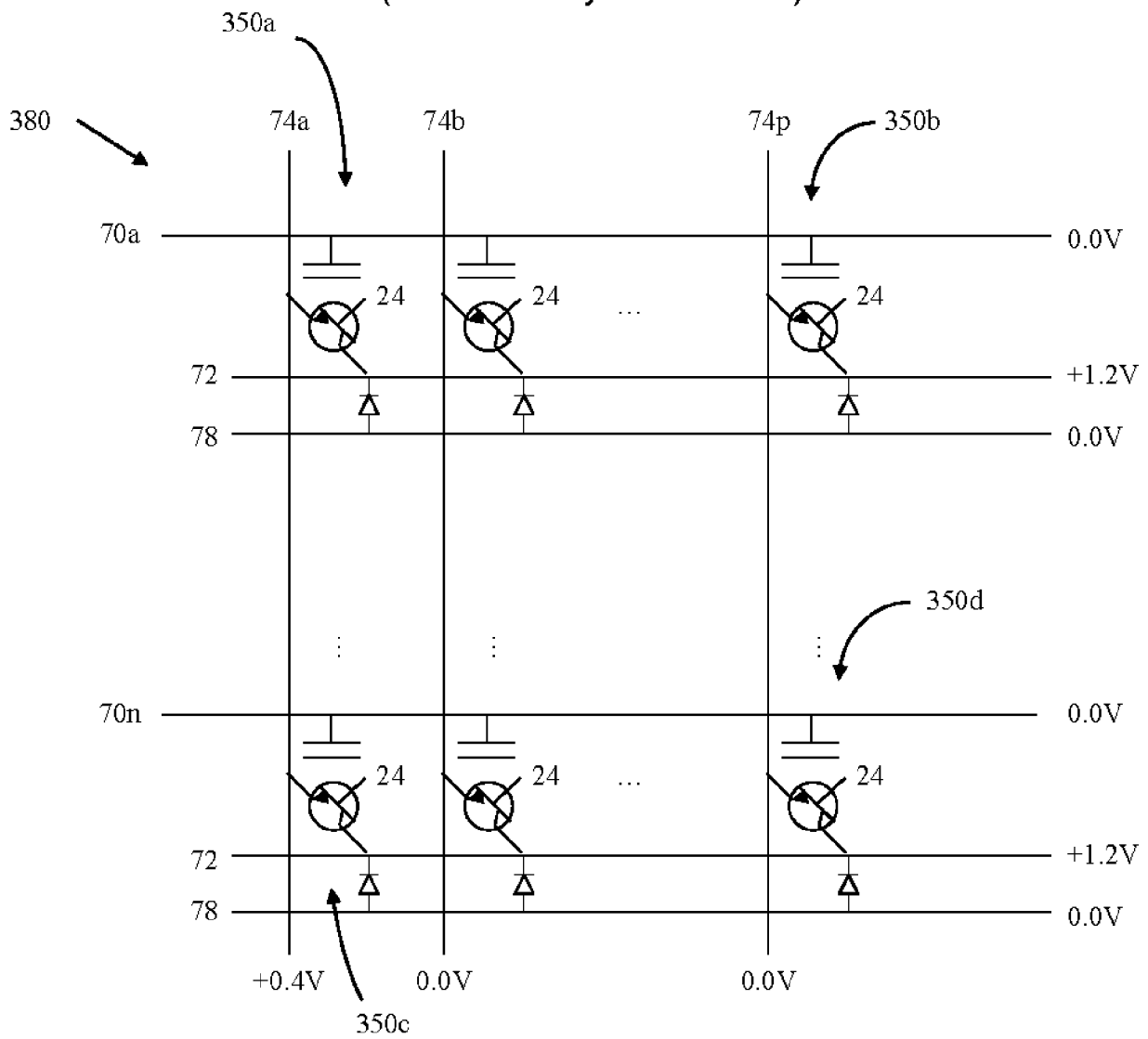


FIG. 54B

Read Operation (Single Memory Cell 350a)

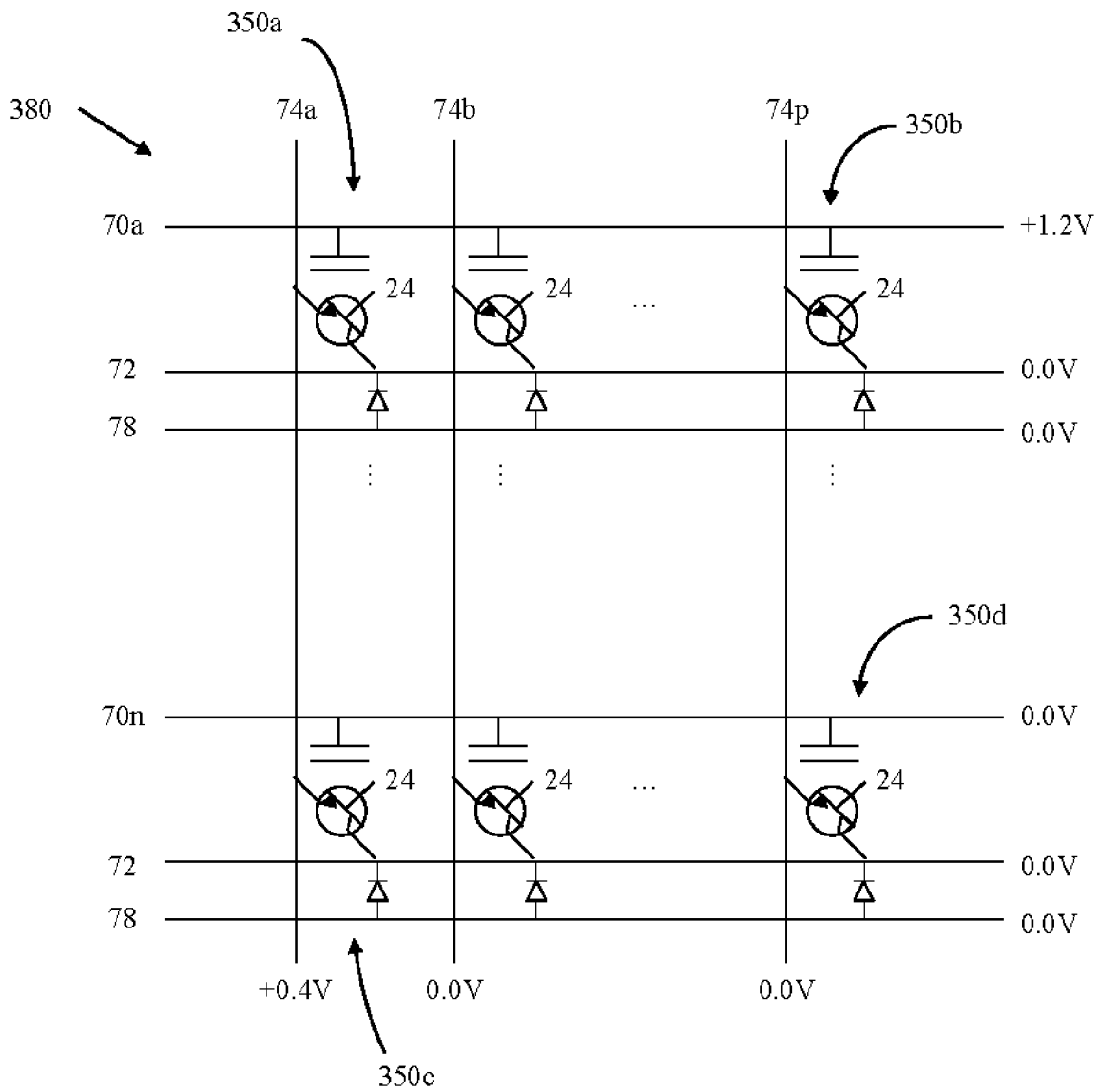


FIG. 54C

Array Write Logic-0 Operation
(All Memory Cells 350)

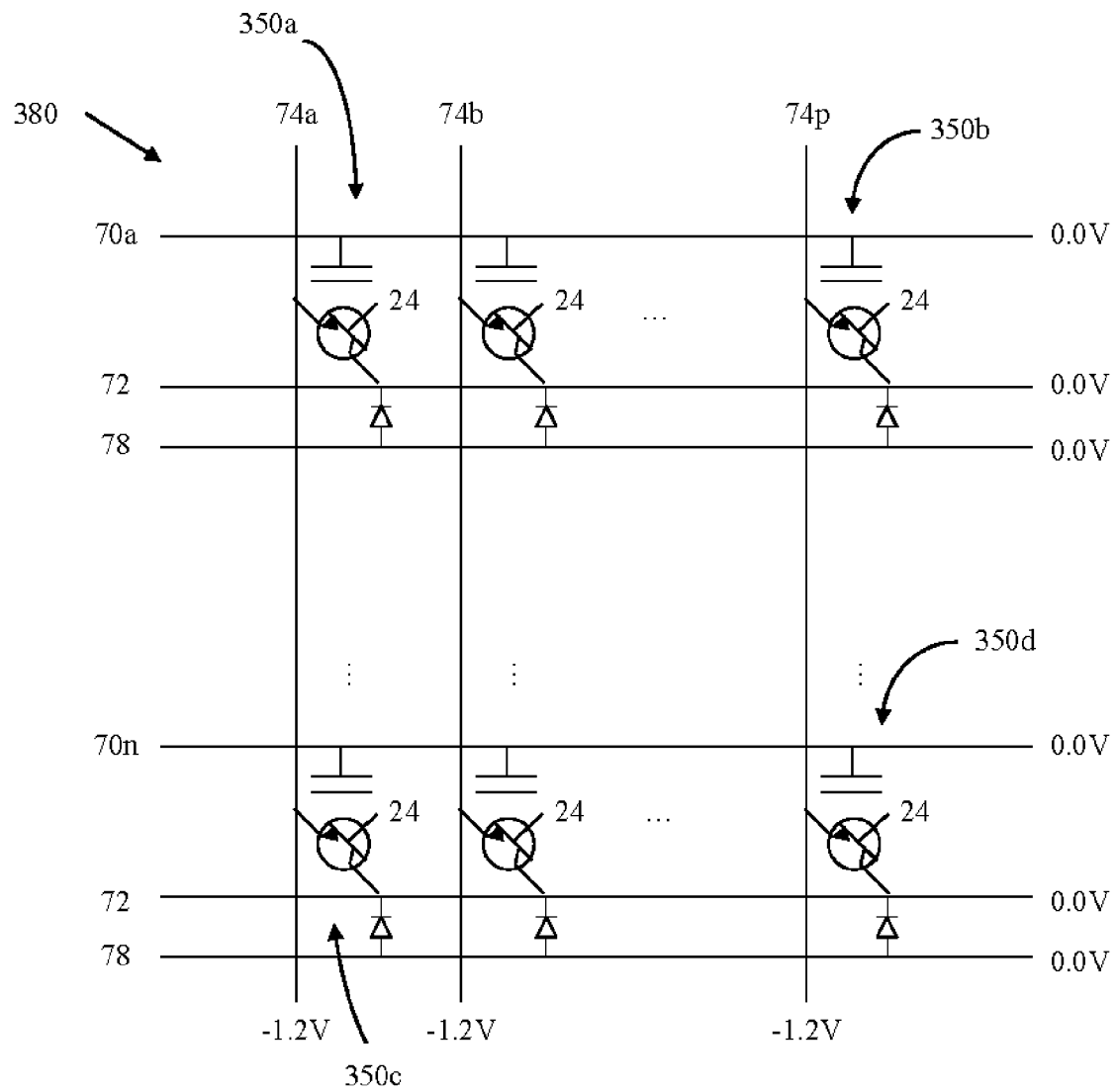


FIG. 54D

Column Write Logic-0 Operation (Memory Cells 350a and 350c)

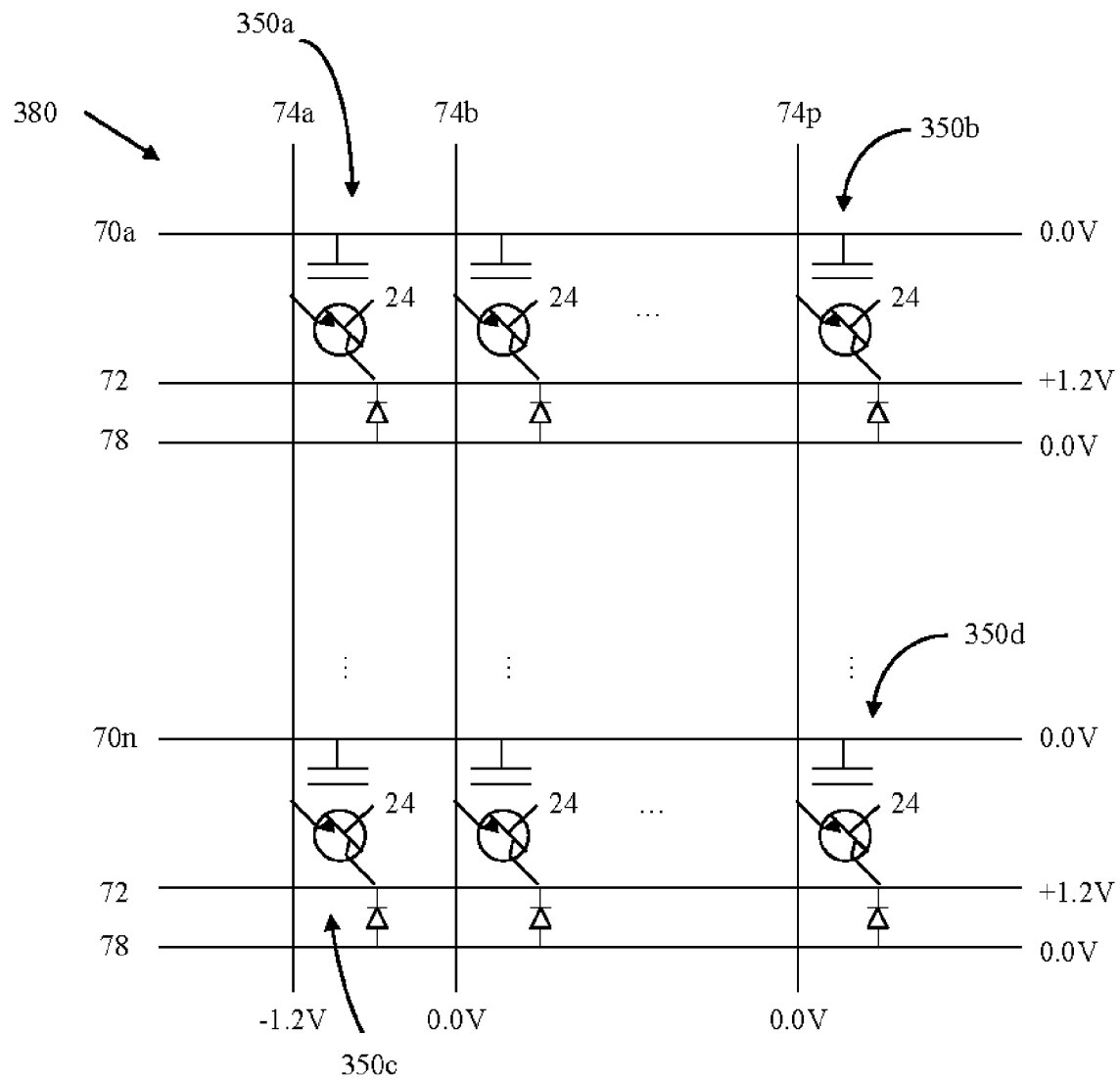


FIG. 54E

Write Logic-0 Operation
(Single Memory Cell 350a)

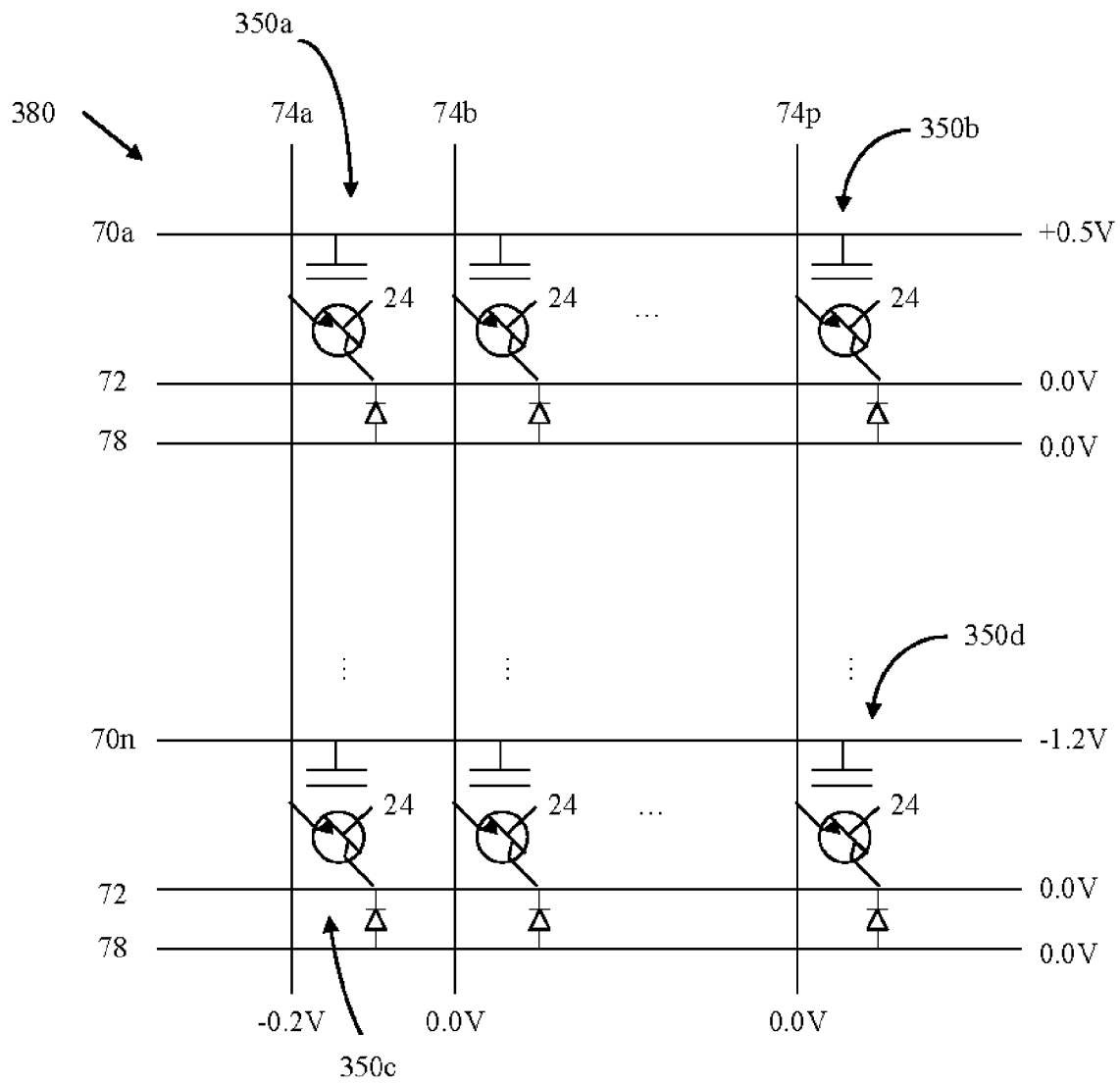


FIG. 54F

Write Logic-1 Operation – GIDL
(Single Memory Cell 350a)

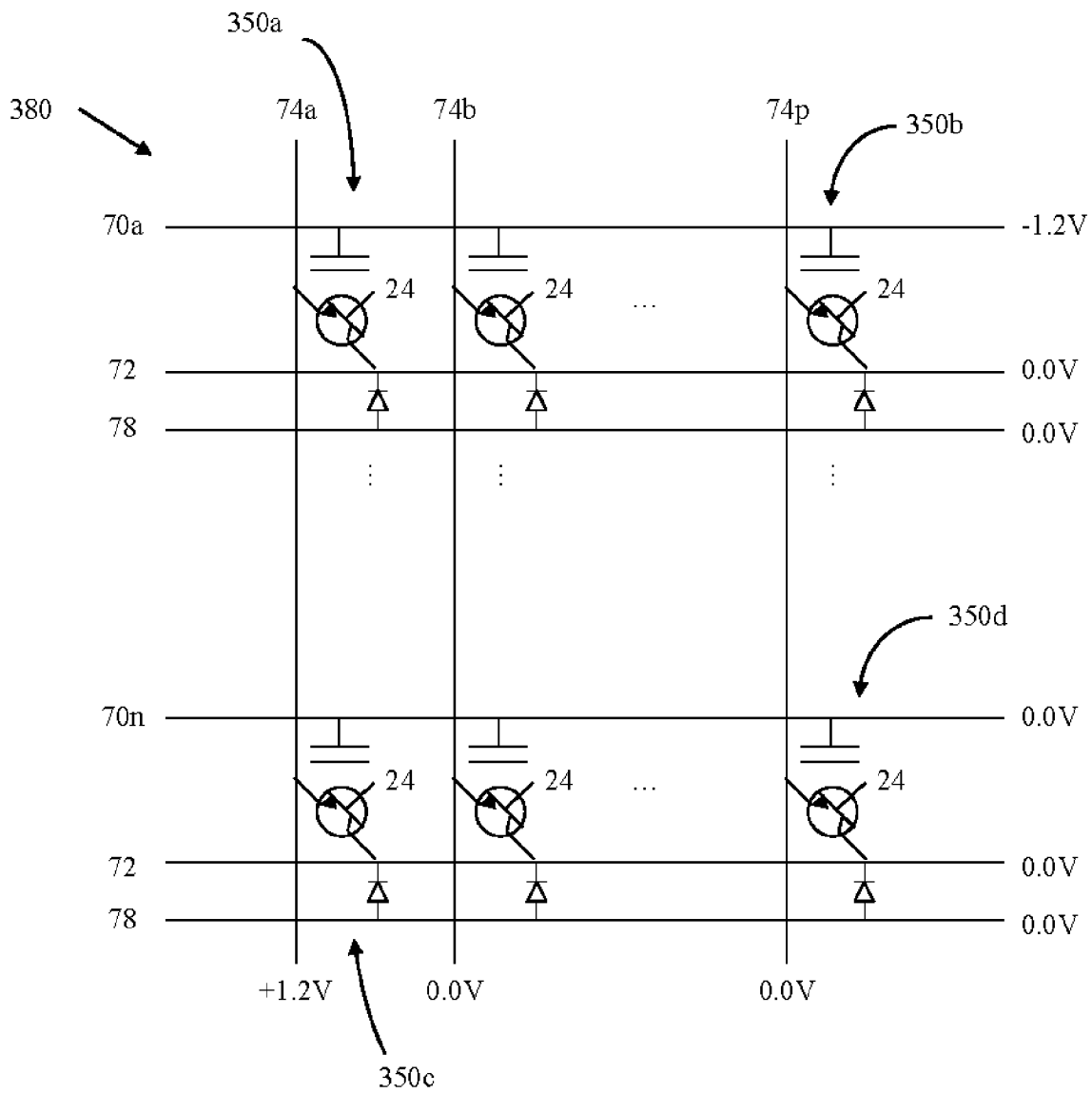


FIG. 54G

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 350a)

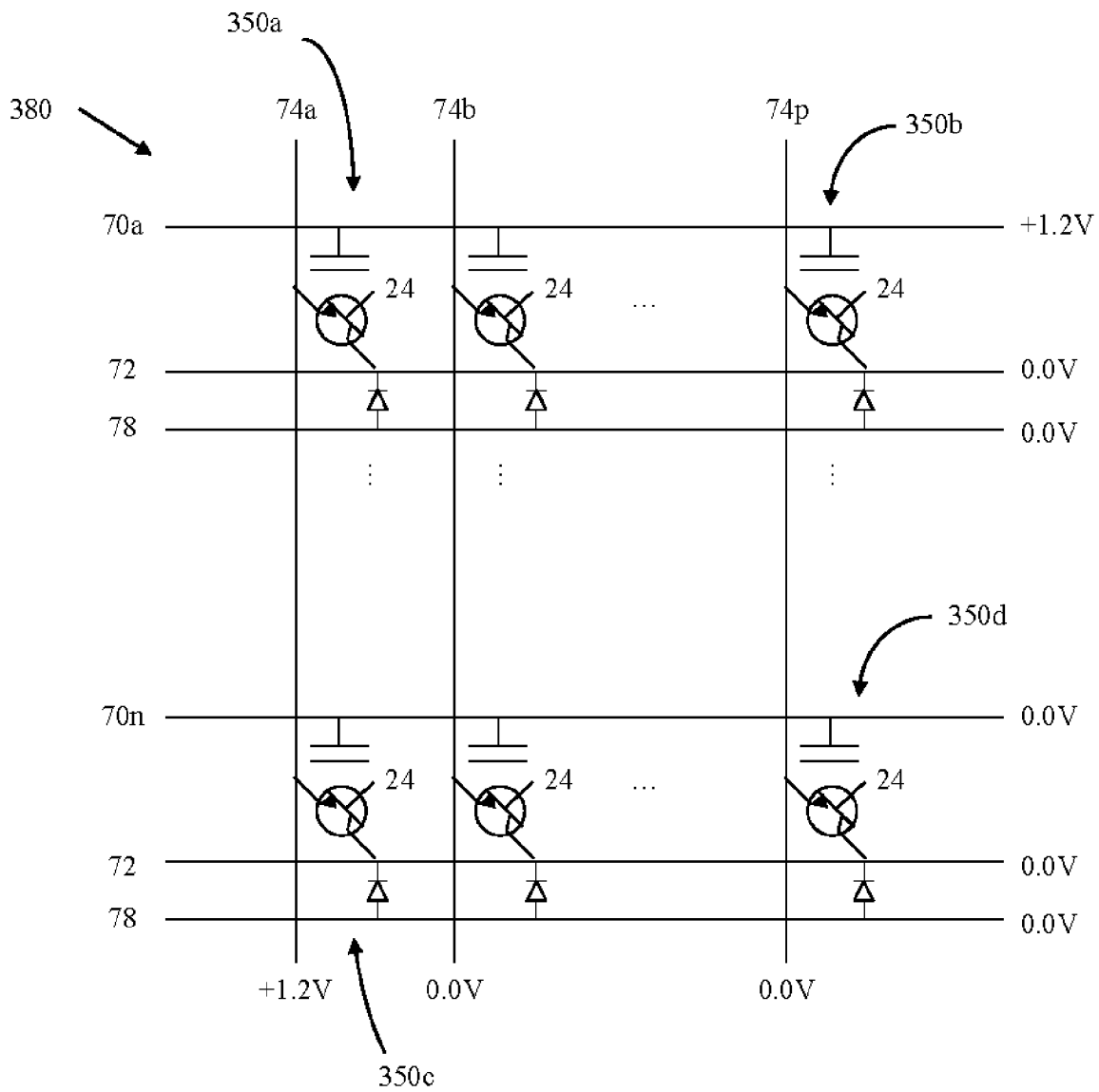


FIG. 54H

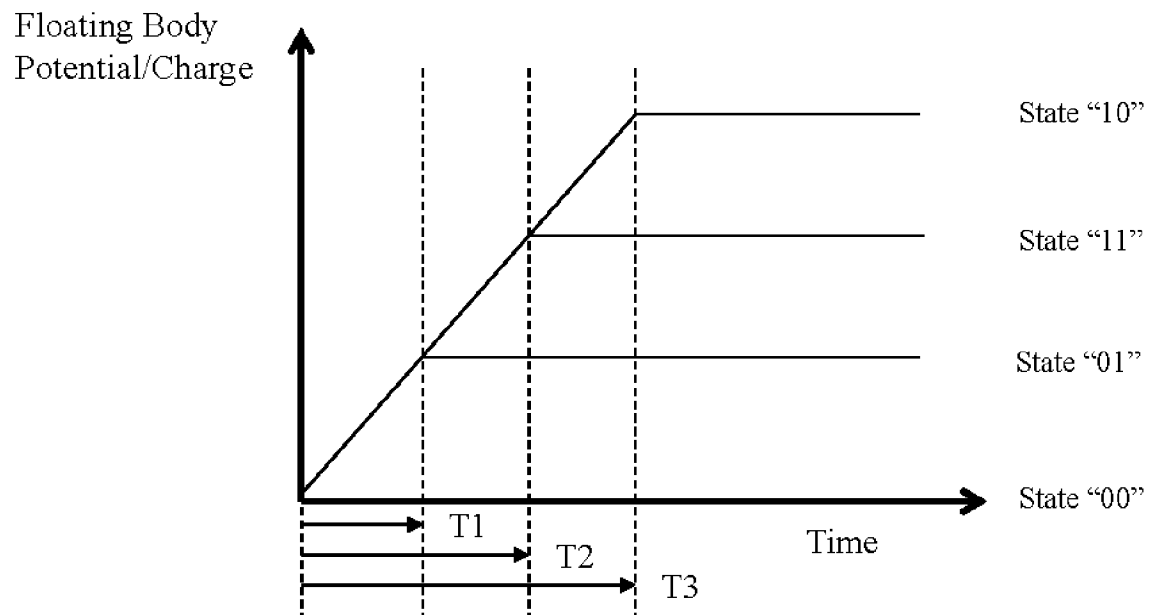


FIG. 55A

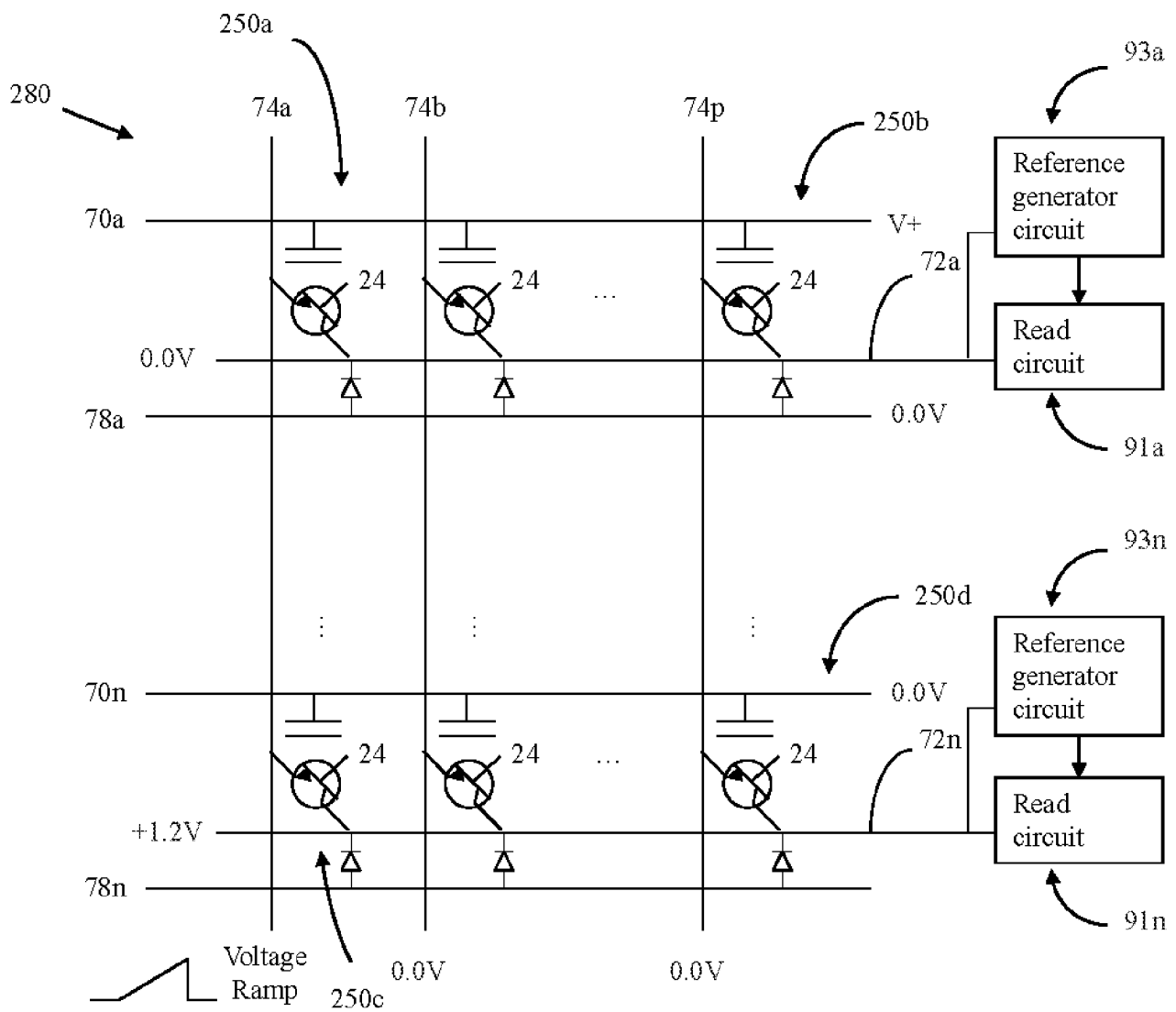


FIG. 55B

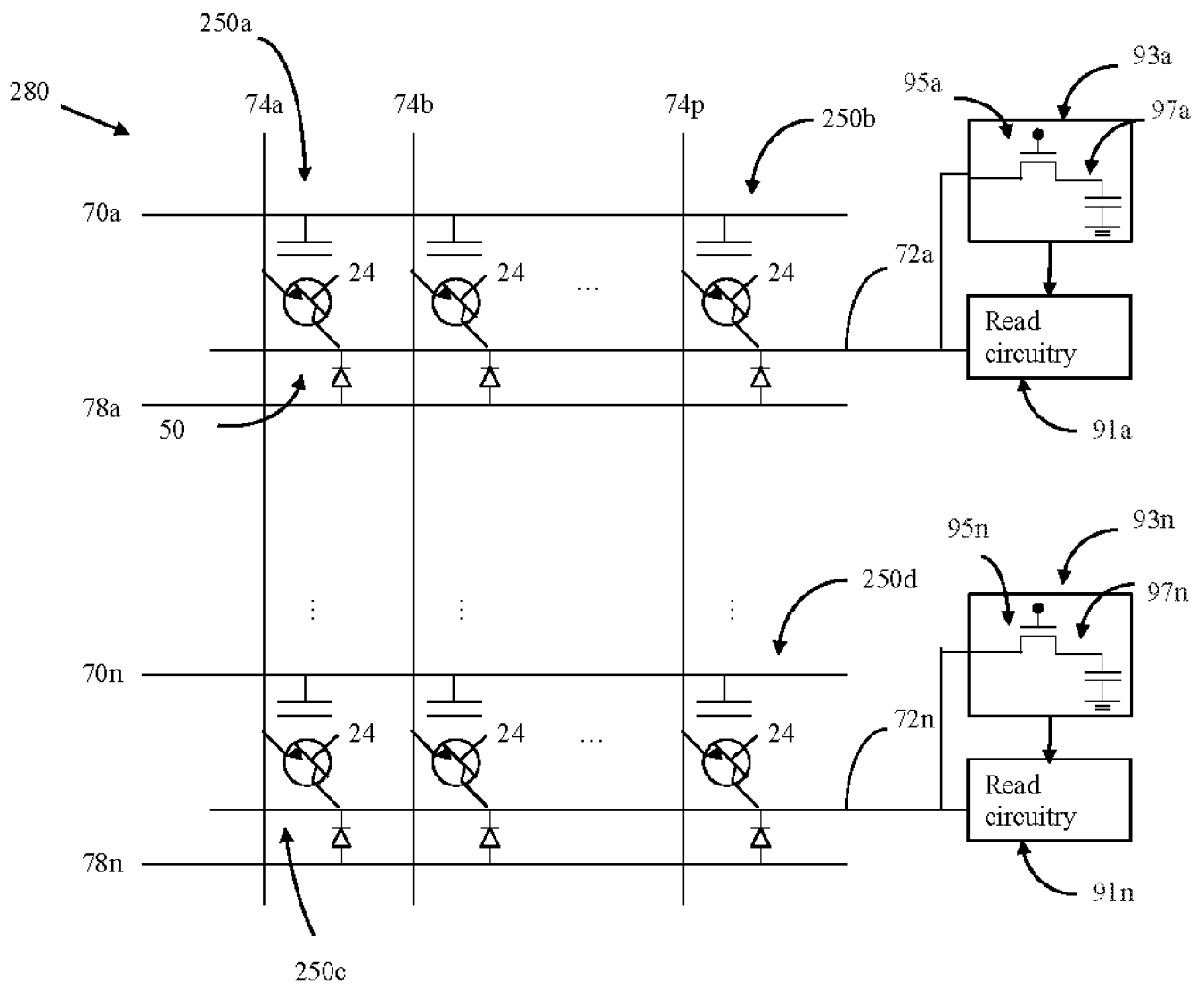


FIG. 55C

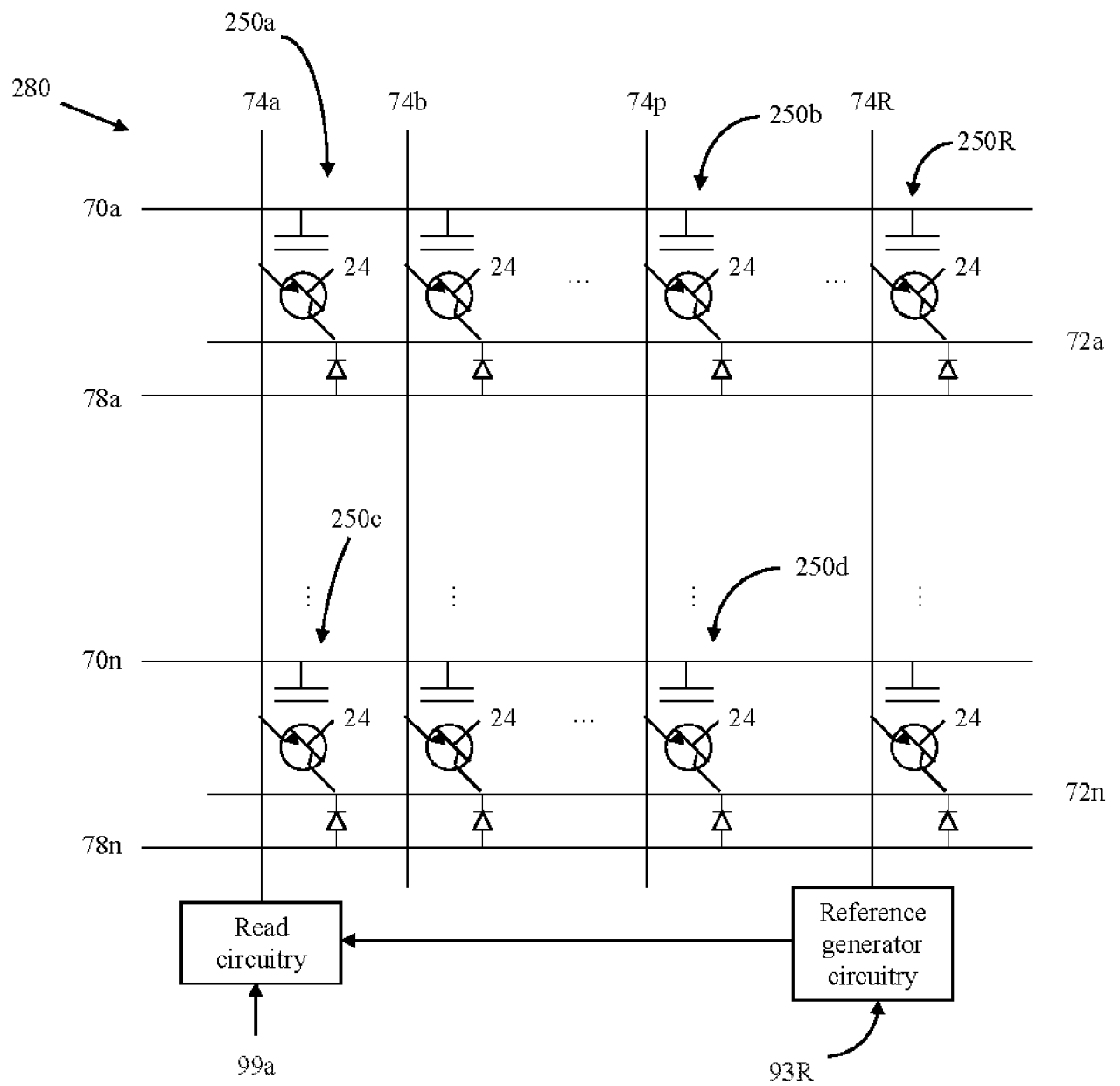


FIG. 55E

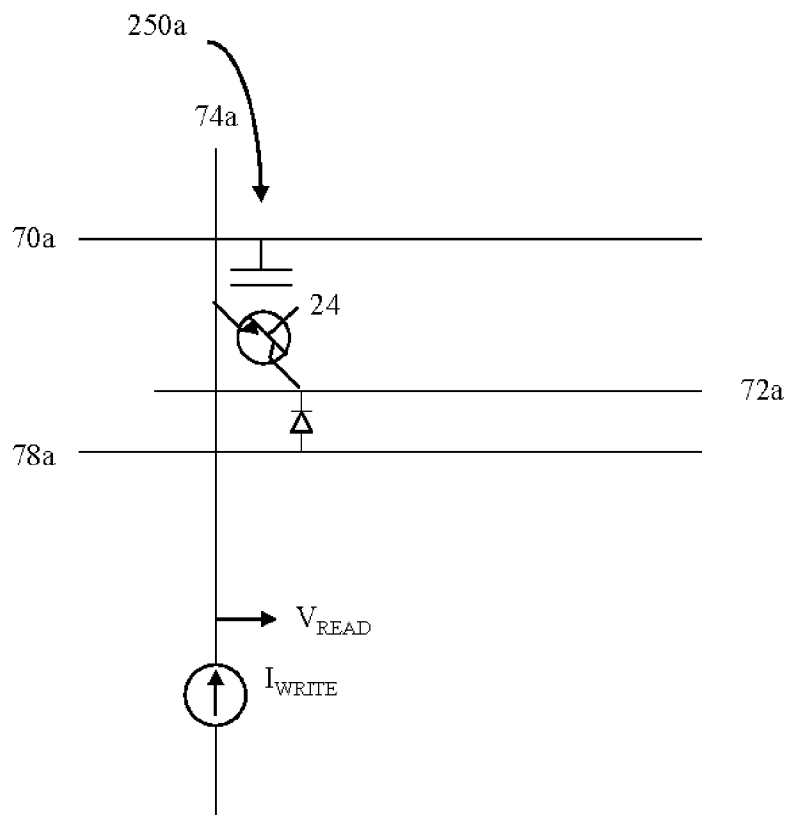


FIG. 55F

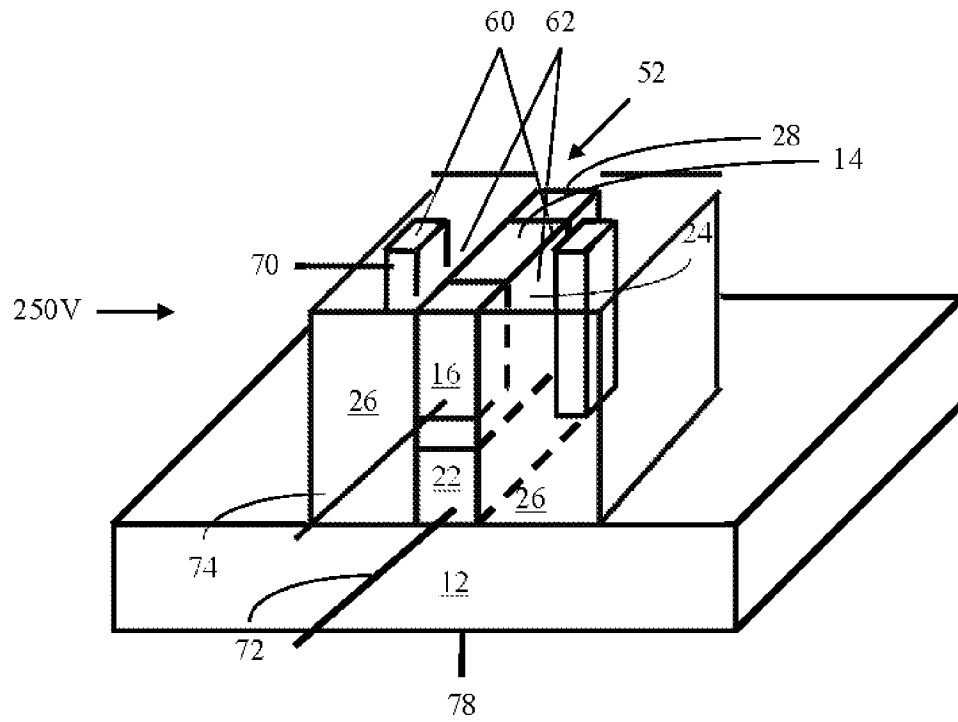


FIG. 56

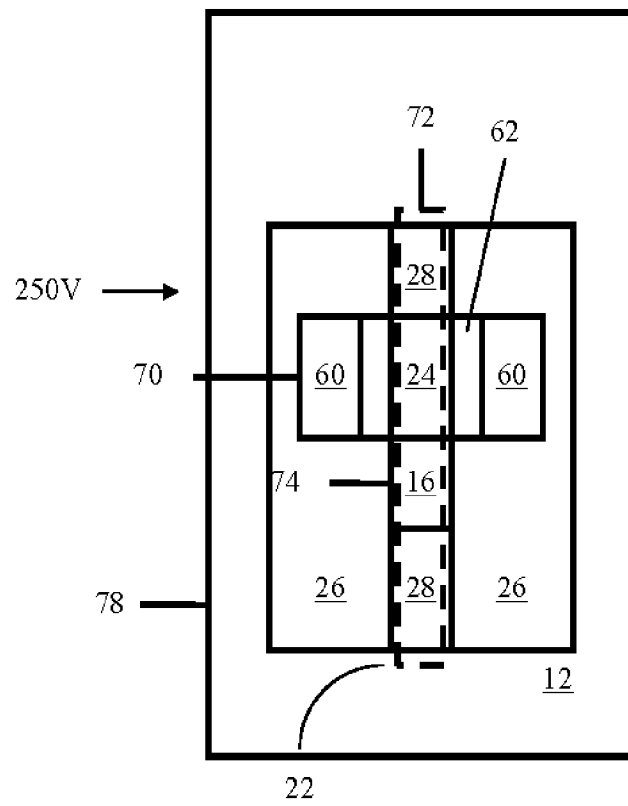


FIG. 57

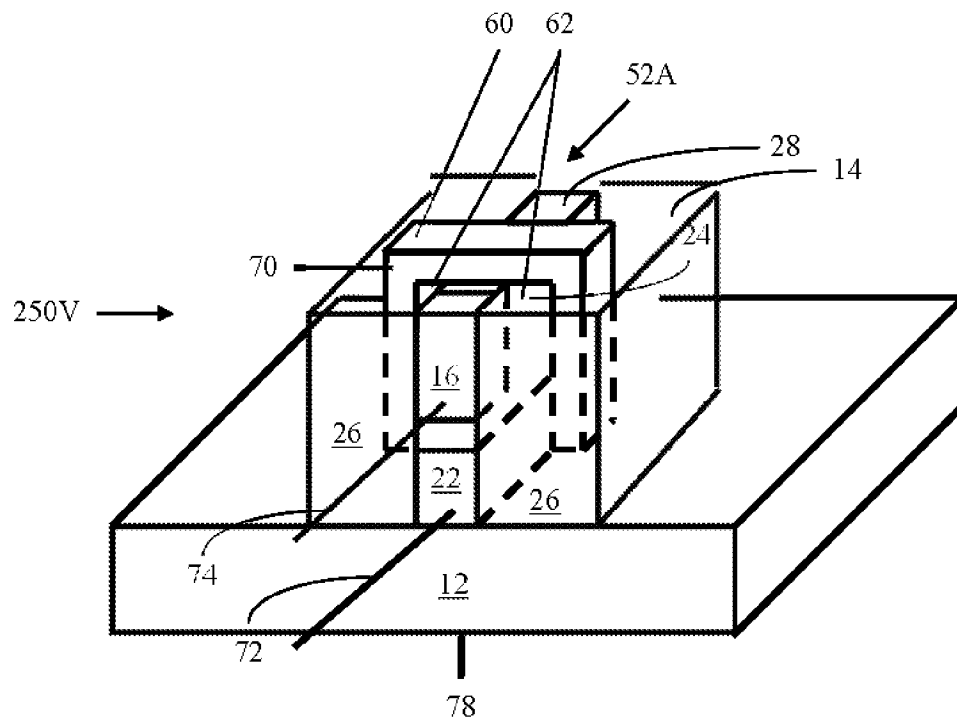


FIG. 58A

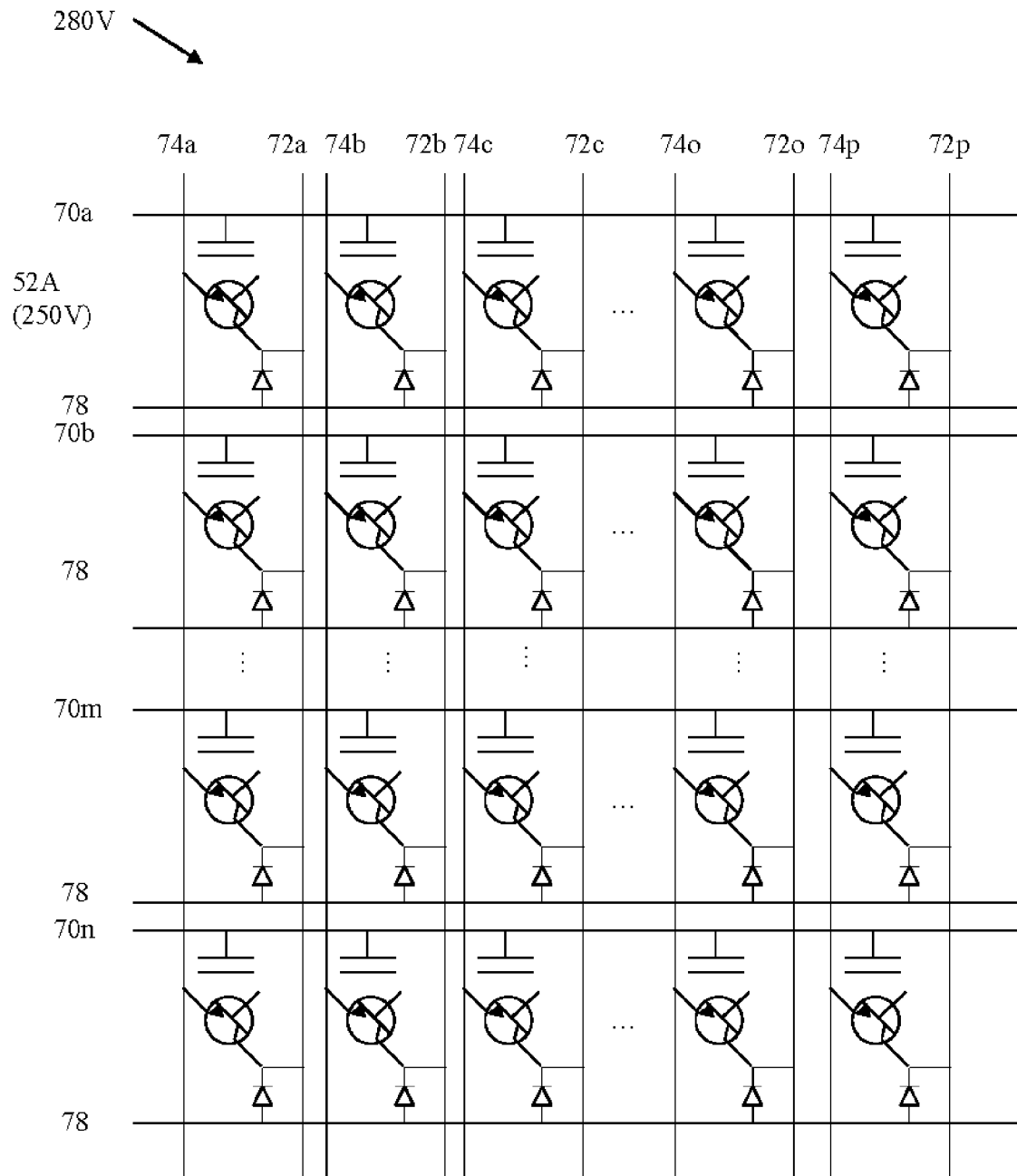


FIG. 58B

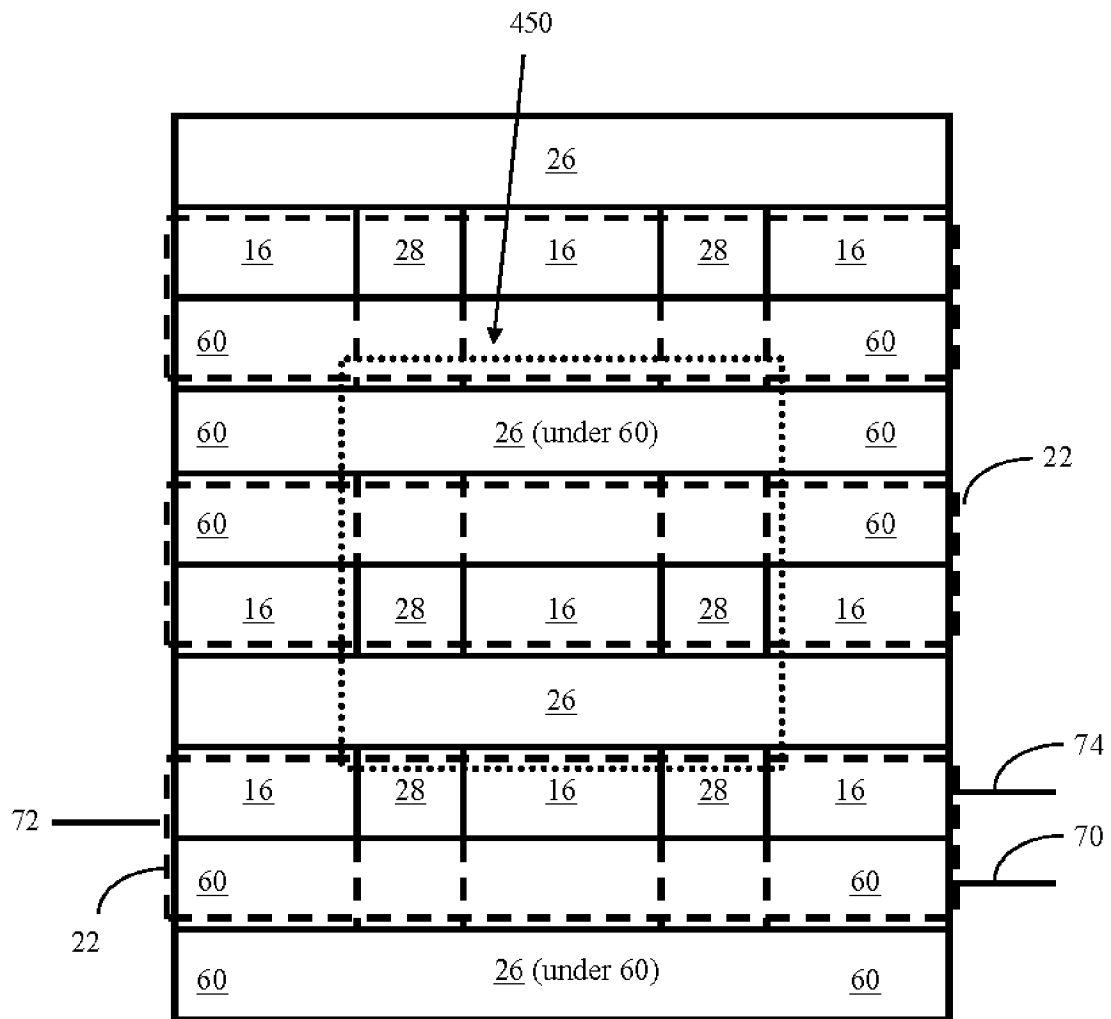


FIG. 59A

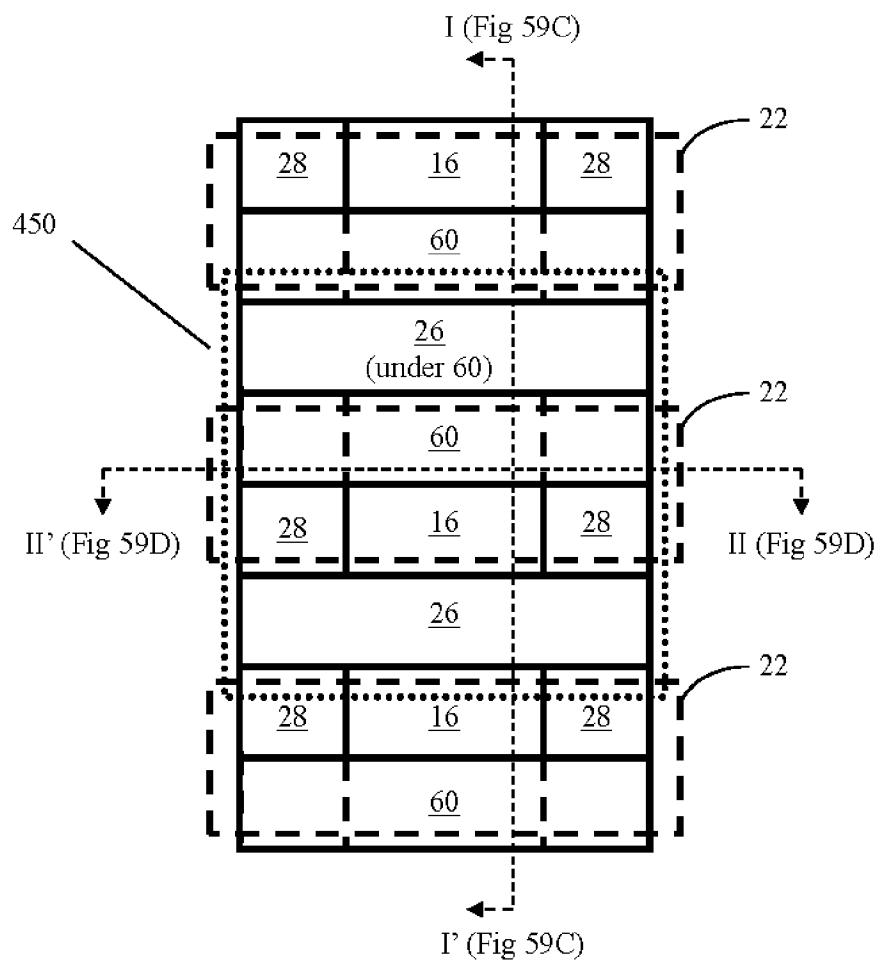


FIG. 59B

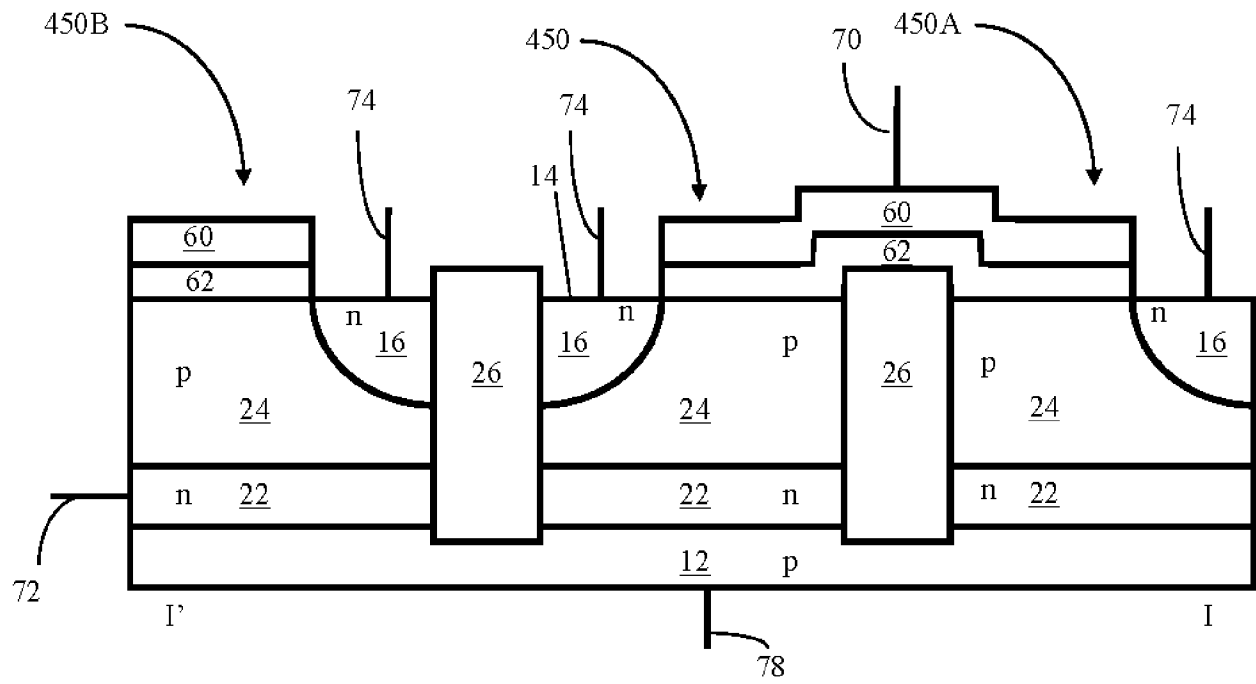


FIG. 59C

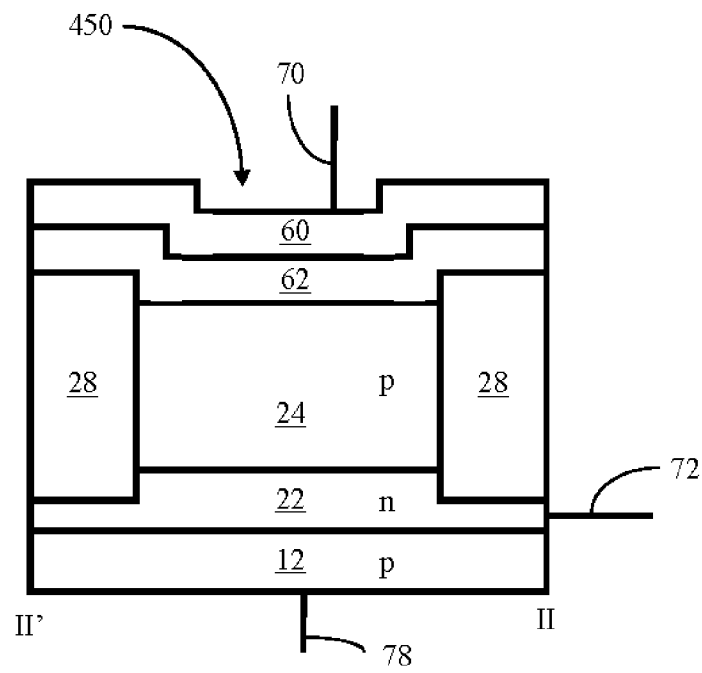


FIG. 59D

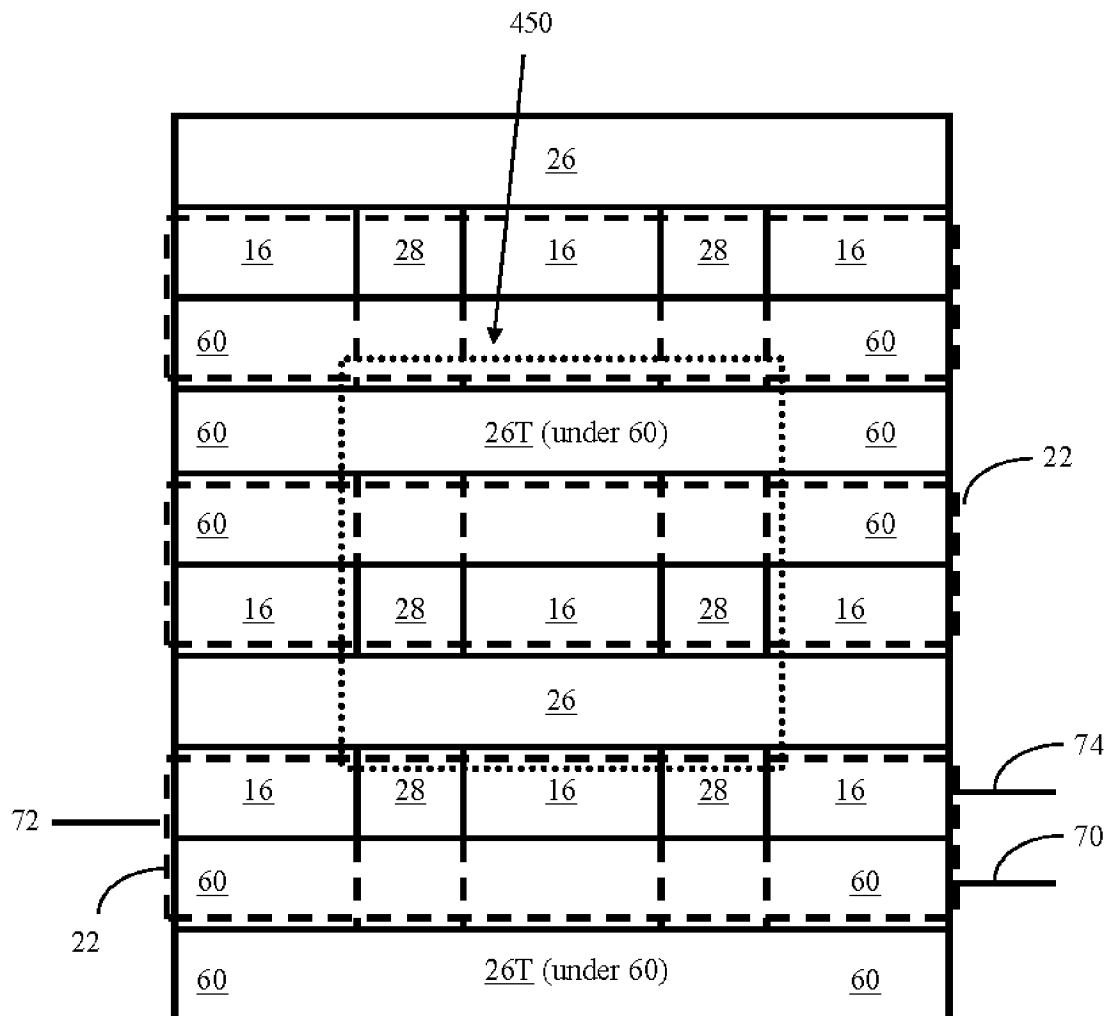


FIG. 60A

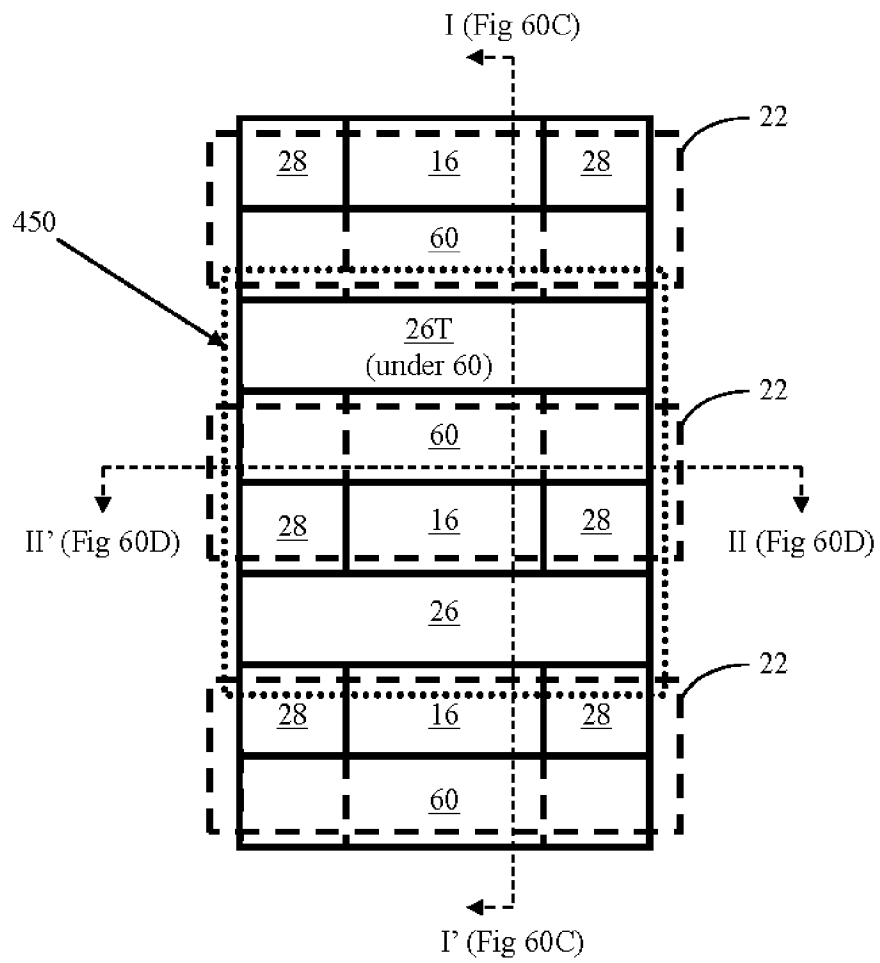


FIG. 60B

[illegible]

FIG. 60F

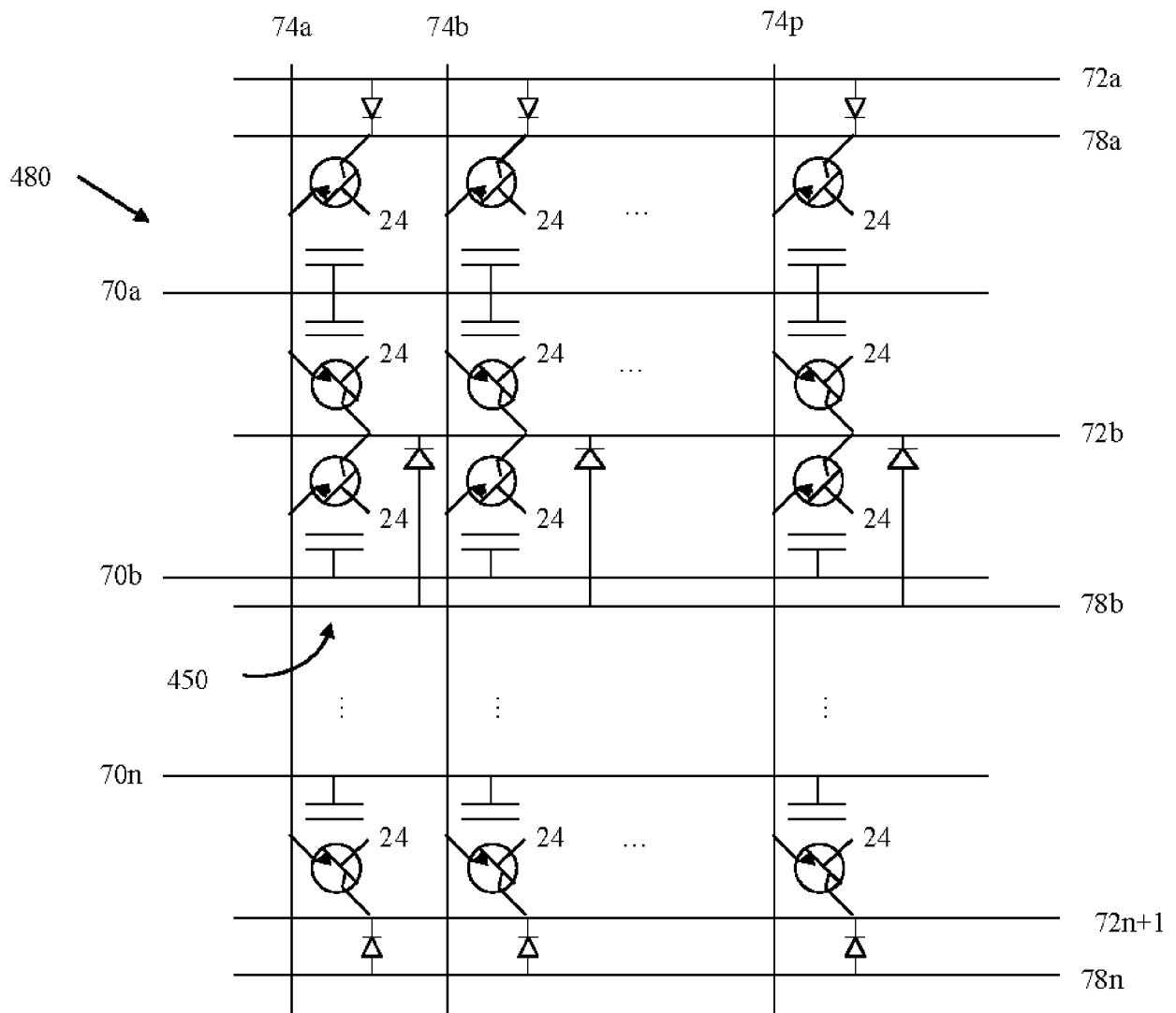


FIG. 61A

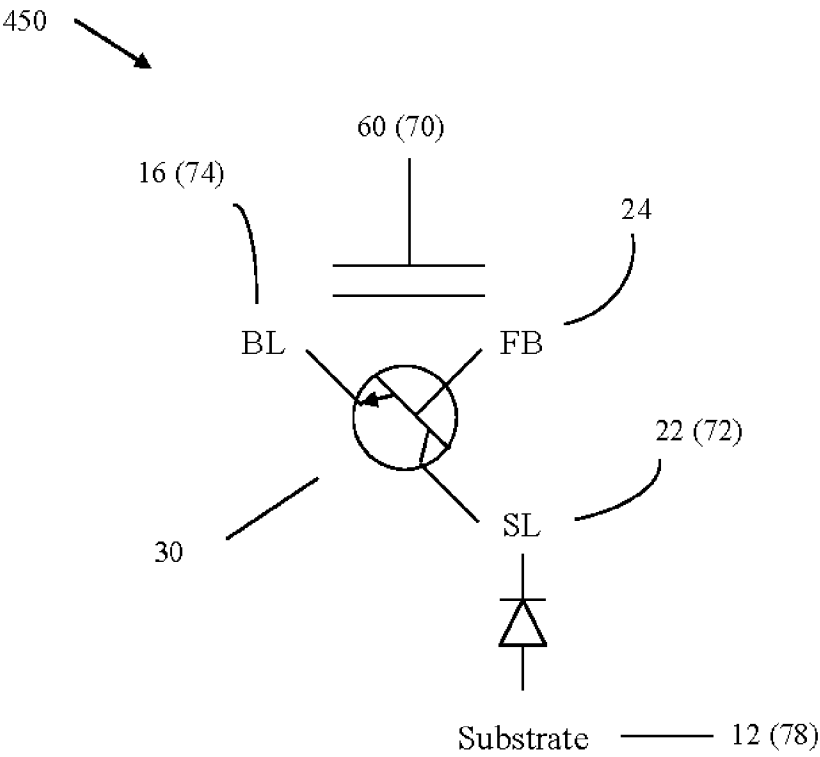


FIG. 61B

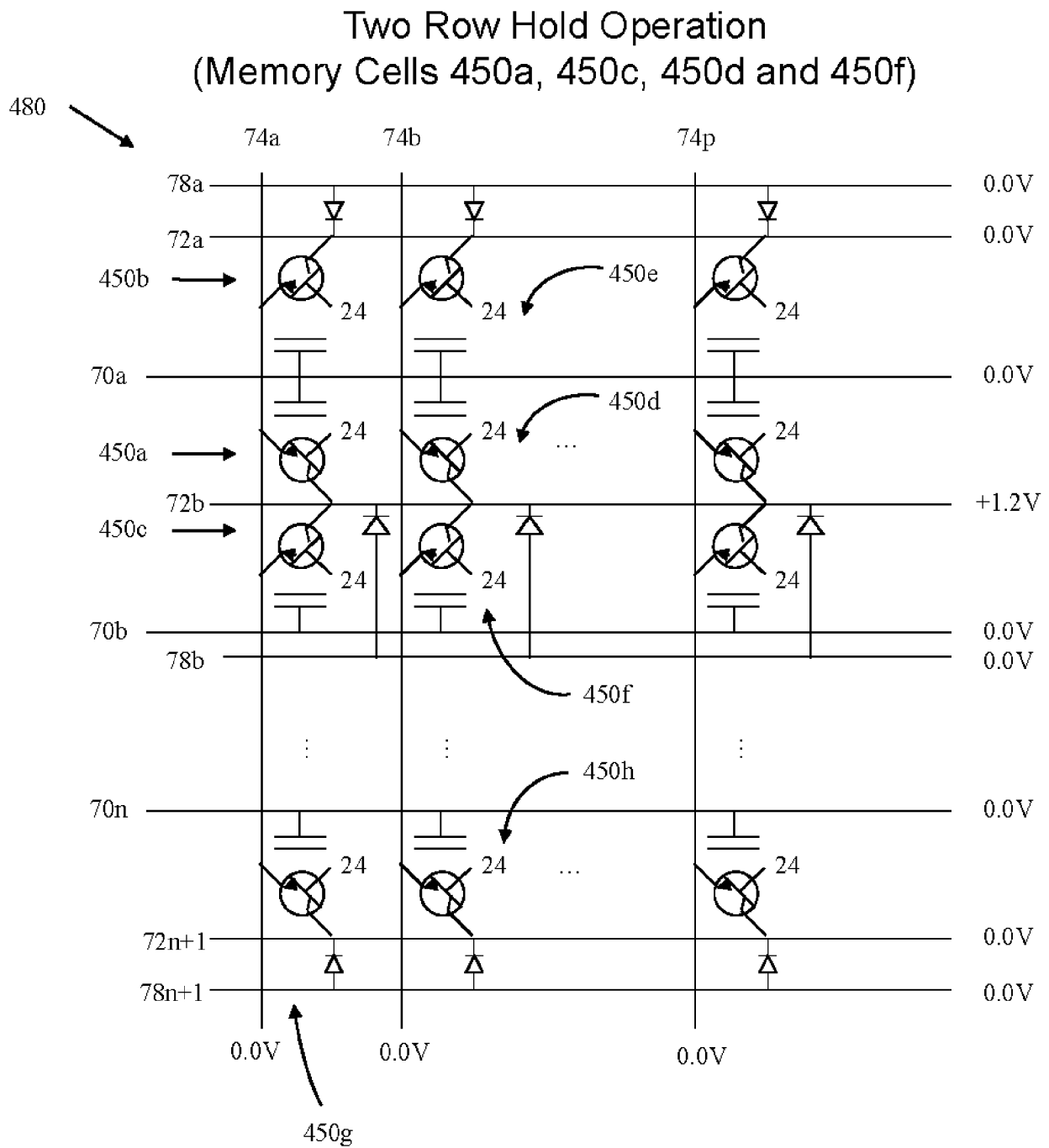


FIG. 62

Read Operation (Single Memory Cell 450a)

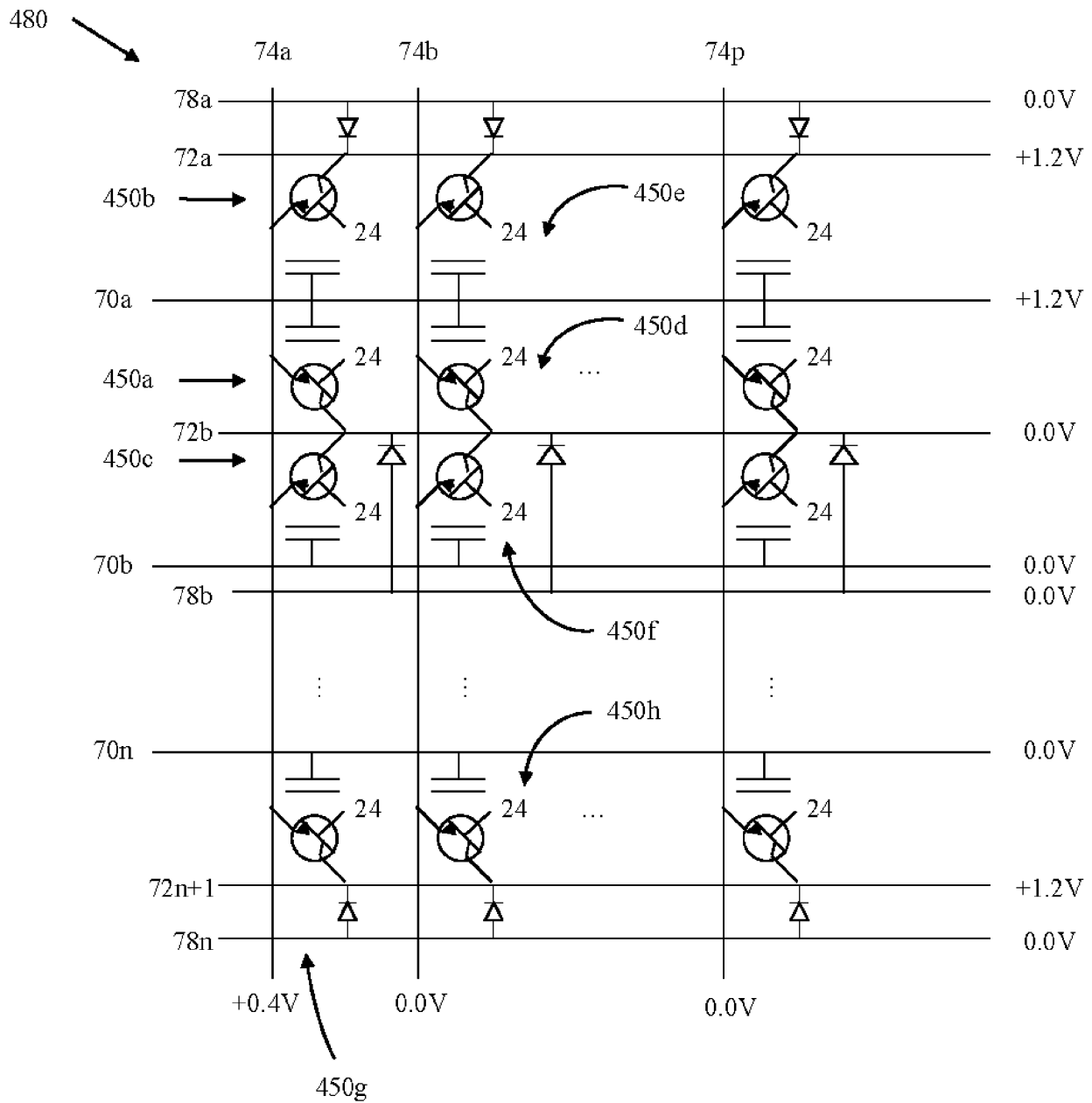


FIG. 63

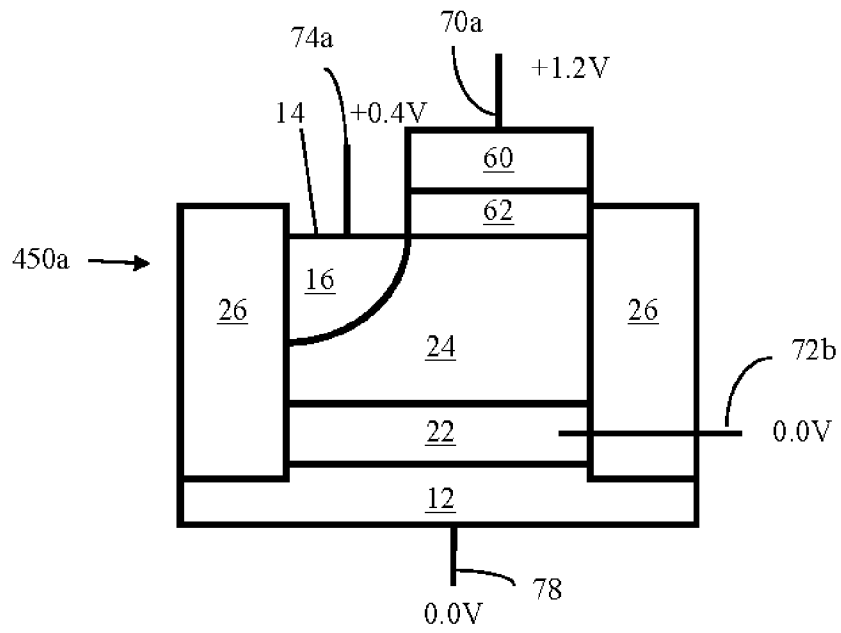


FIG. 64A

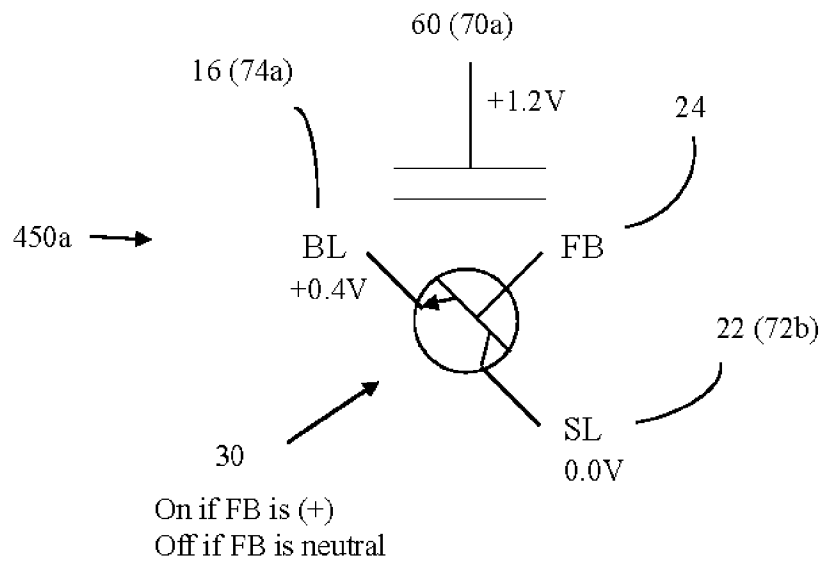


FIG. 64B

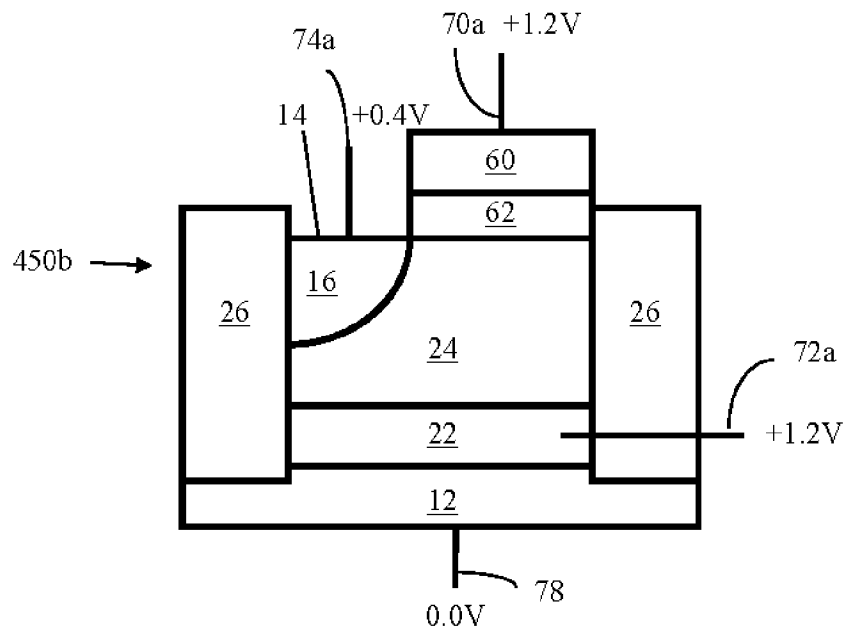


FIG. 64C

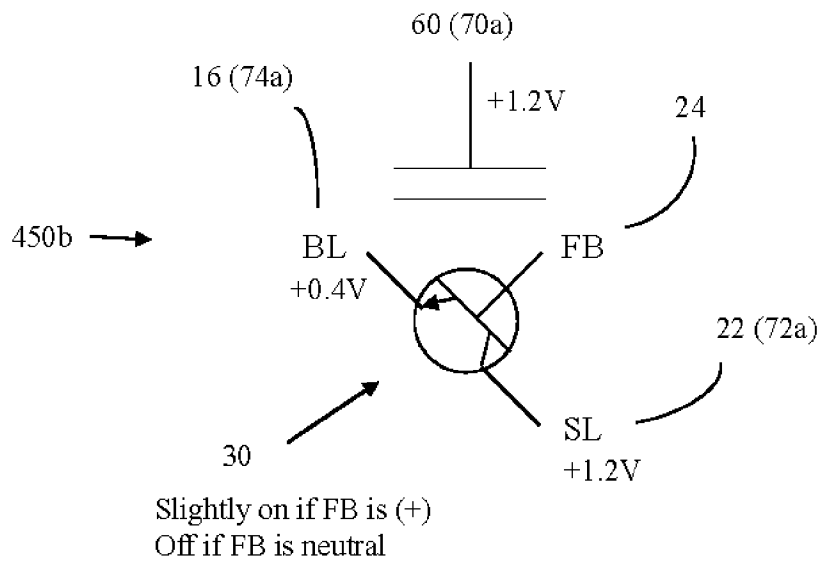


FIG. 64D

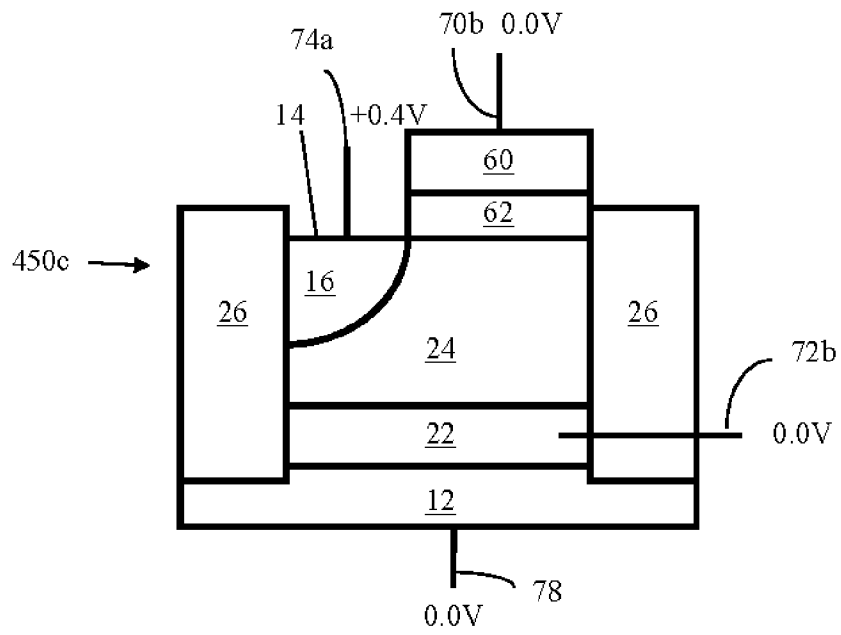


FIG. 64E

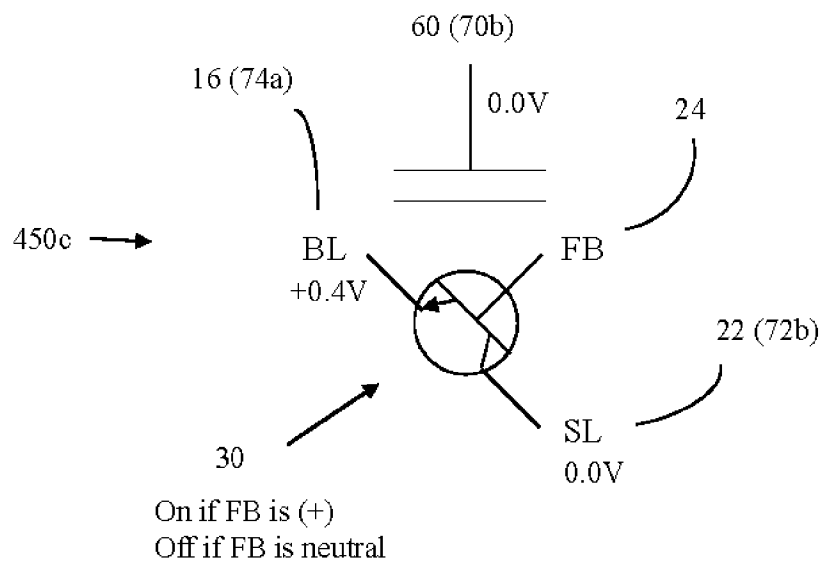


FIG. 64F

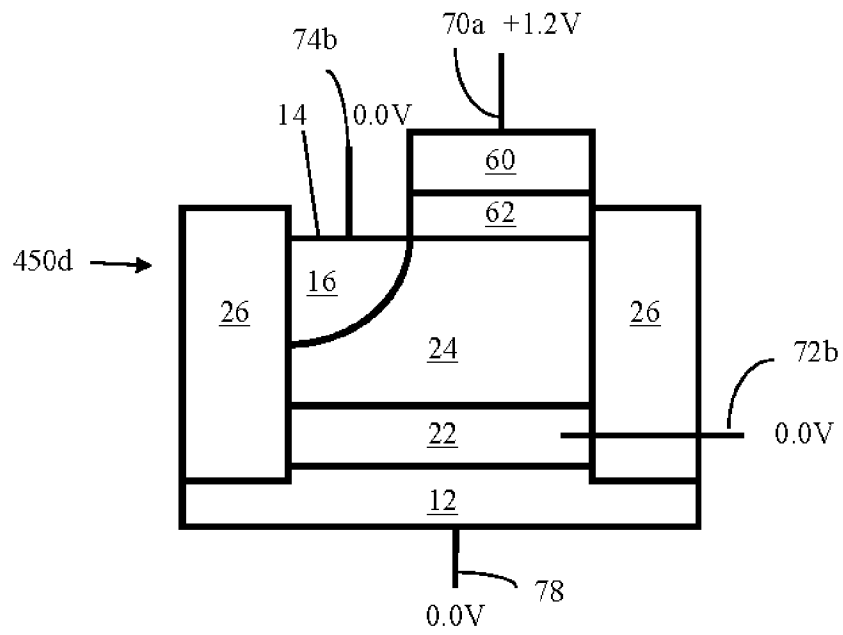


FIG. 64G

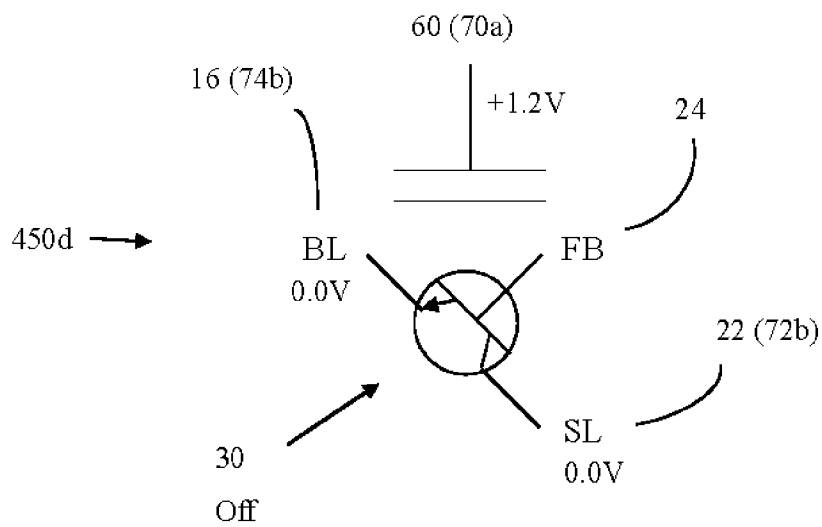


FIG. 64H

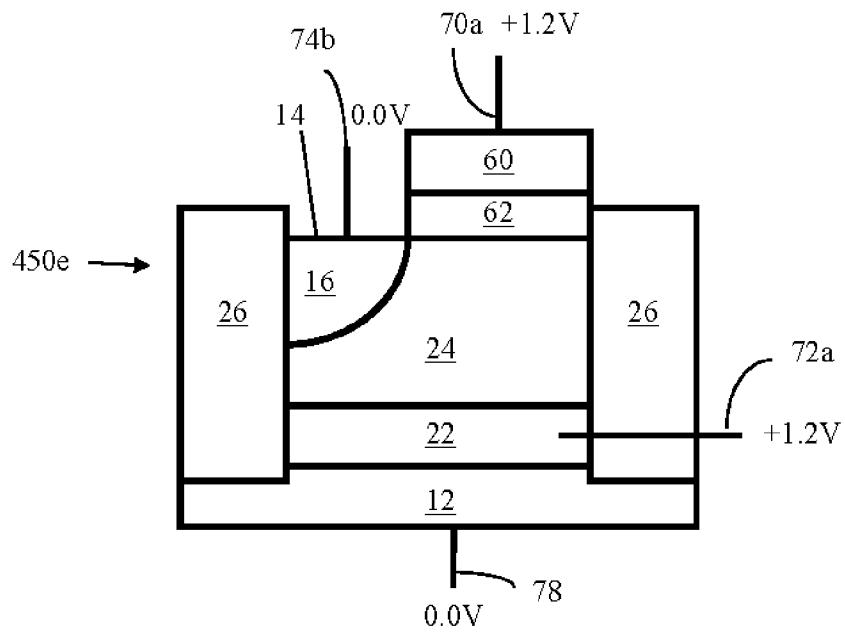


FIG. 64I

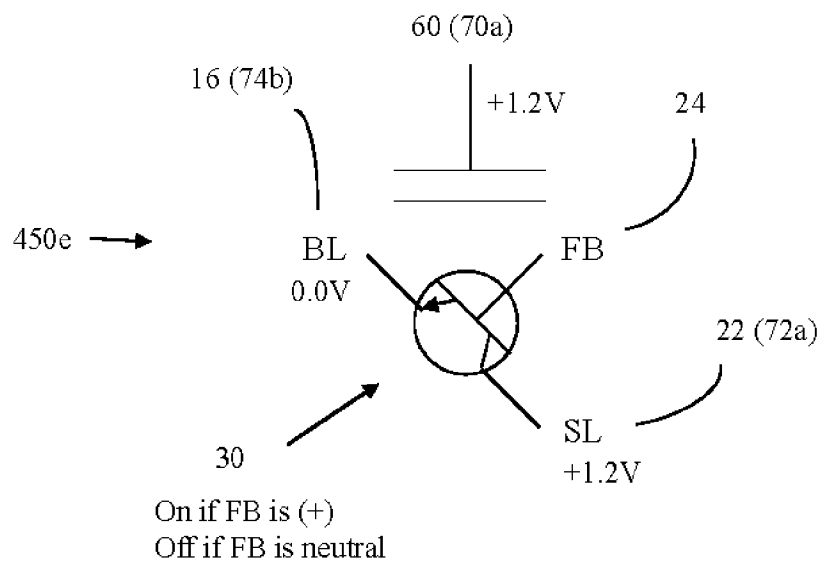


FIG. 64J

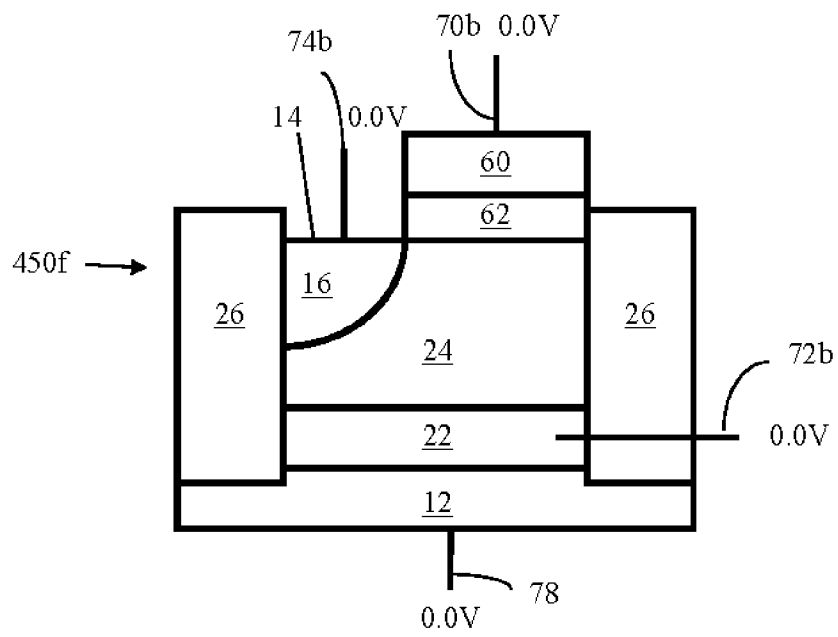


FIG. 64K

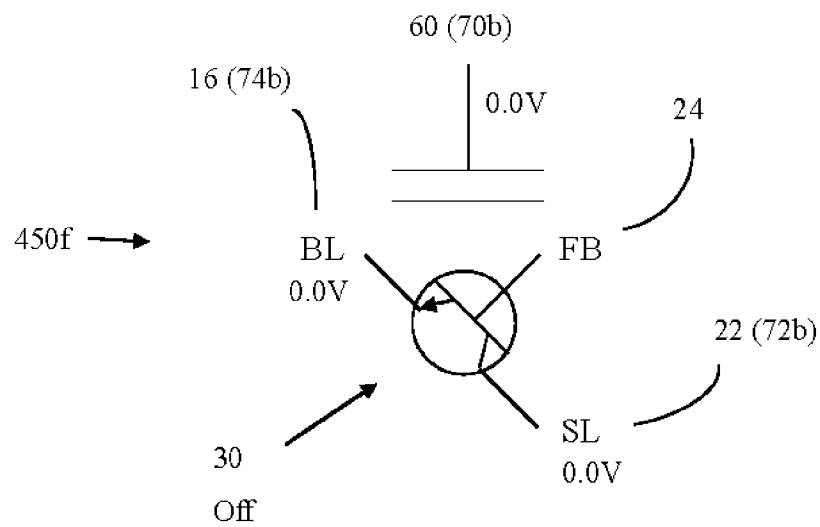


FIG. 64L

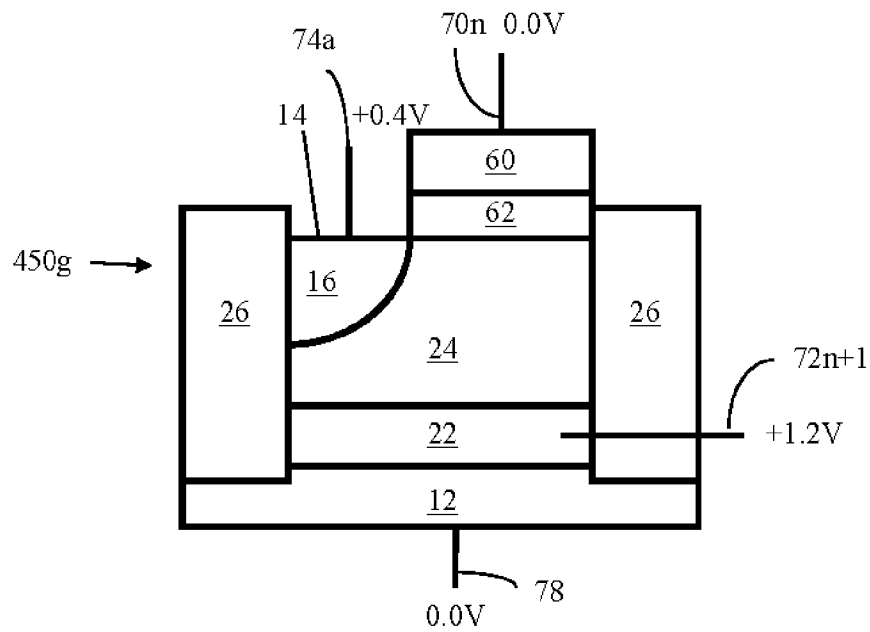


FIG. 64M

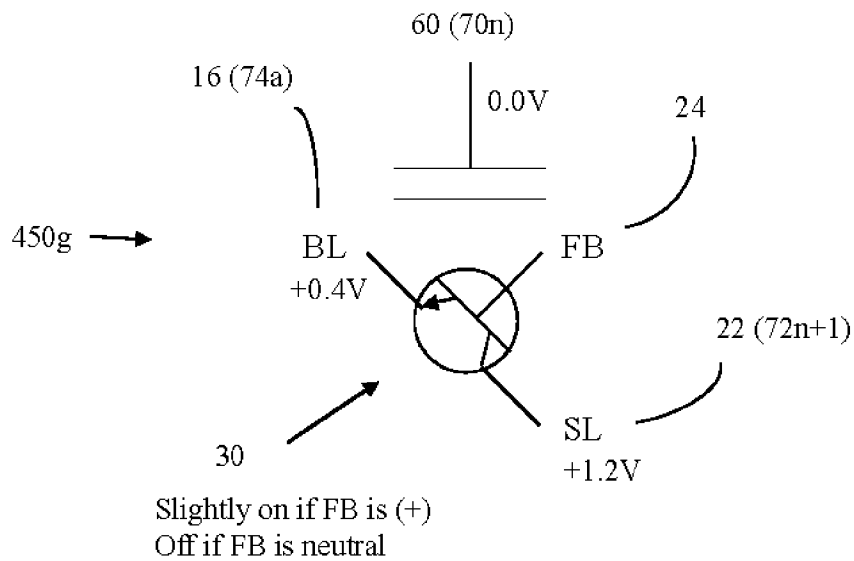


FIG. 64N

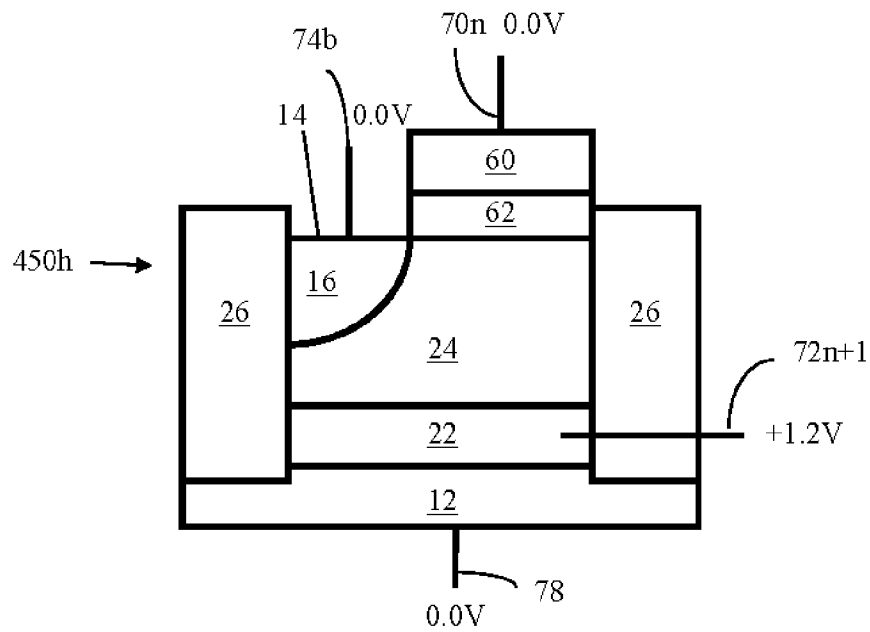


FIG. 64O

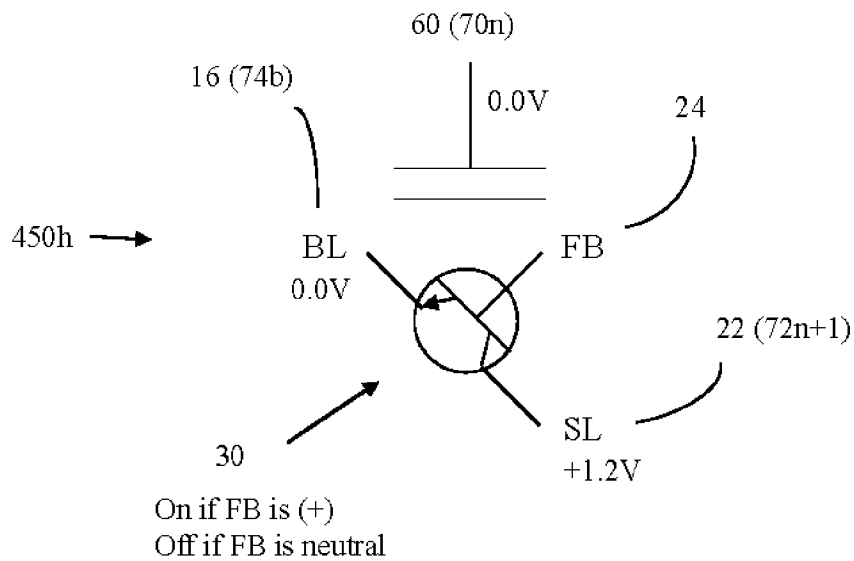


FIG. 64P

Two Row Write Logic-0 Operation (Memory Cells 450a, 450c, 450d and 450f)

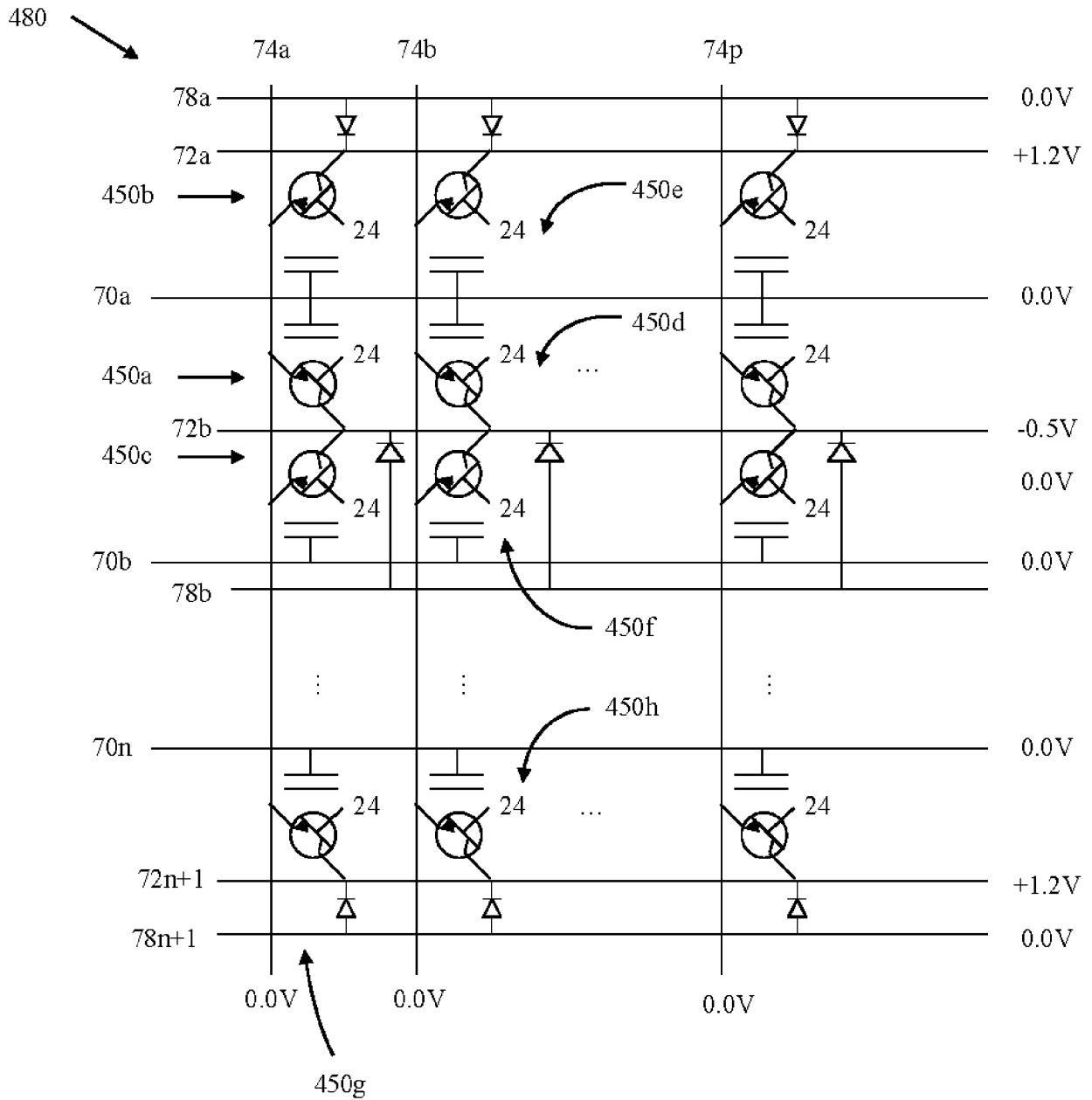


FIG. 65

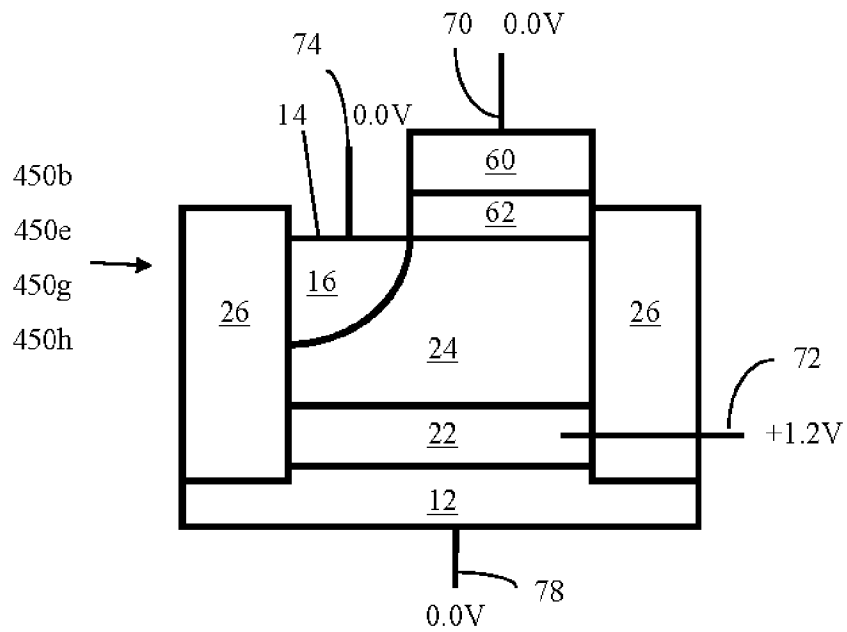


FIG. 66A

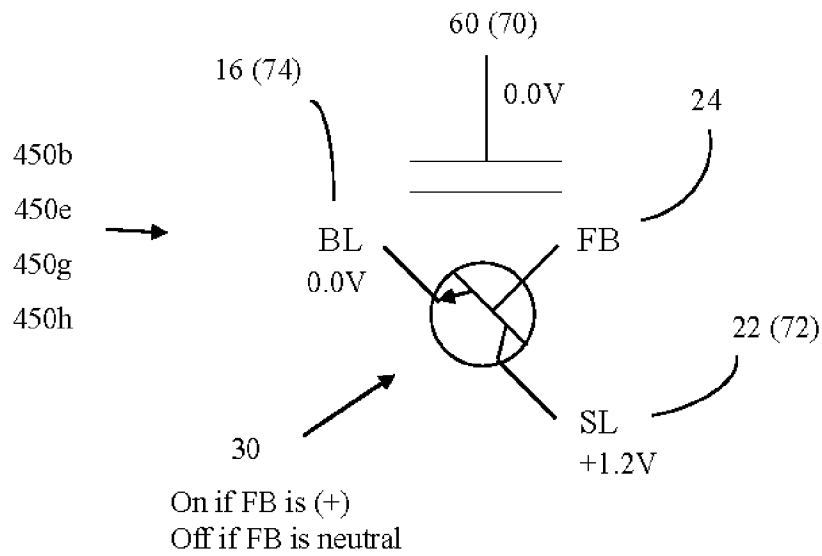


FIG. 66B

Single Column Write Logic-0 Operation (Memory Cells 450a, 450b, 450c and 450g)

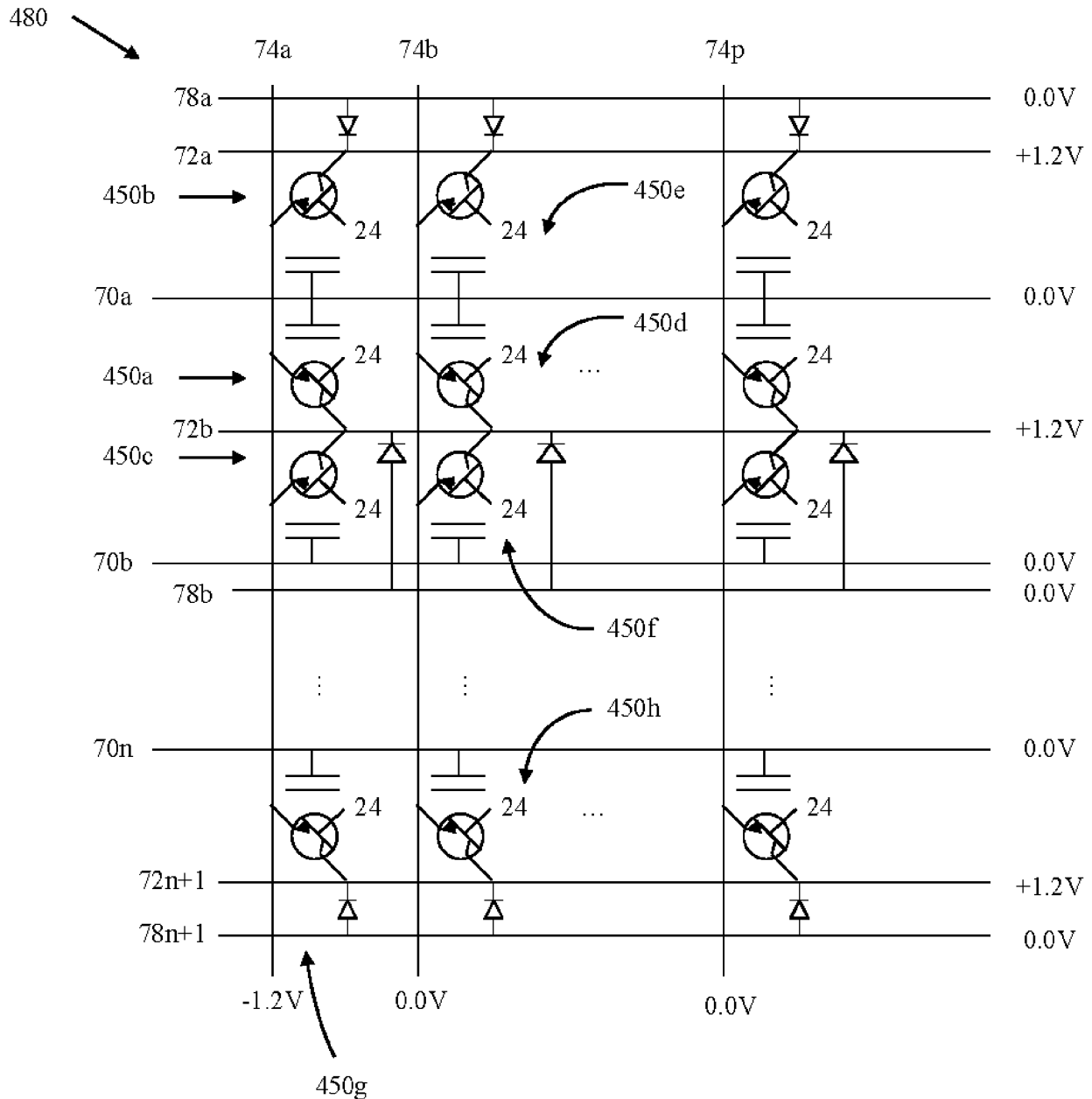


FIG. 67

Write Logic-0 Operation (Single Memory Cell 450a)

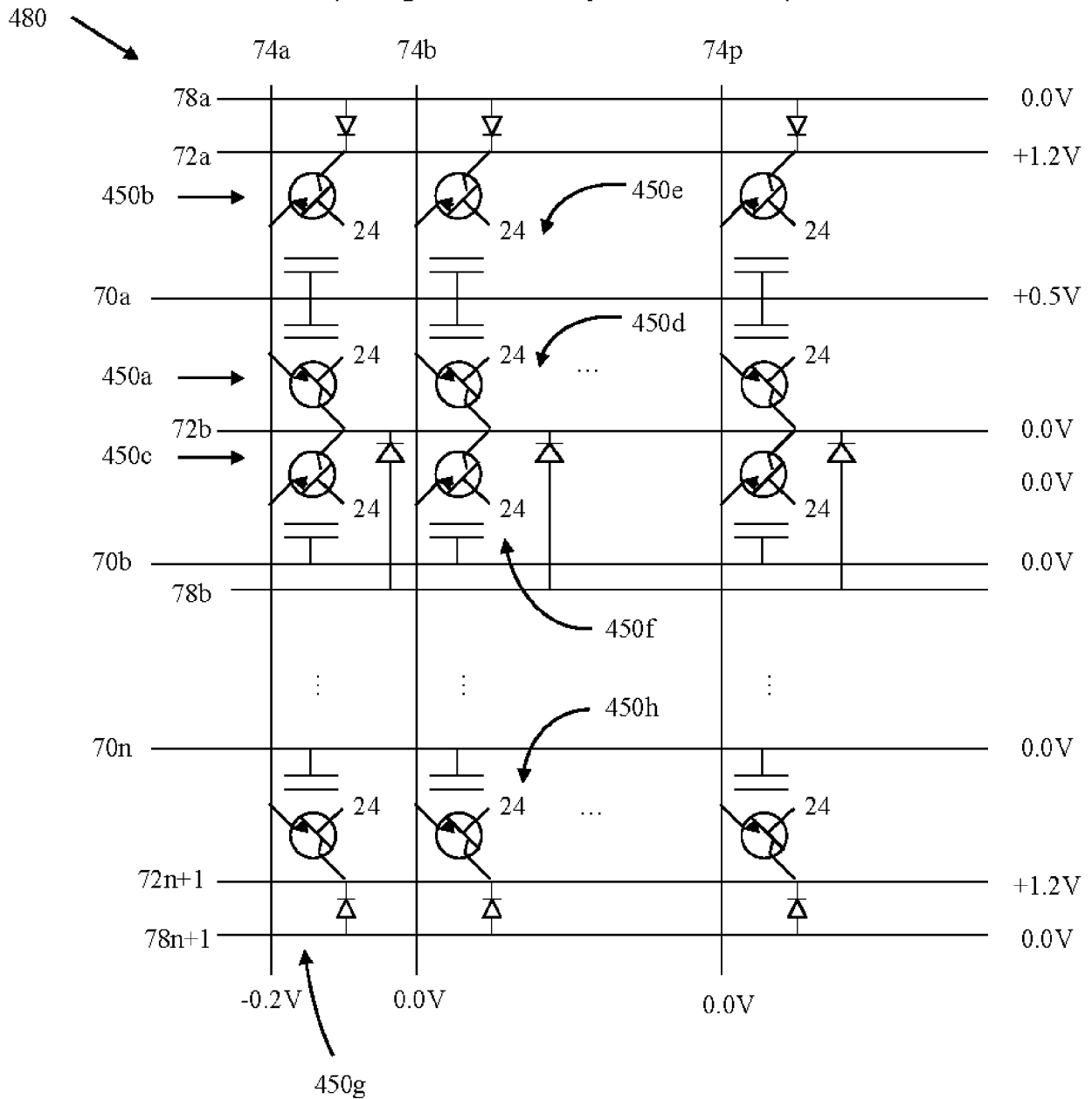


FIG. 68

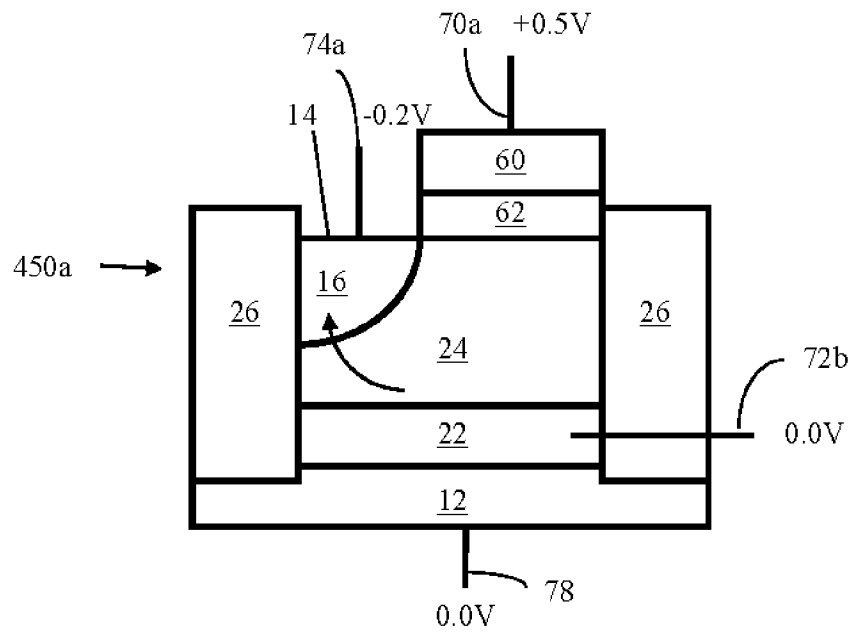


FIG. 69A

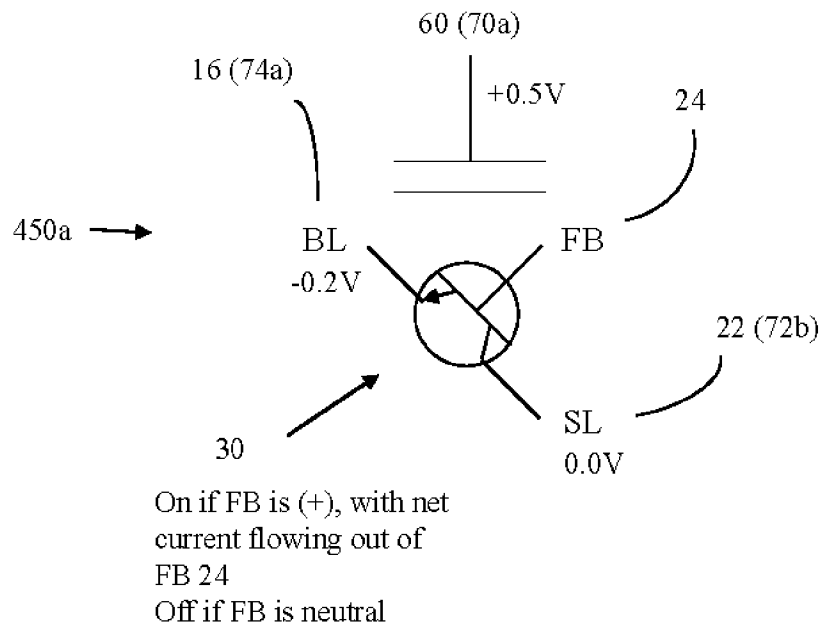


FIG. 69B

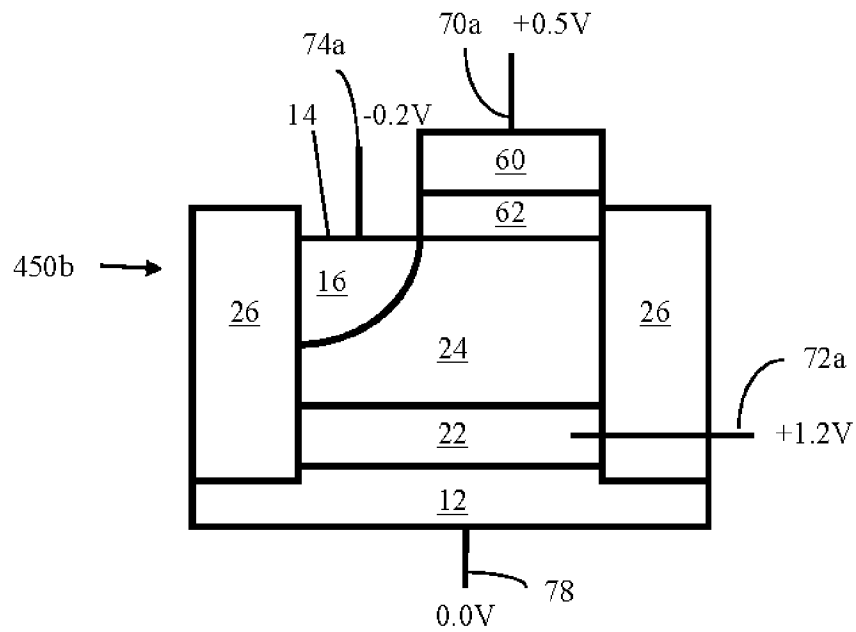
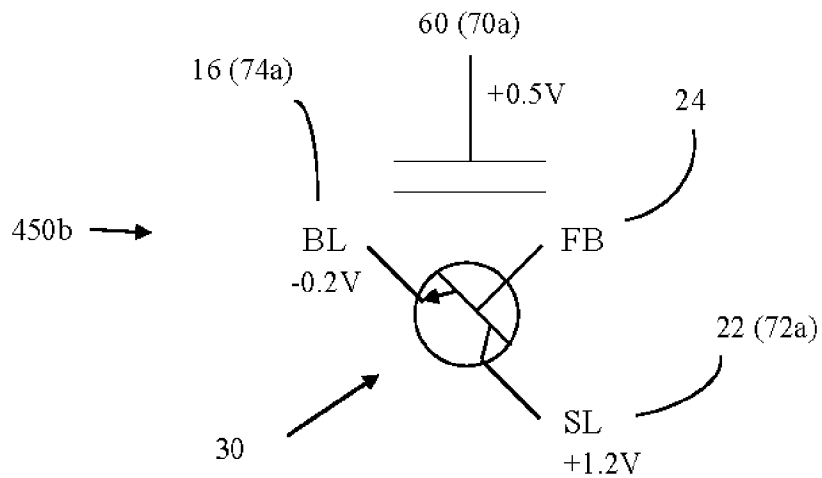


FIG. 69C



On if FB is (+); forward
bias current is balanced
by higher bipolar base
current
Off if FB is neutral

FIG. 69D

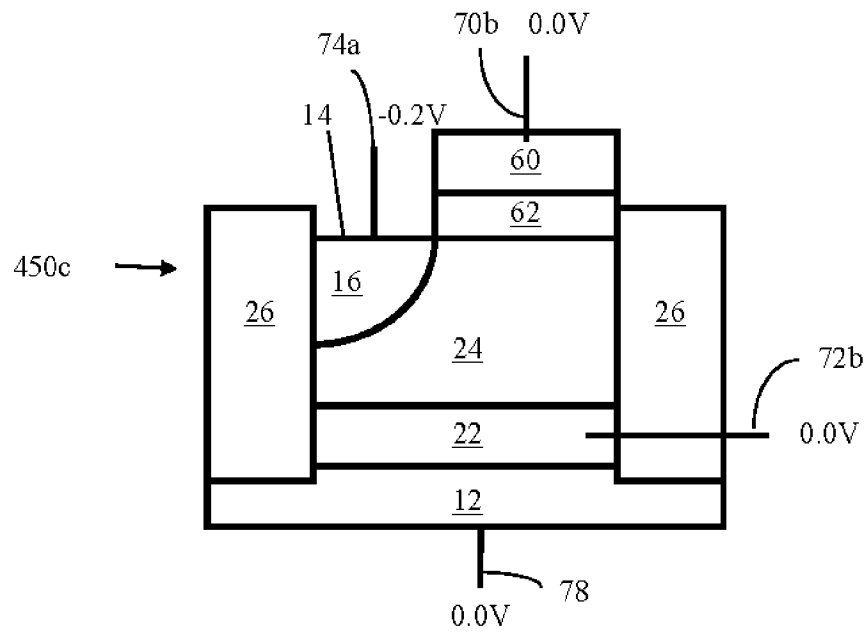


FIG. 69E

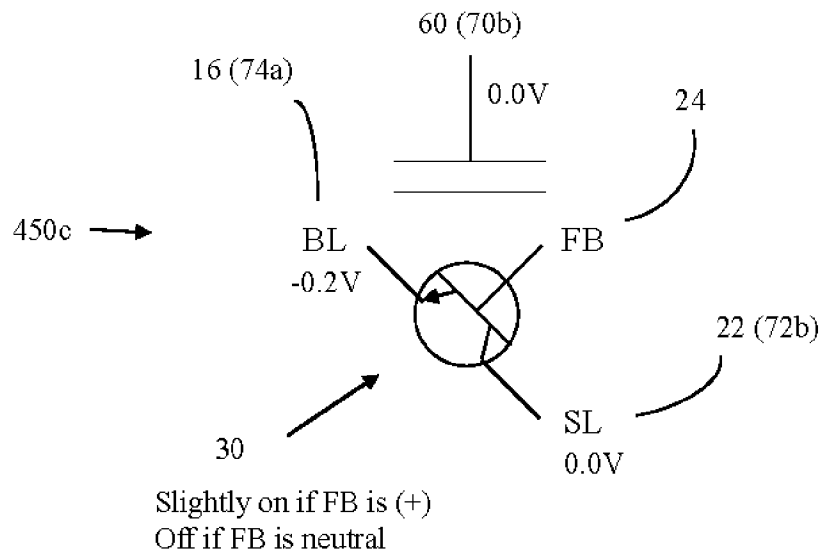


FIG. 69F

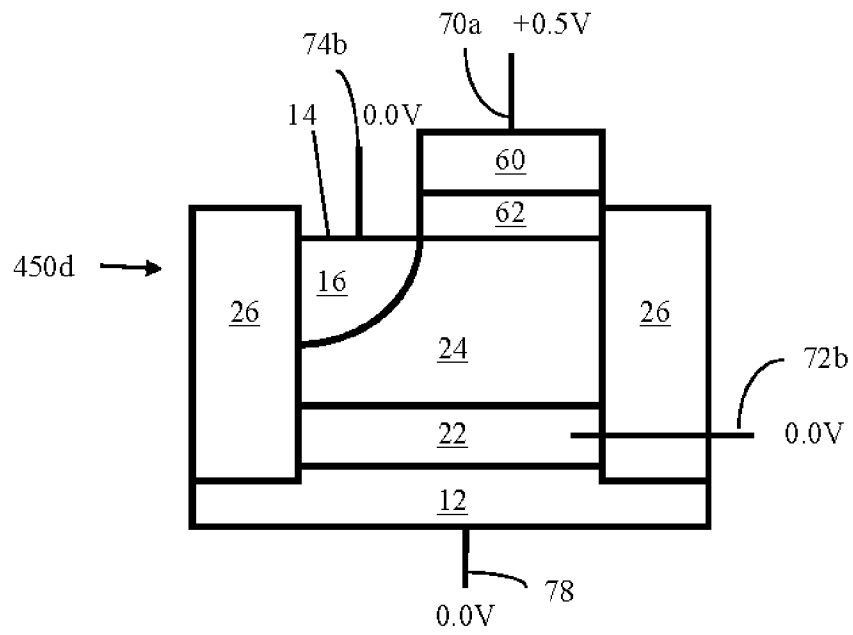


FIG. 69G

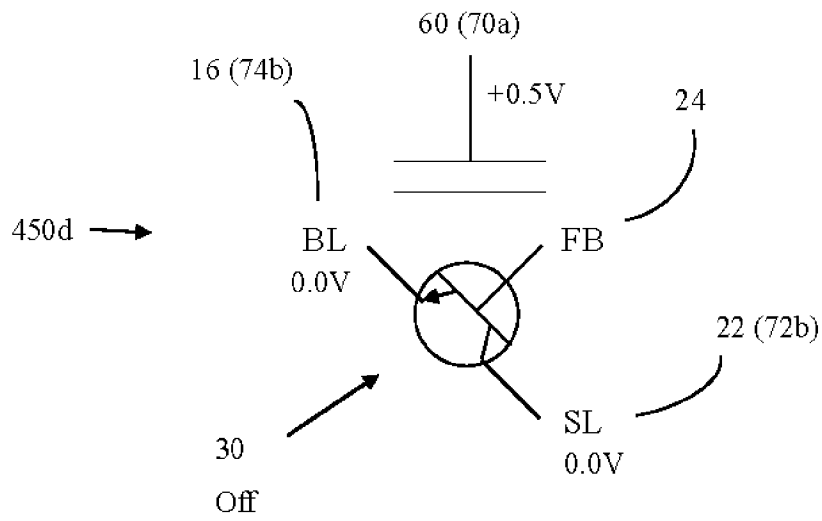


FIG. 69H

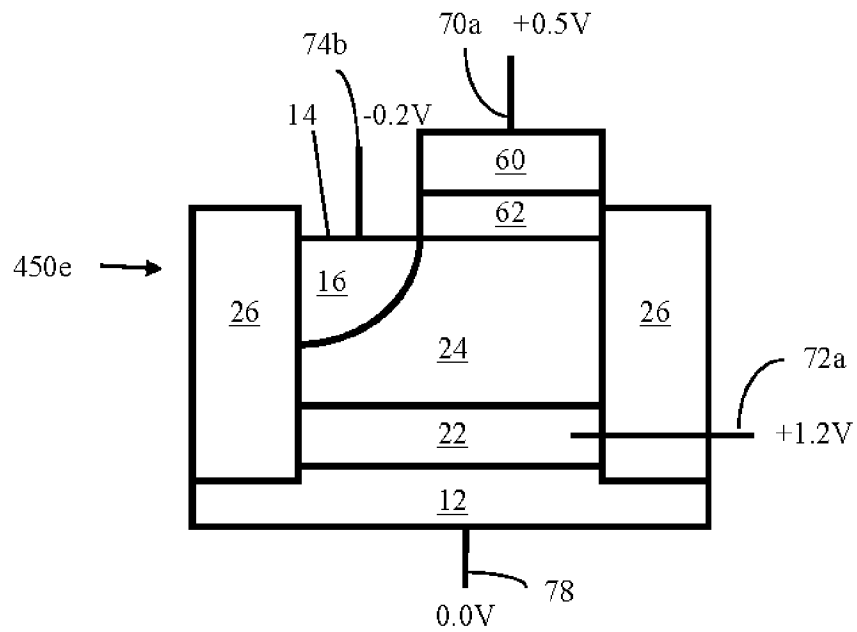
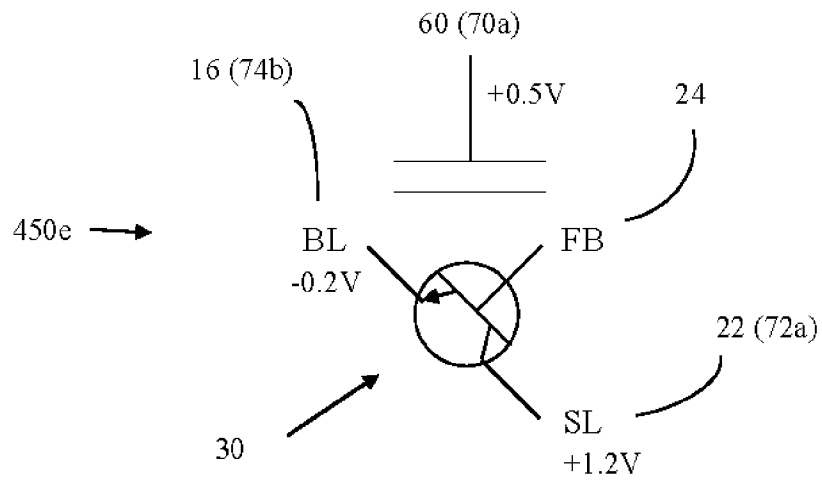


FIG. 69I



On if FB is (+); forward
bias current is balanced
by higher bipolar base
current
Off if FB is neutral

FIG. 69J

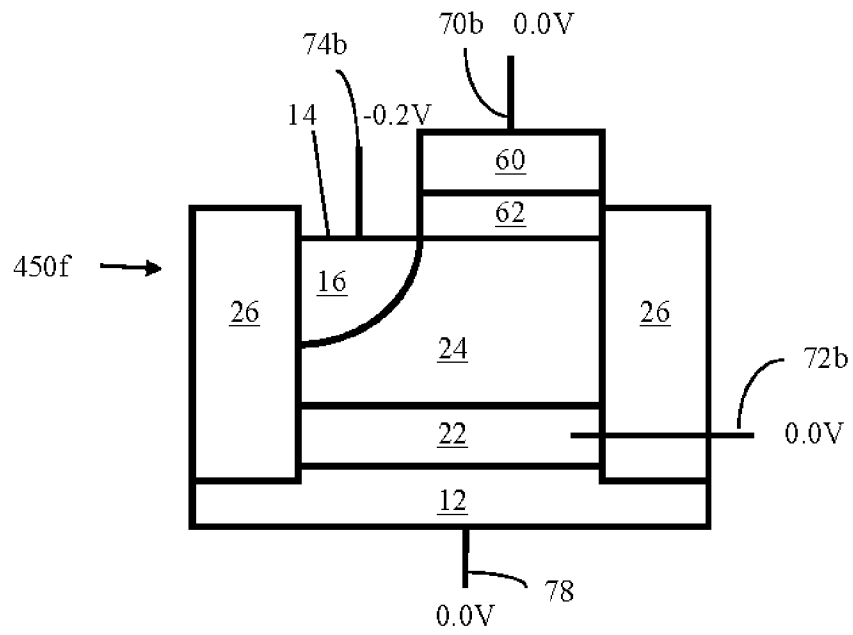


FIG. 69K

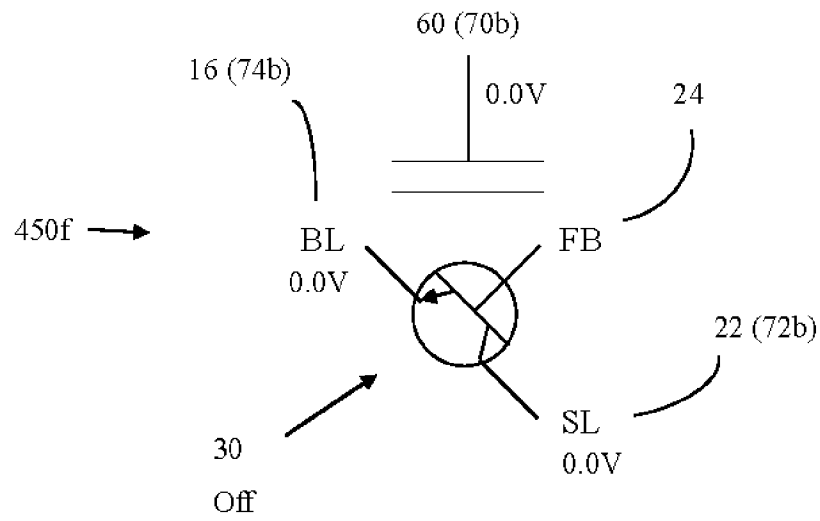
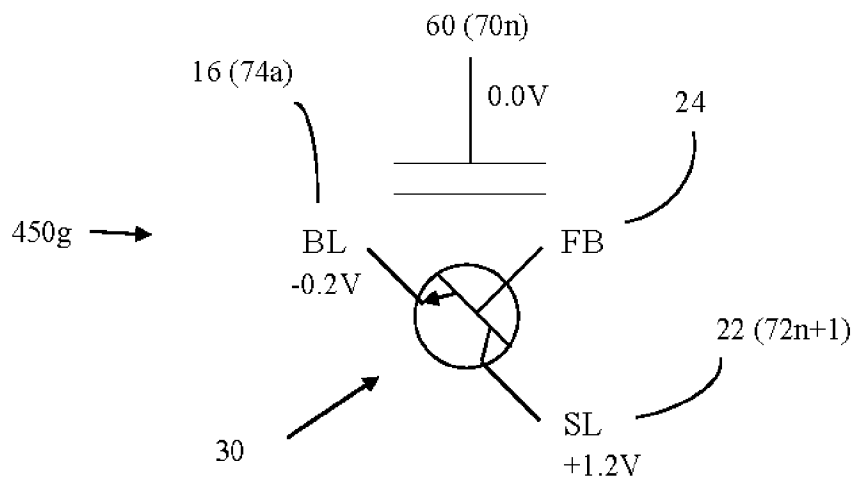
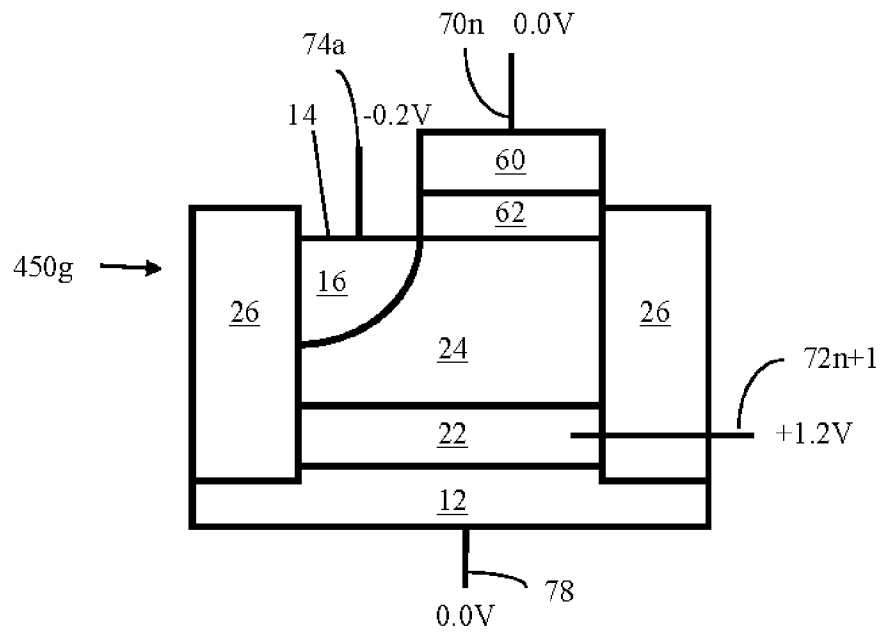


FIG. 69L



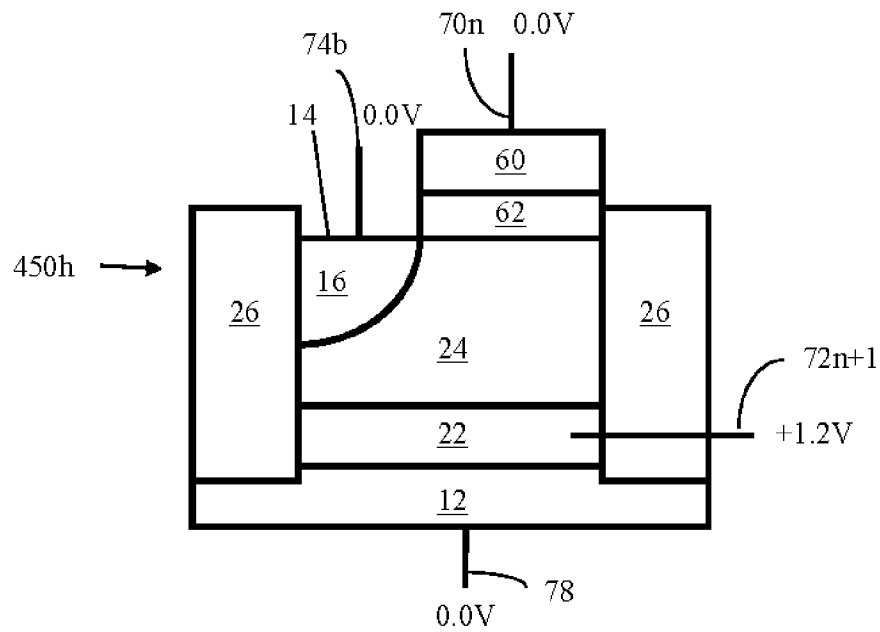


FIG. 69O

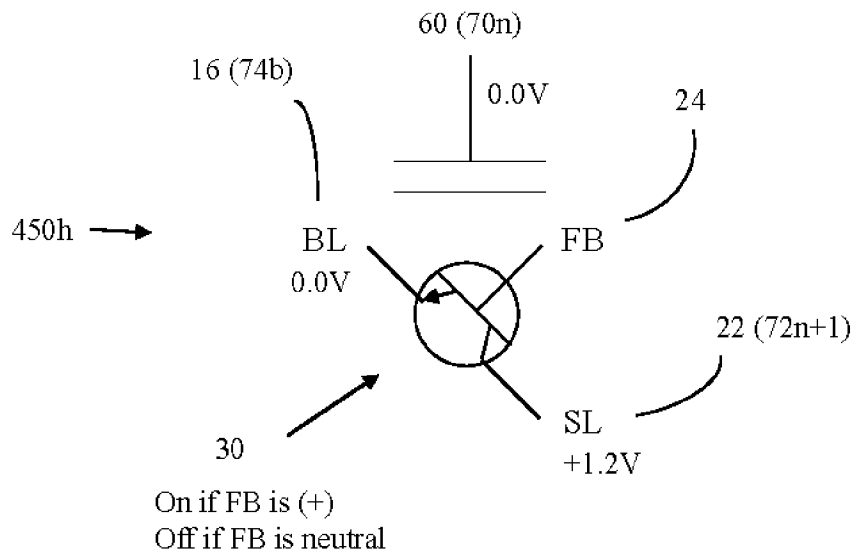


FIG. 69P

Write Logic-1 Operation – GIDL (Single Memory Cell 450a)

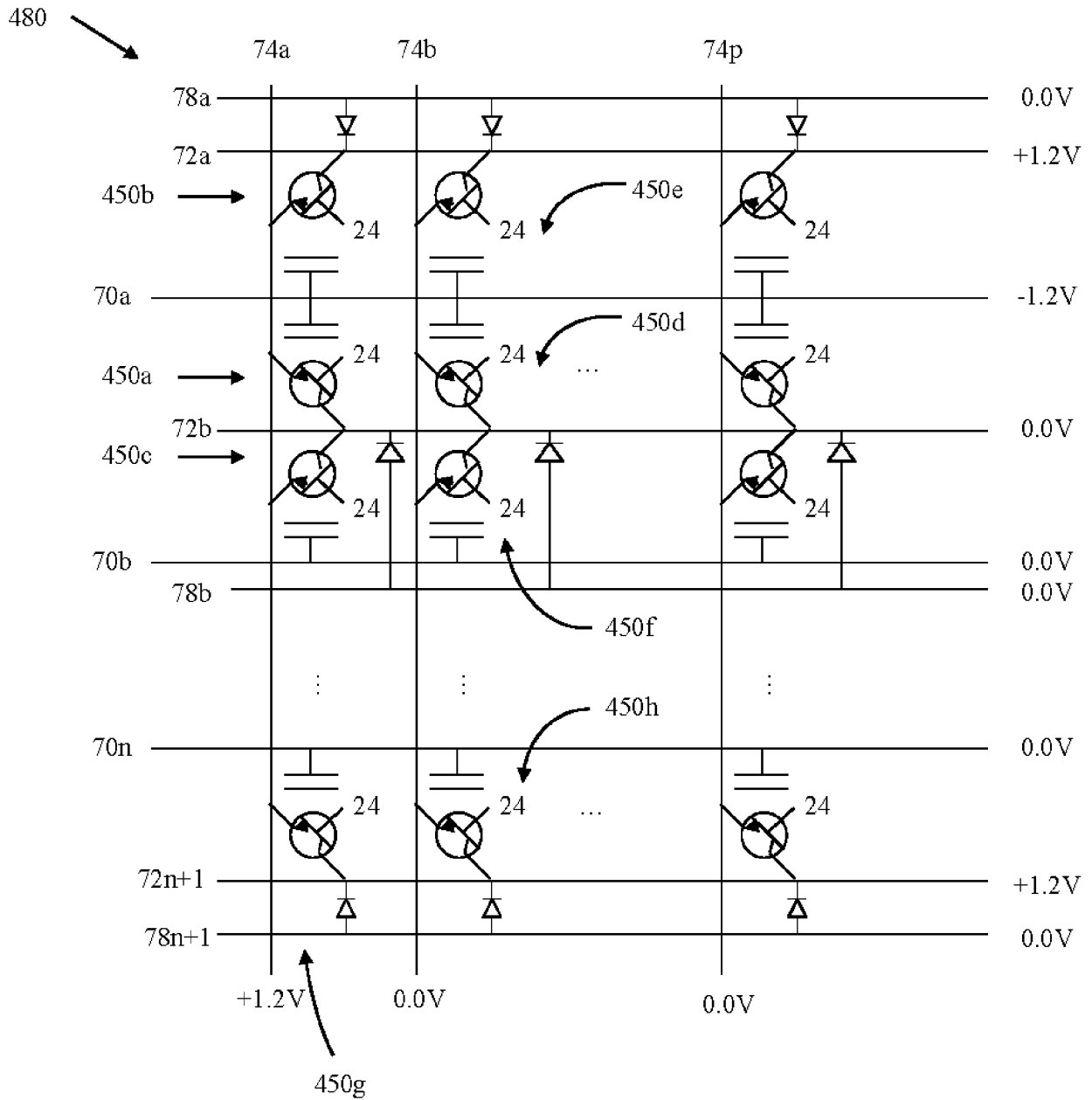


FIG. 70

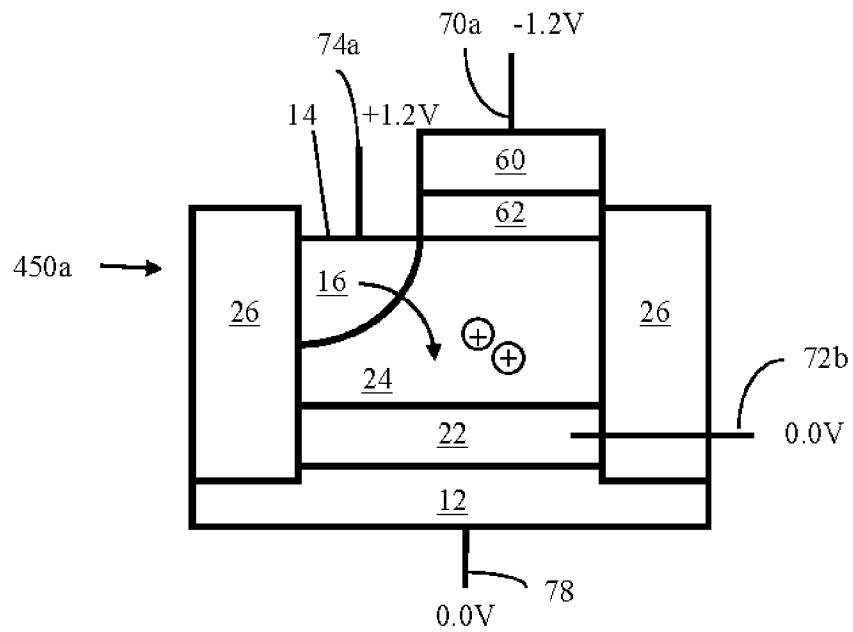


FIG. 71A

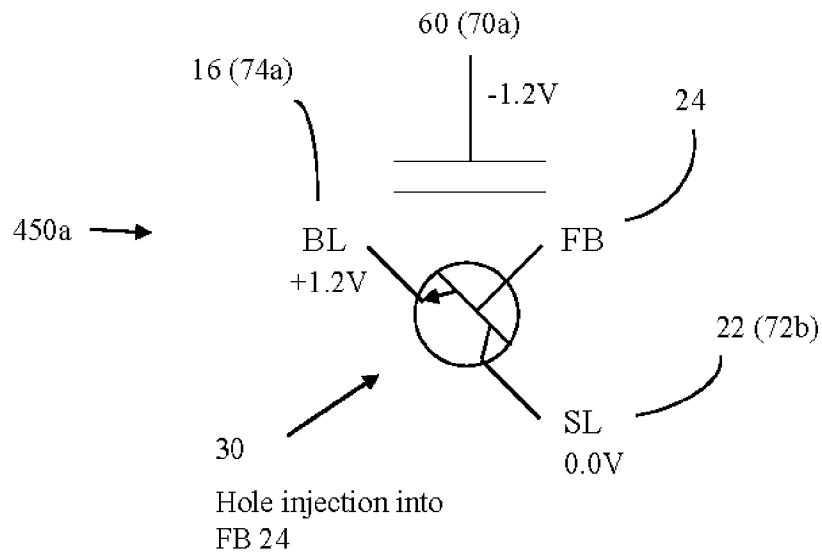


FIG. 71B

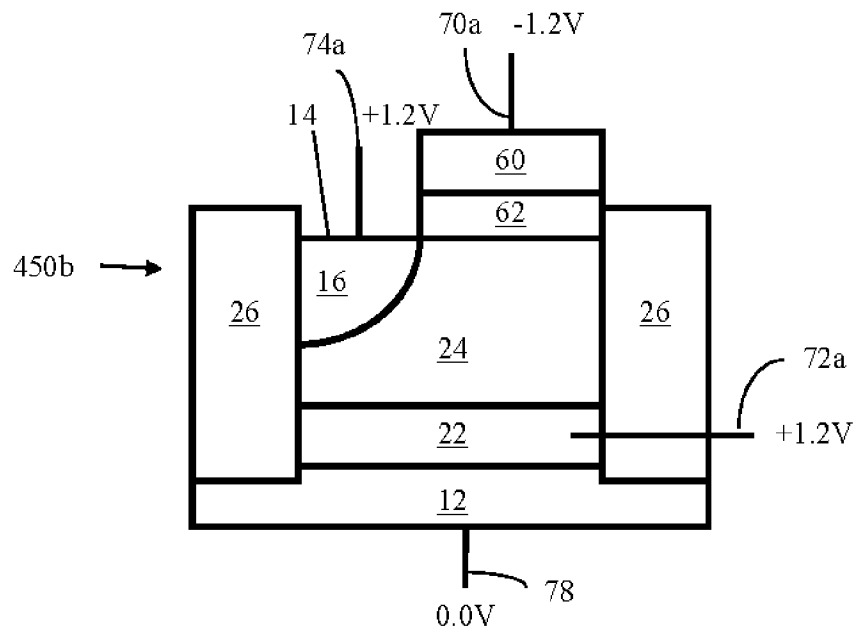


FIG. 71C

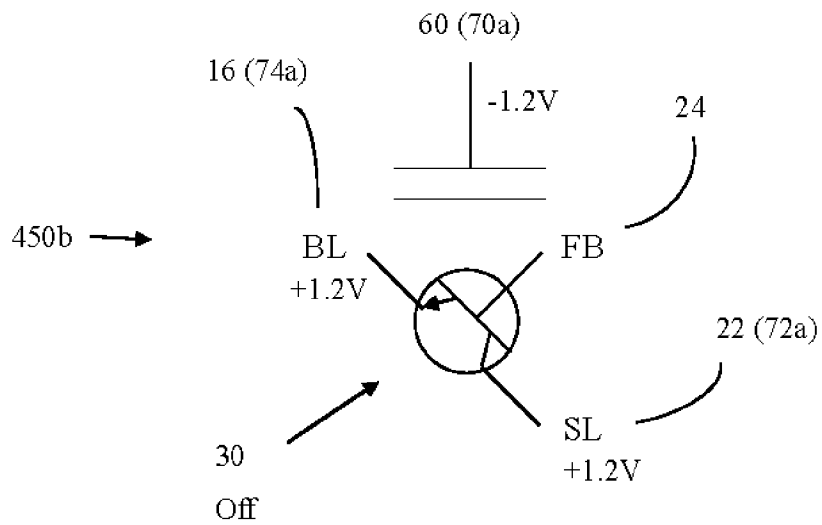


FIG. 71D

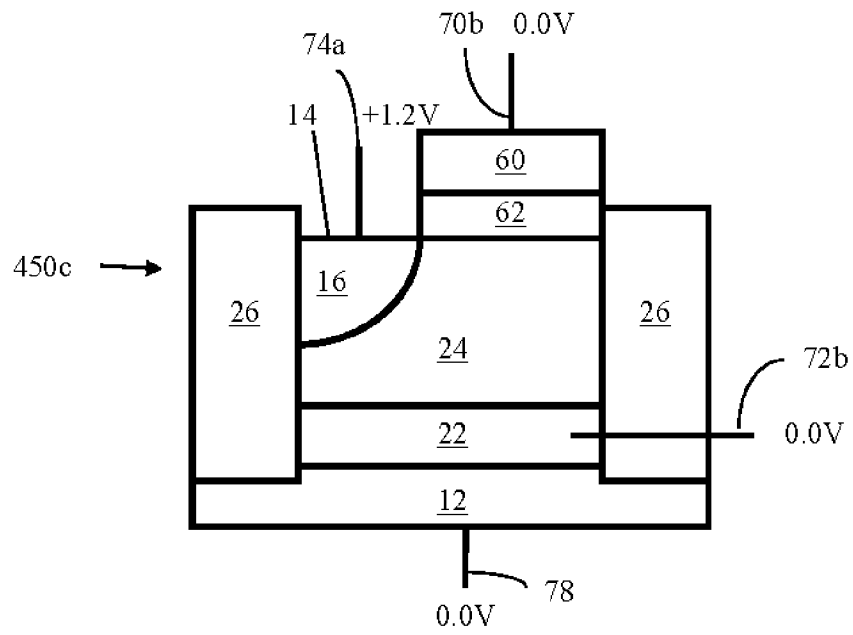


FIG. 71E

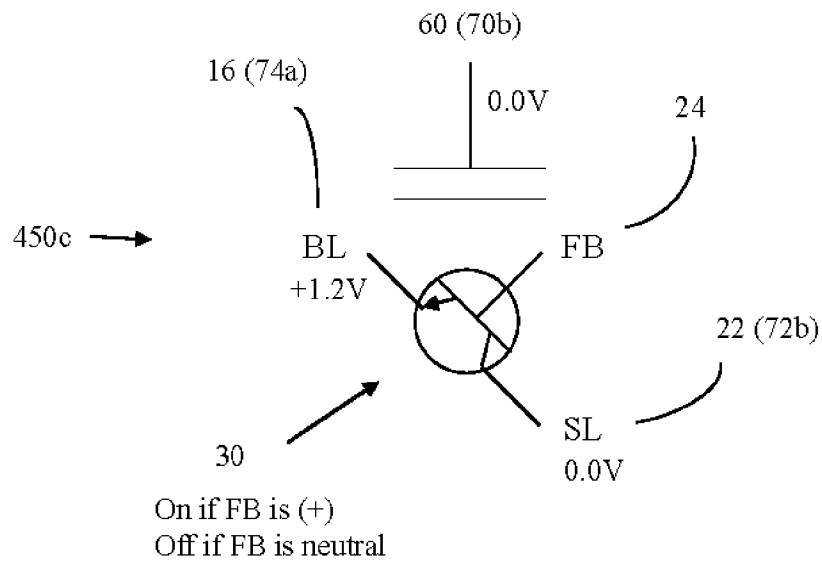


FIG. 71F

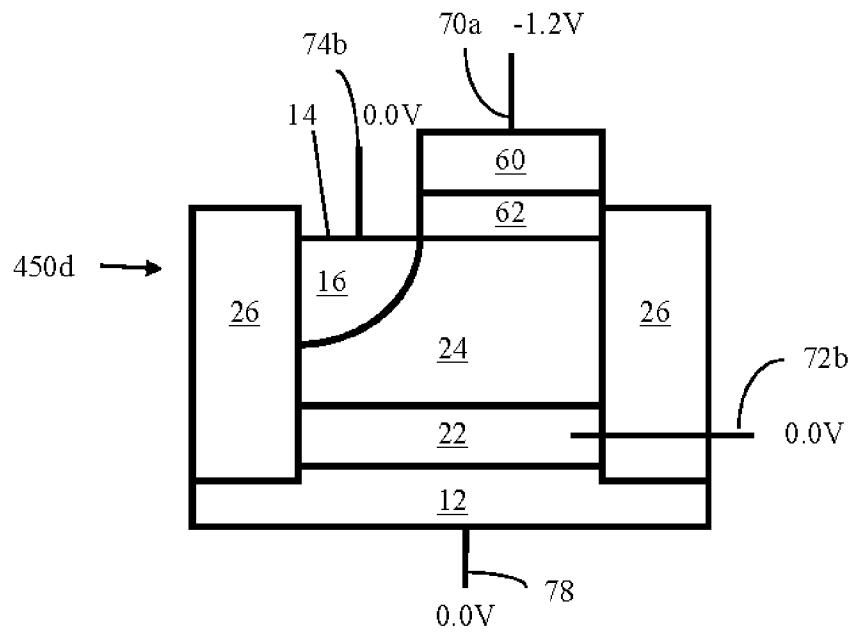


FIG. 71G

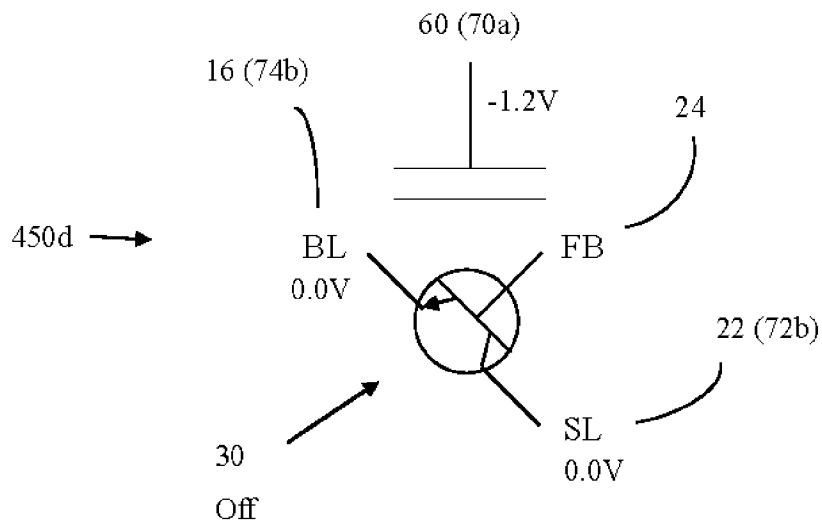


FIG. 71H

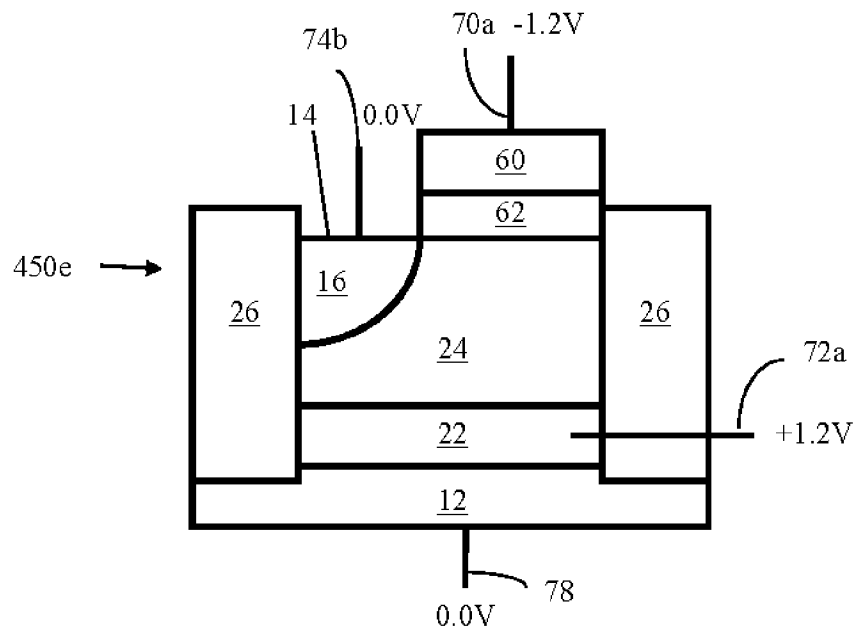


FIG. 71I

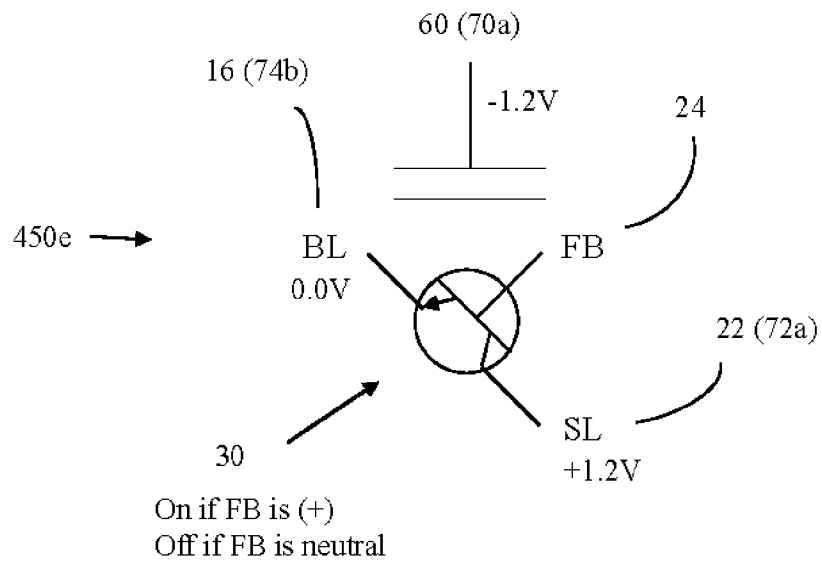


FIG. 71J

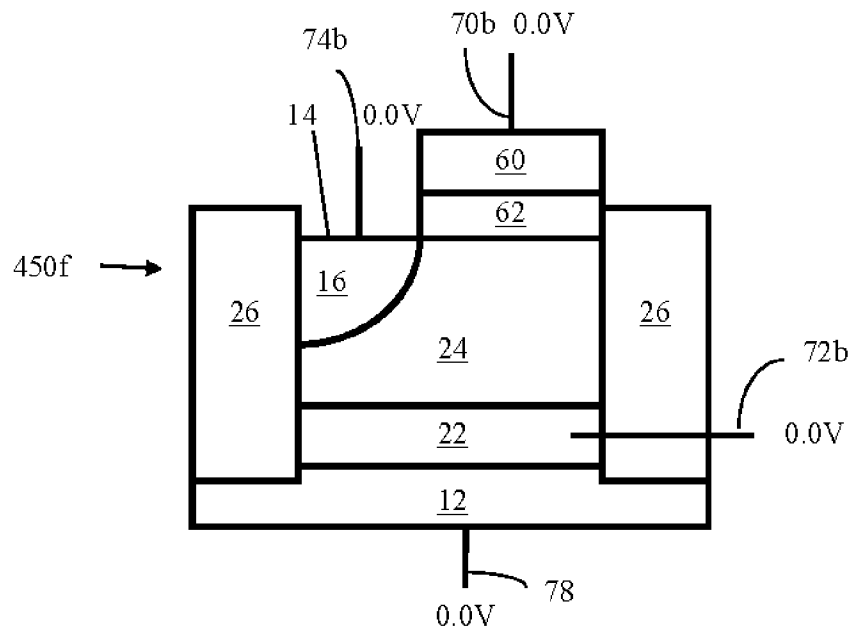


FIG. 71K

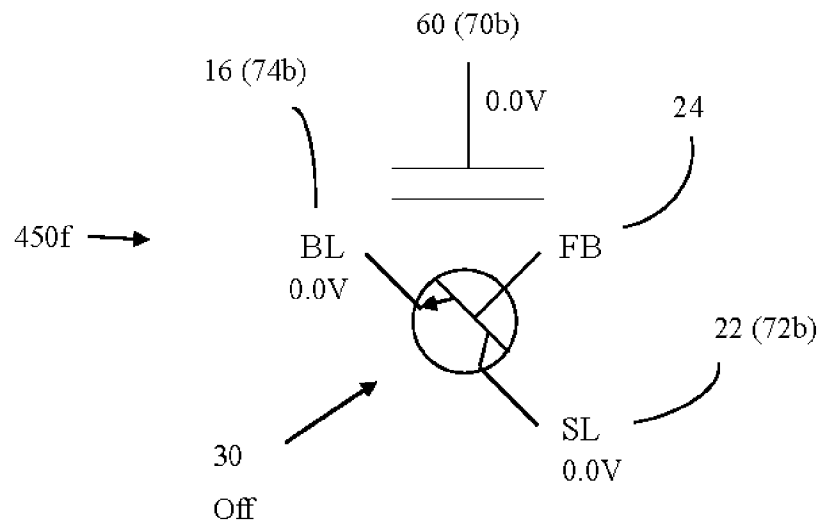


FIG. 71L

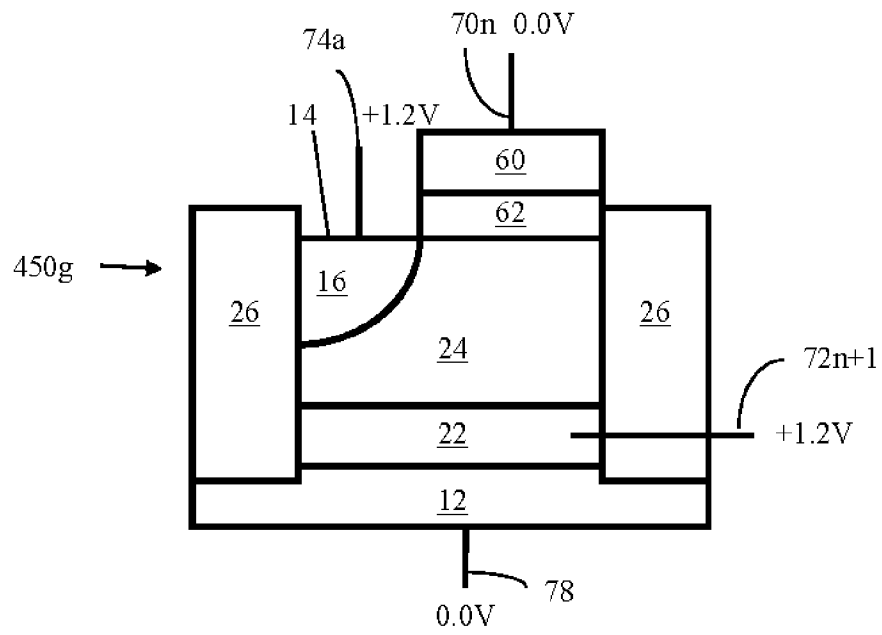


FIG. 71M

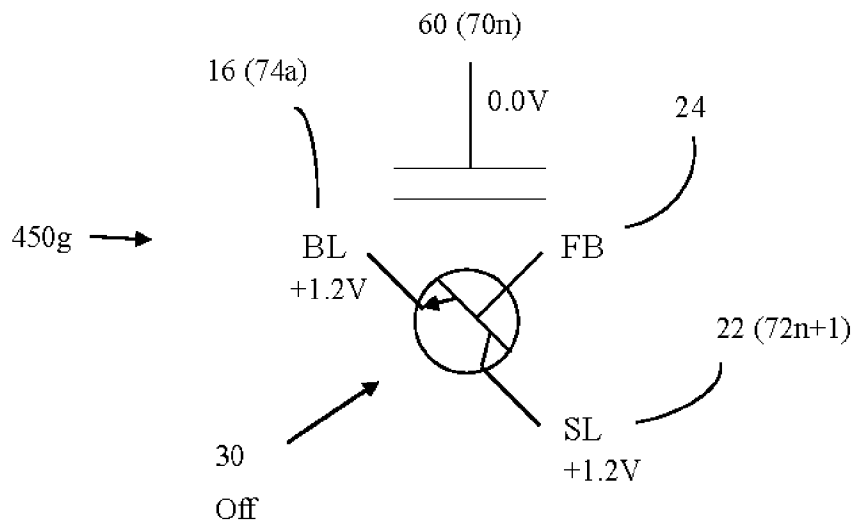


FIG. 71N

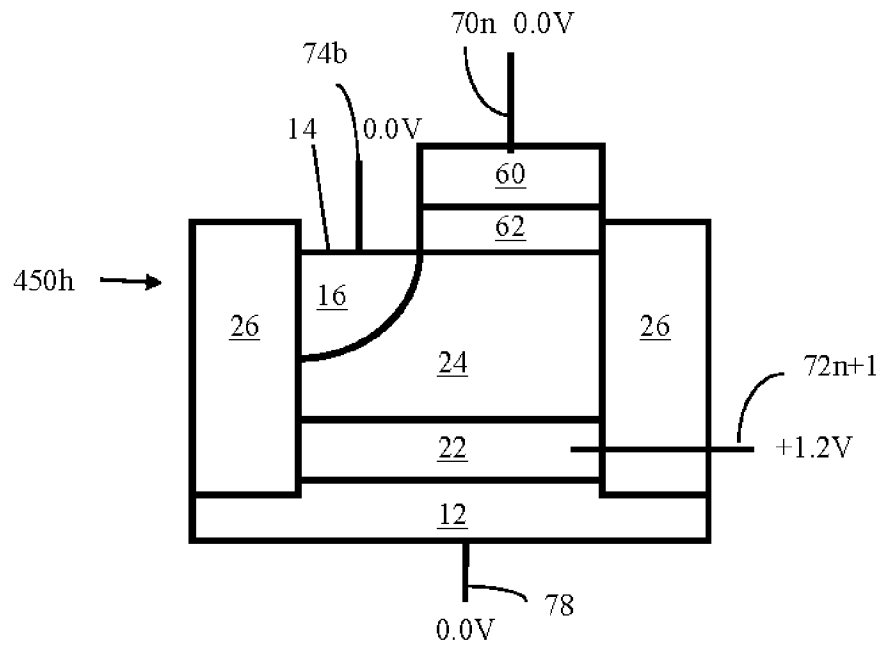


FIG. 71O

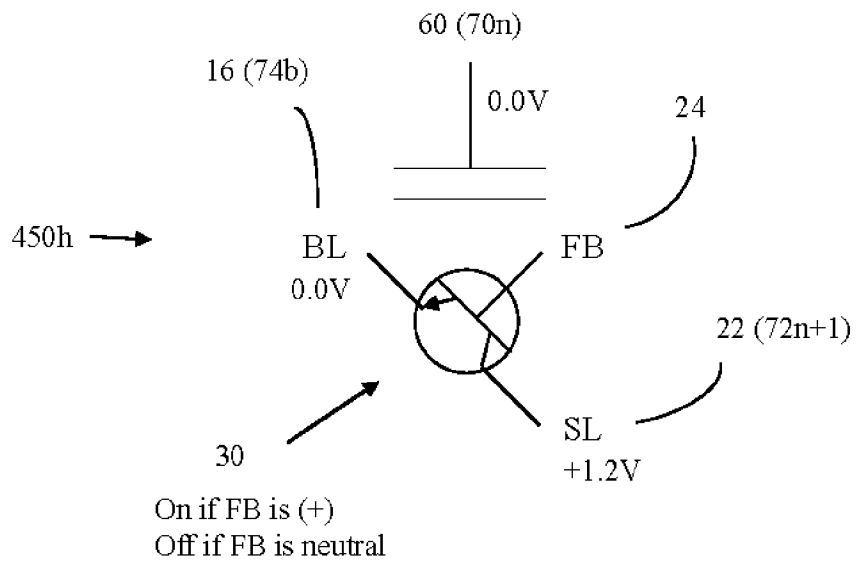


FIG. 71P

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 450a)

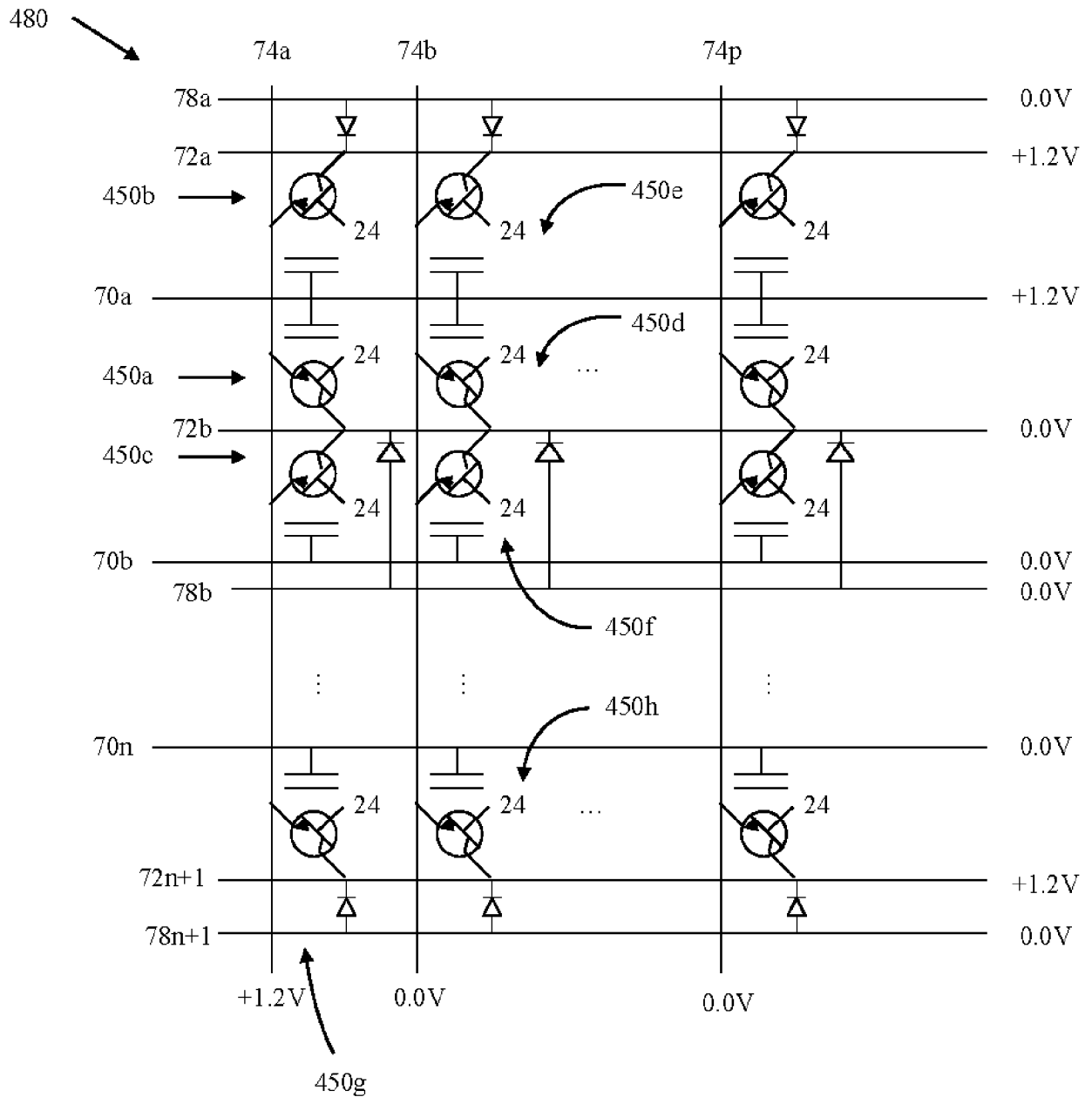


FIG. 72

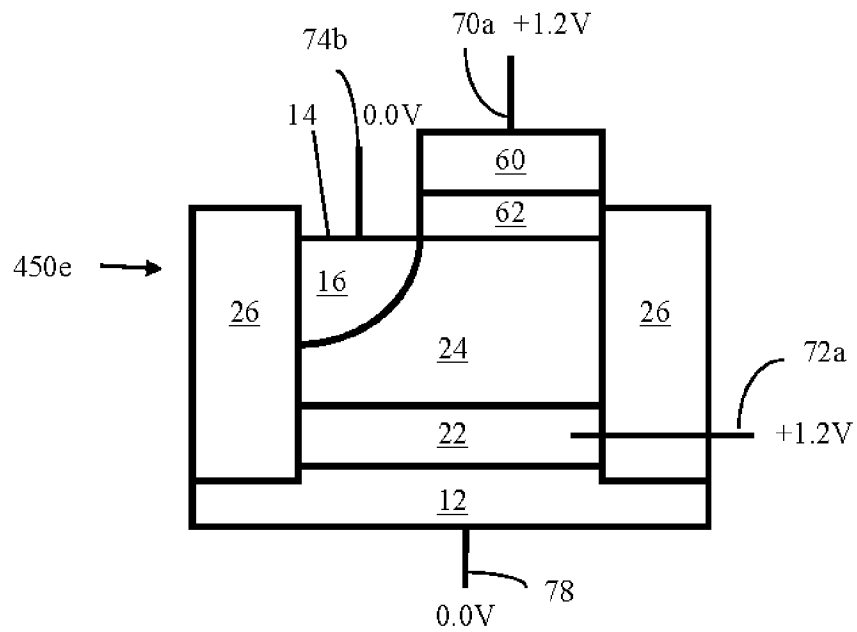


FIG. 73A

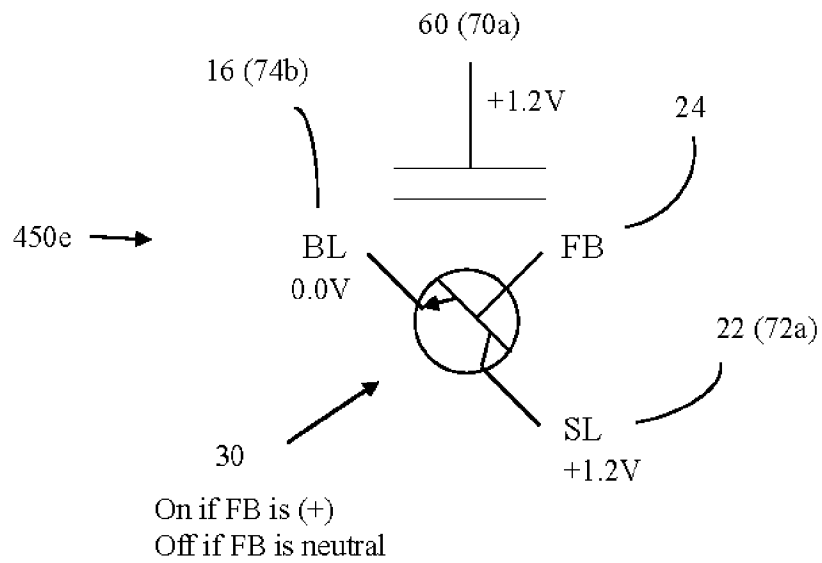


FIG. 73B

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 450a)

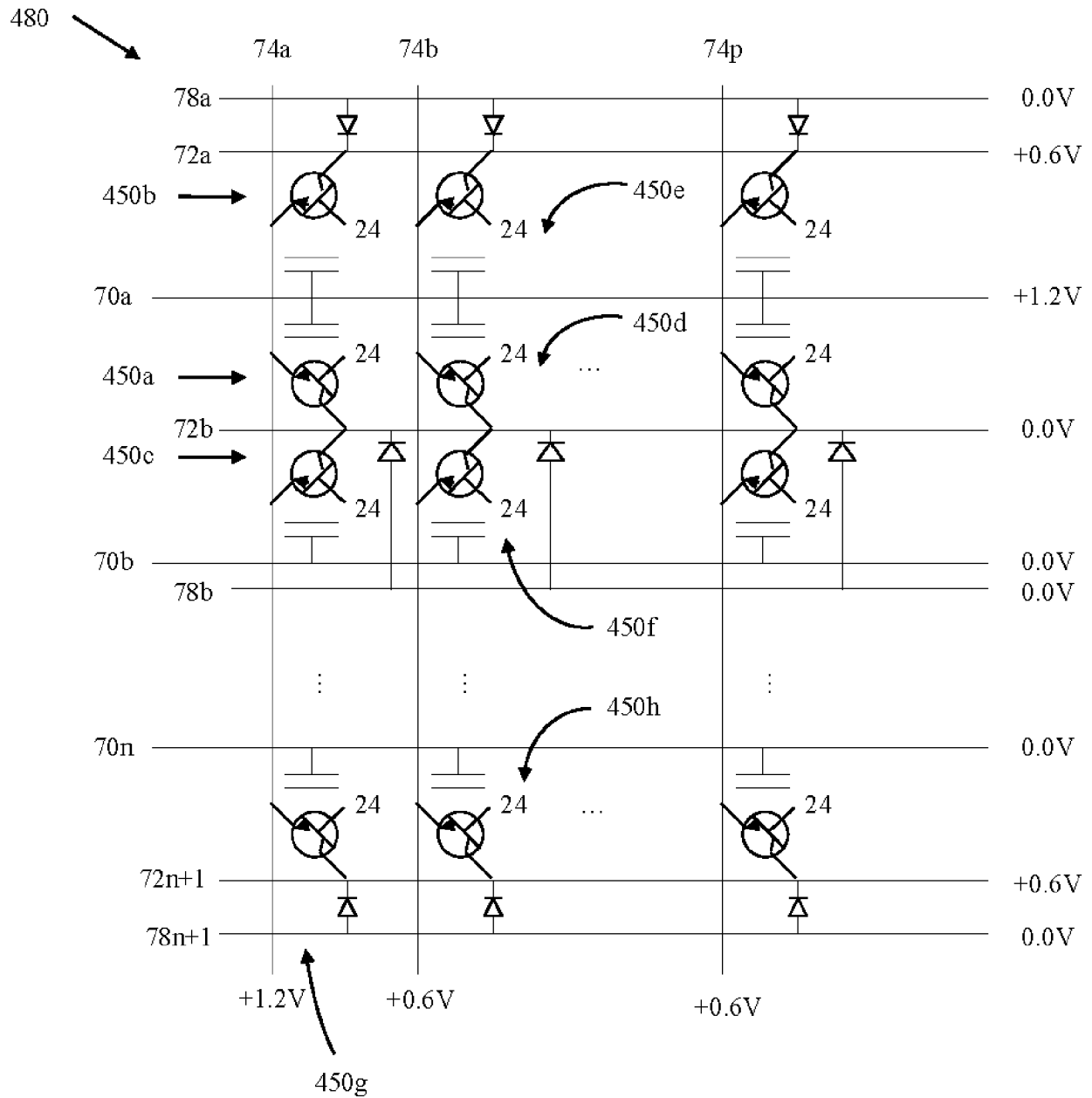


FIG. 74

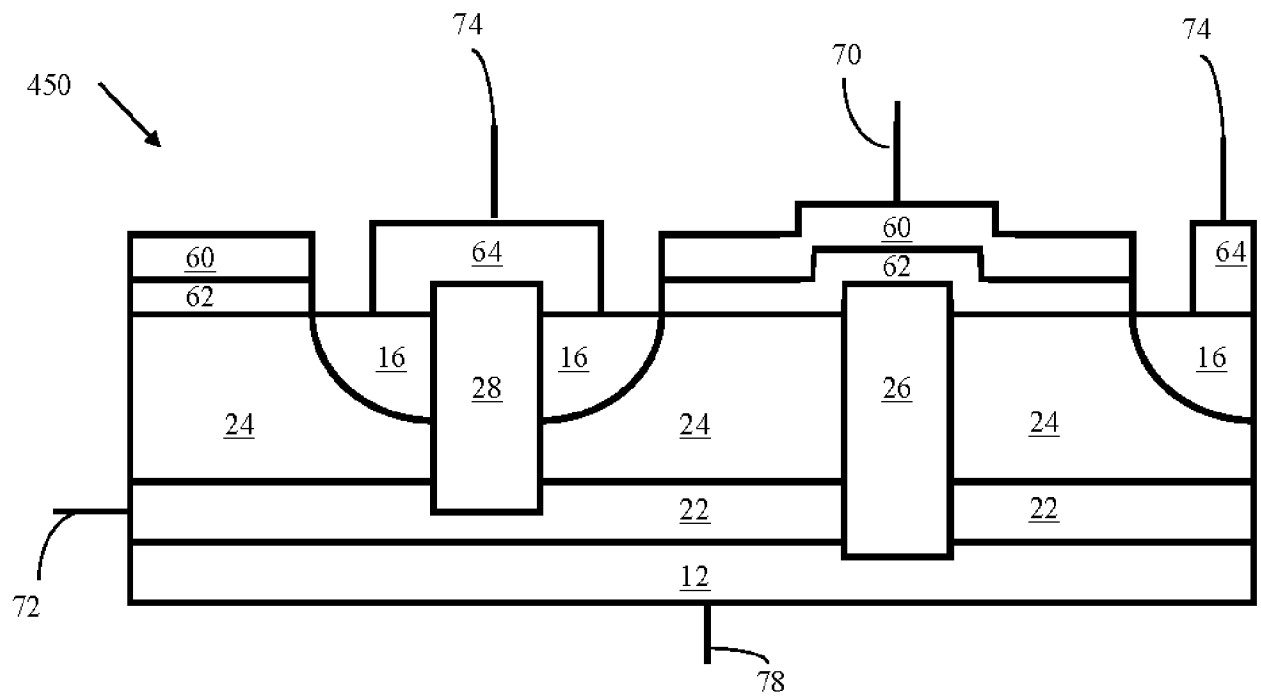


FIG. 75A

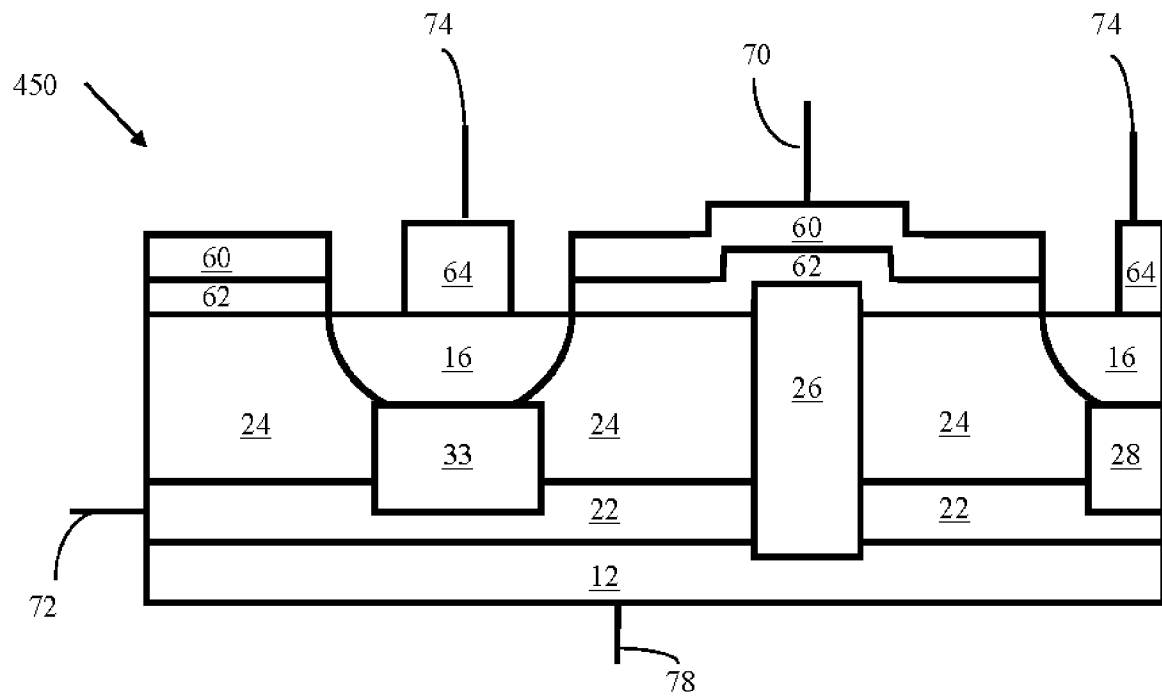


FIG. 75B

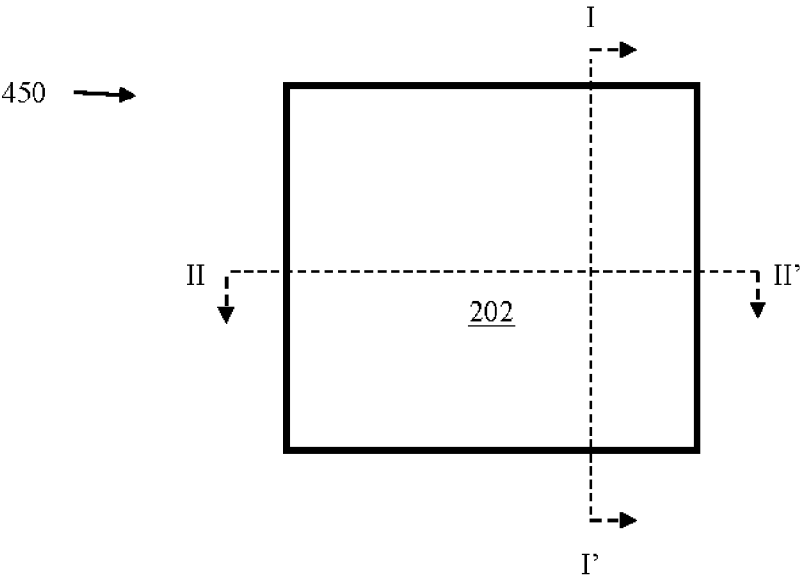


FIG. 76A

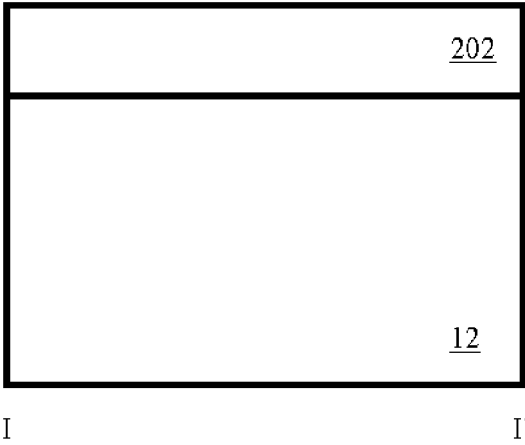


FIG. 76B

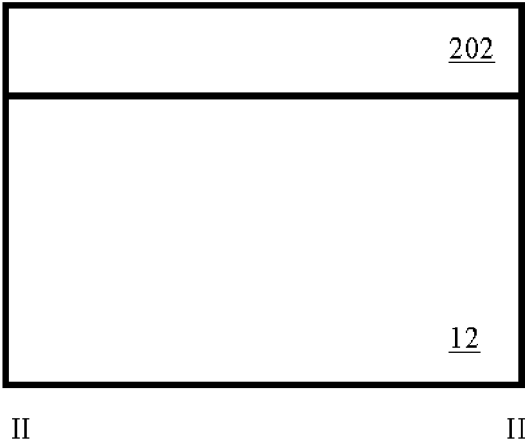


FIG. 76C

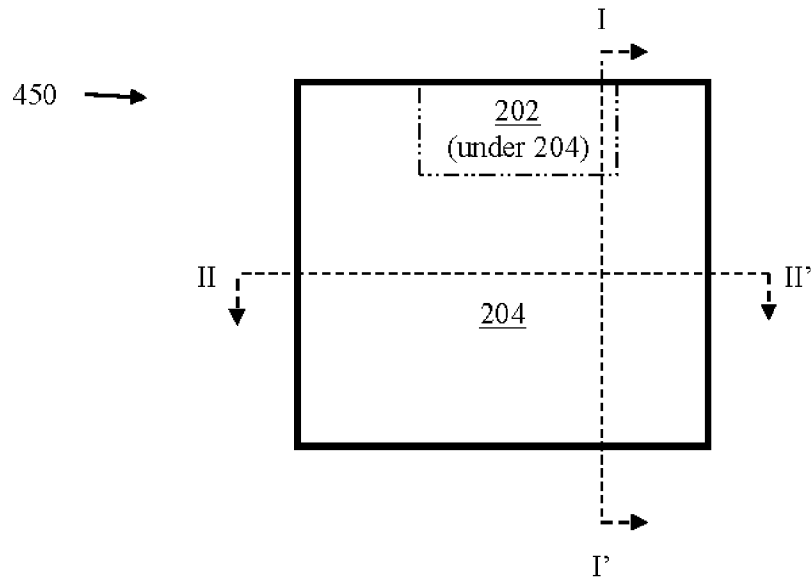


FIG. 76D

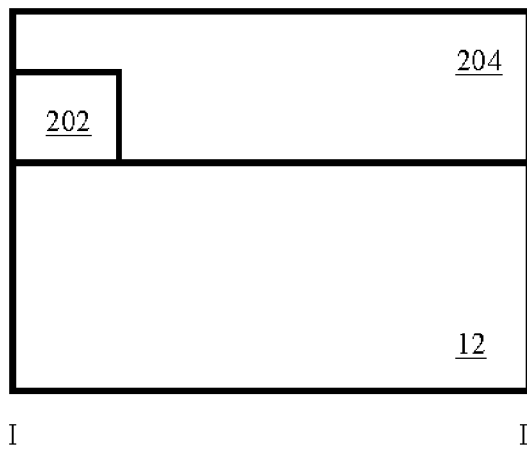


FIG. 76E

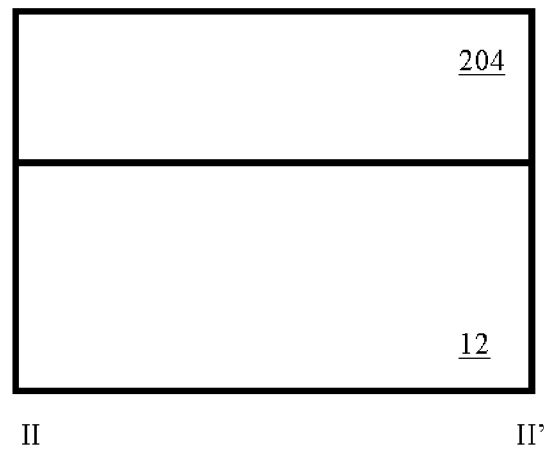


FIG. 76F

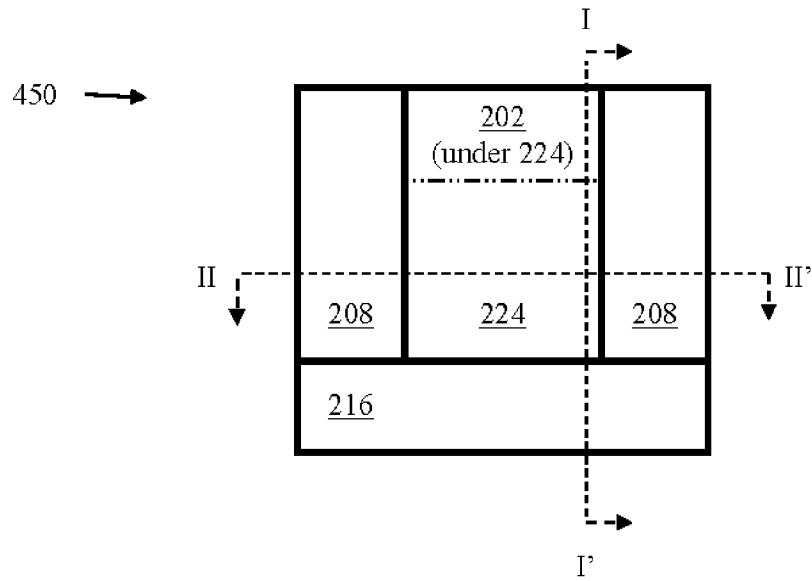


FIG. 76G

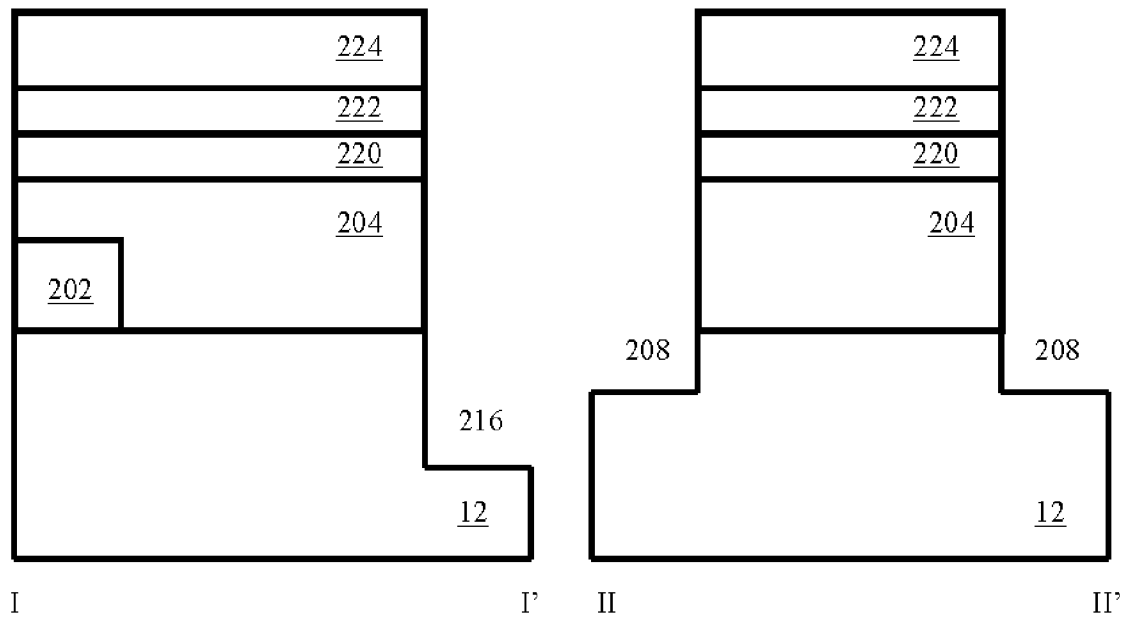


FIG. 76H

FIG. 76I

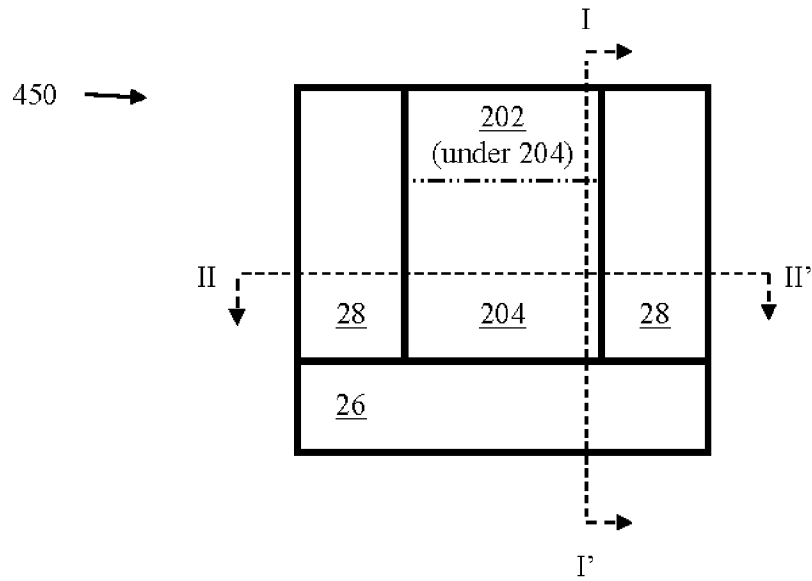


FIG. 76J

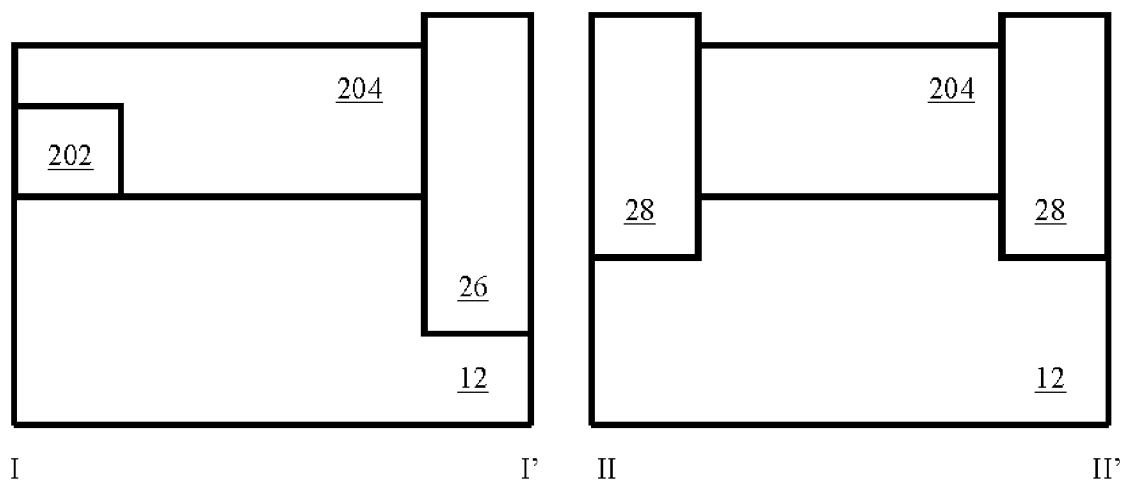


FIG. 76K

FIG. 76L

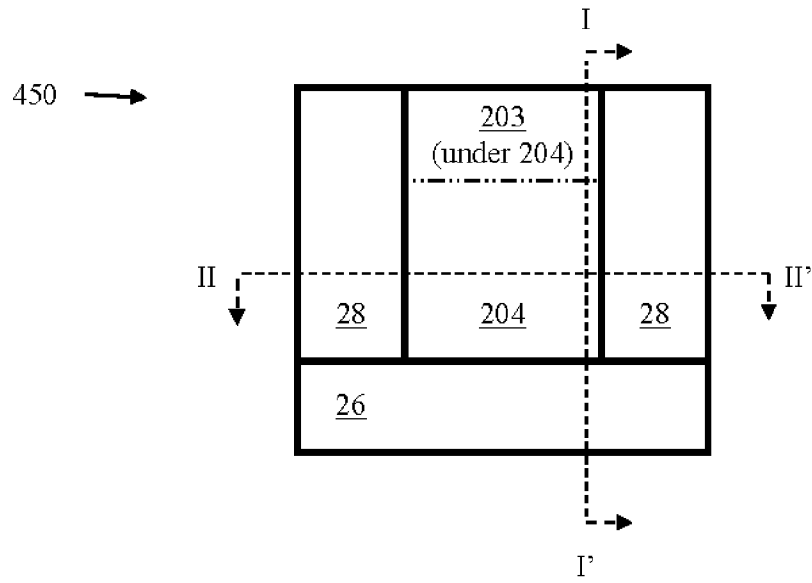


FIG. 76M

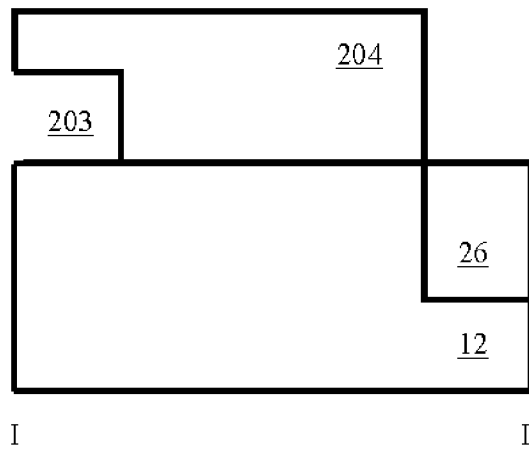


FIG. 76N

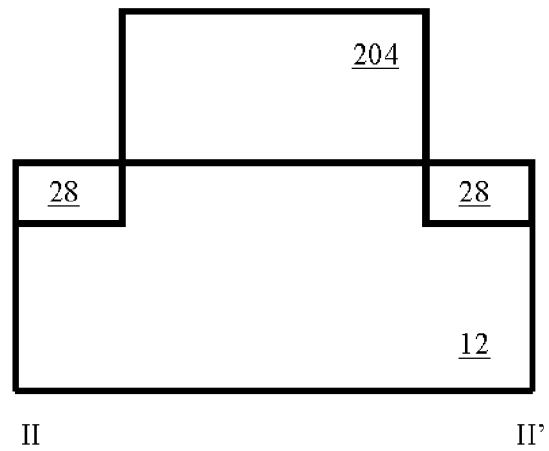


FIG. 76O

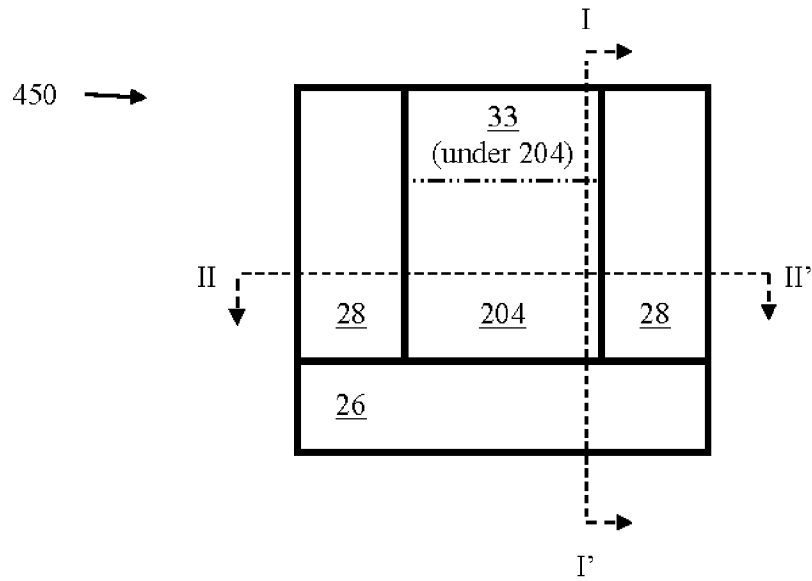


FIG. 76P

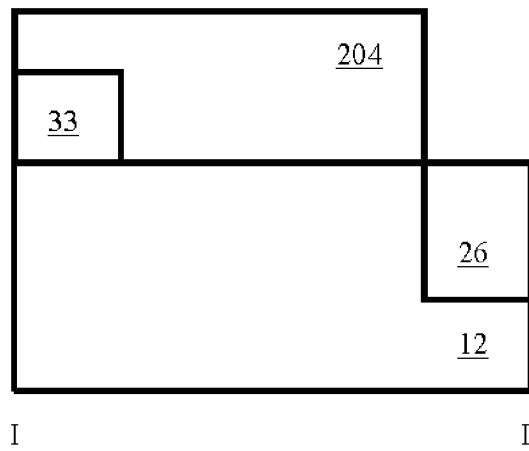


FIG. 76Q

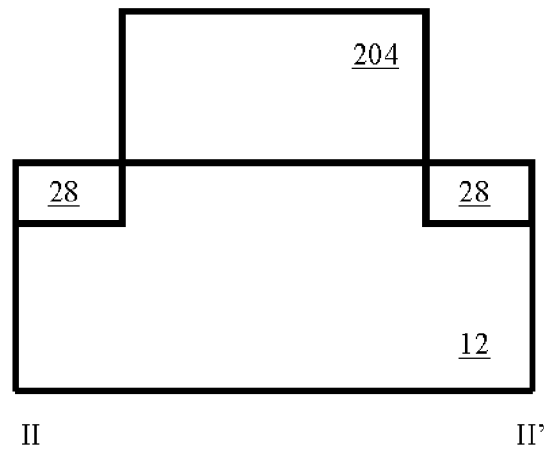


FIG. 76R

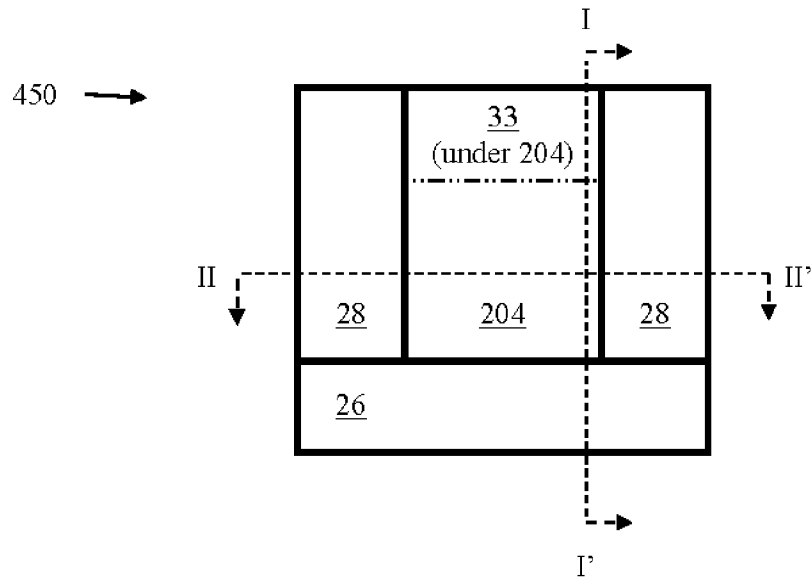


FIG. 76S

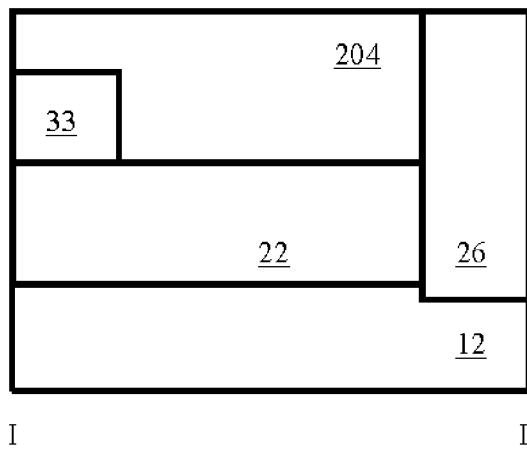


FIG. 76T

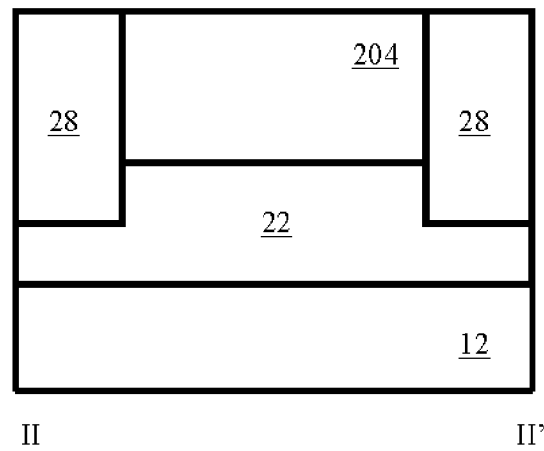


FIG. 76U

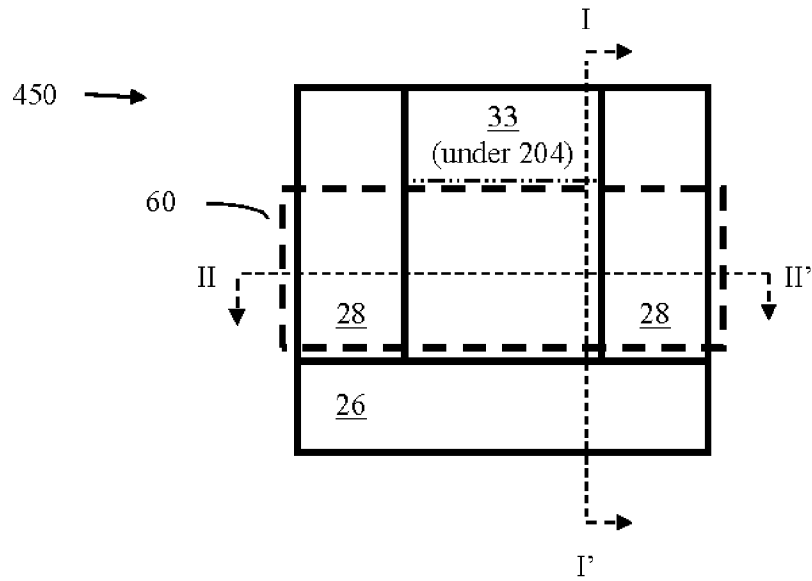


FIG. 76V

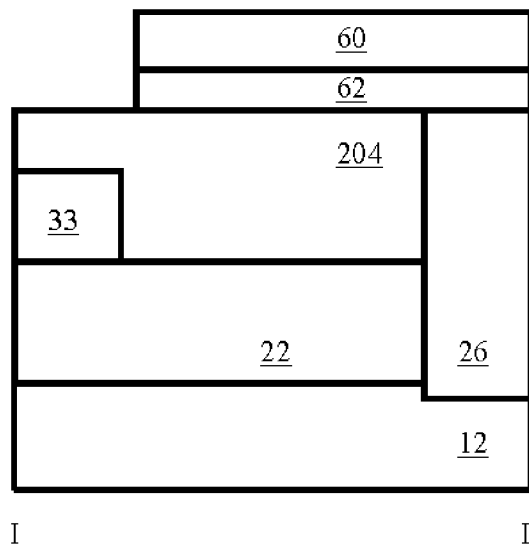


FIG. 76W

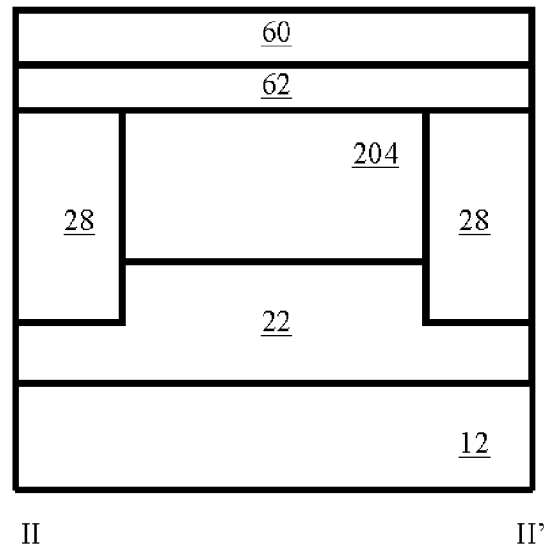


FIG. 76X

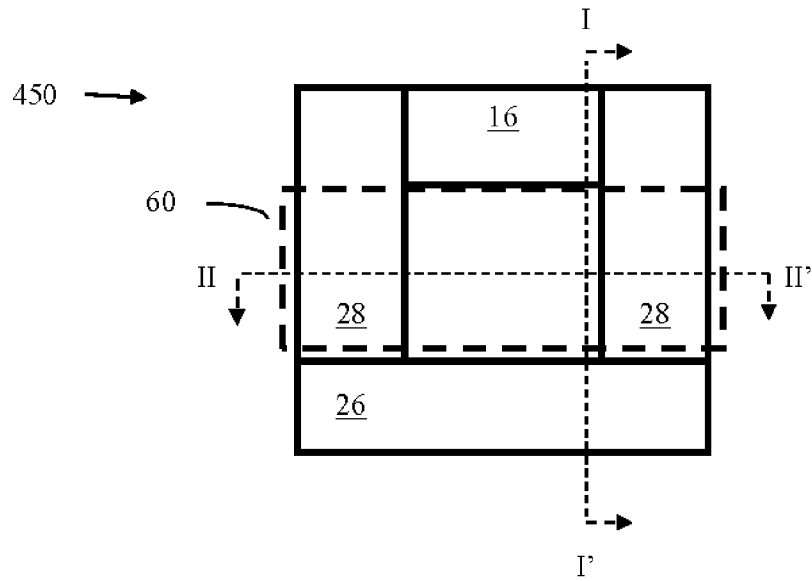


FIG. 76Y

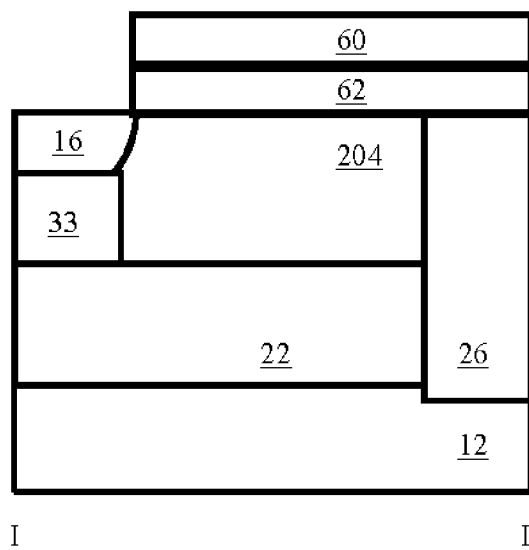


FIG. 76Z

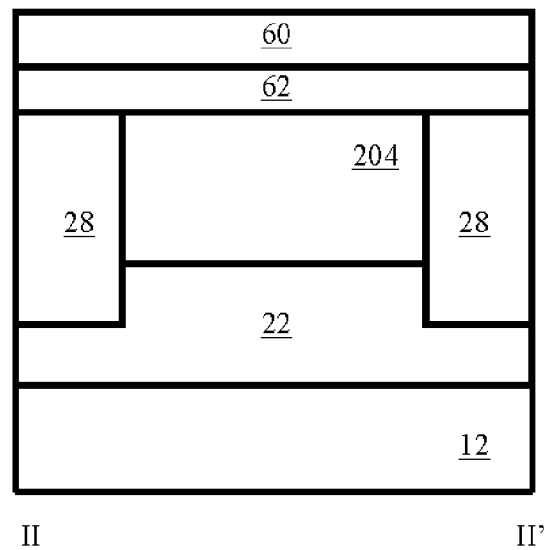


FIG. 76AA

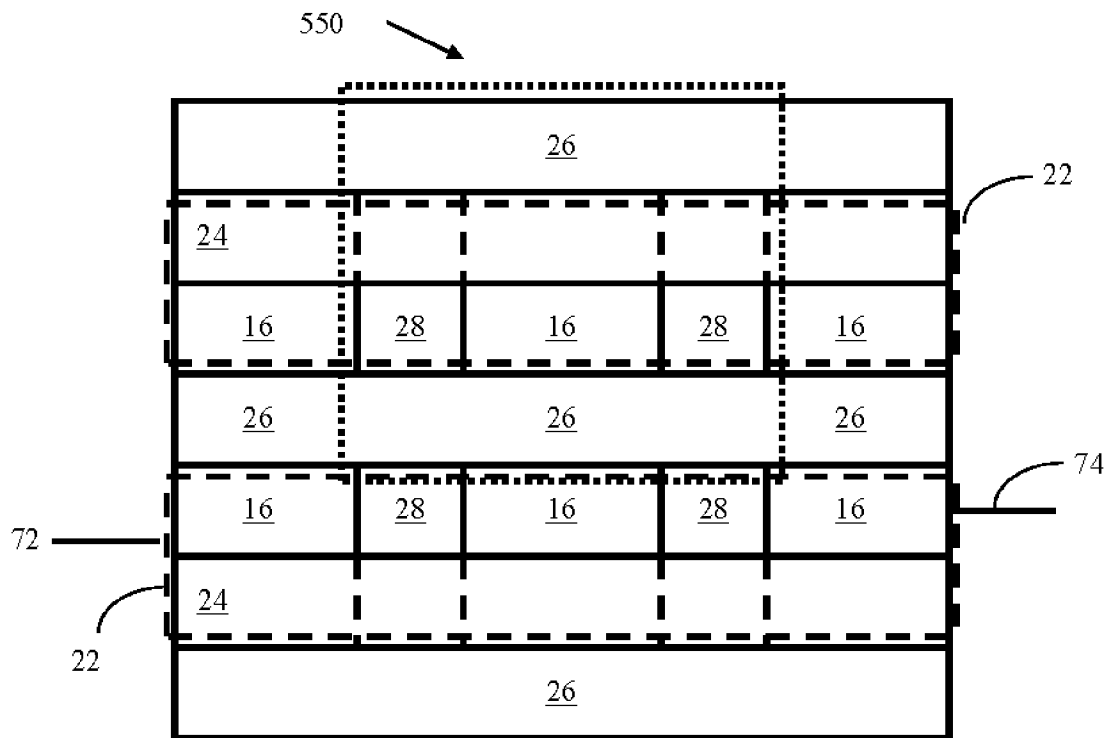


FIG. 77A

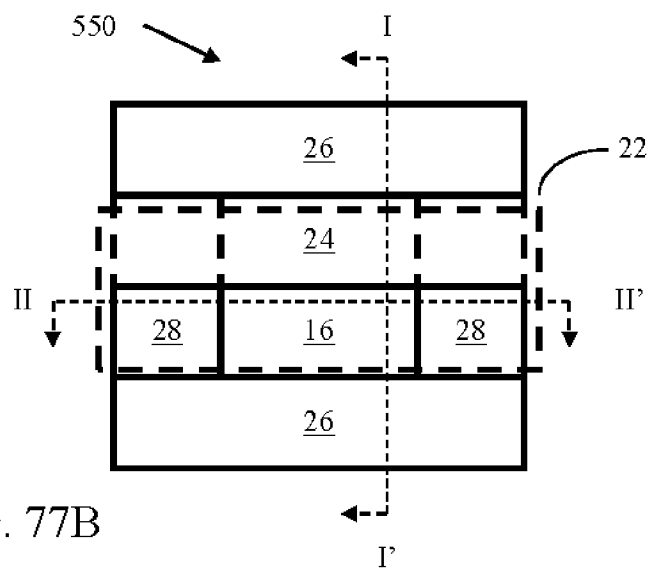


FIG. 77B

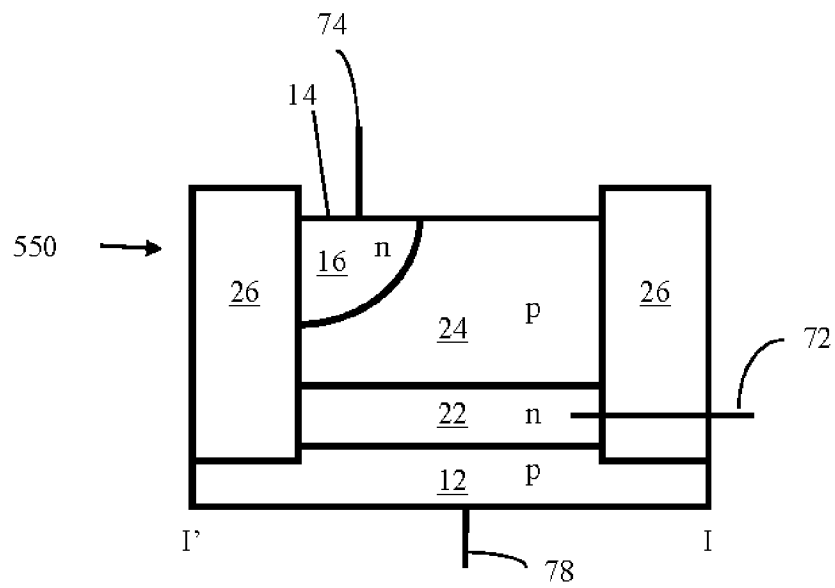


FIG. 77C

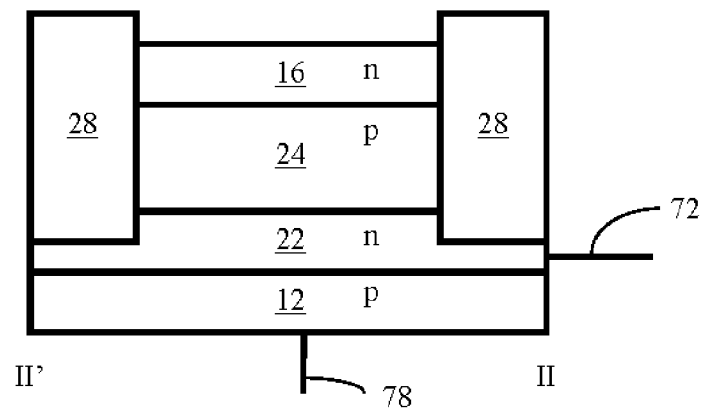


FIG. 77D

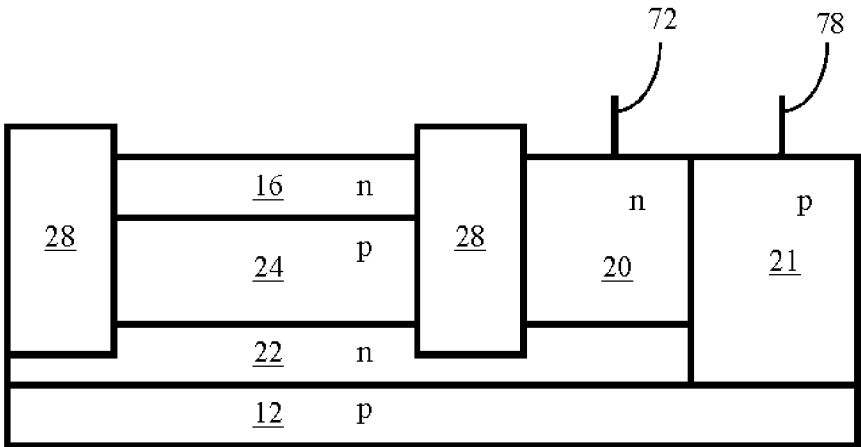


FIG. 77E

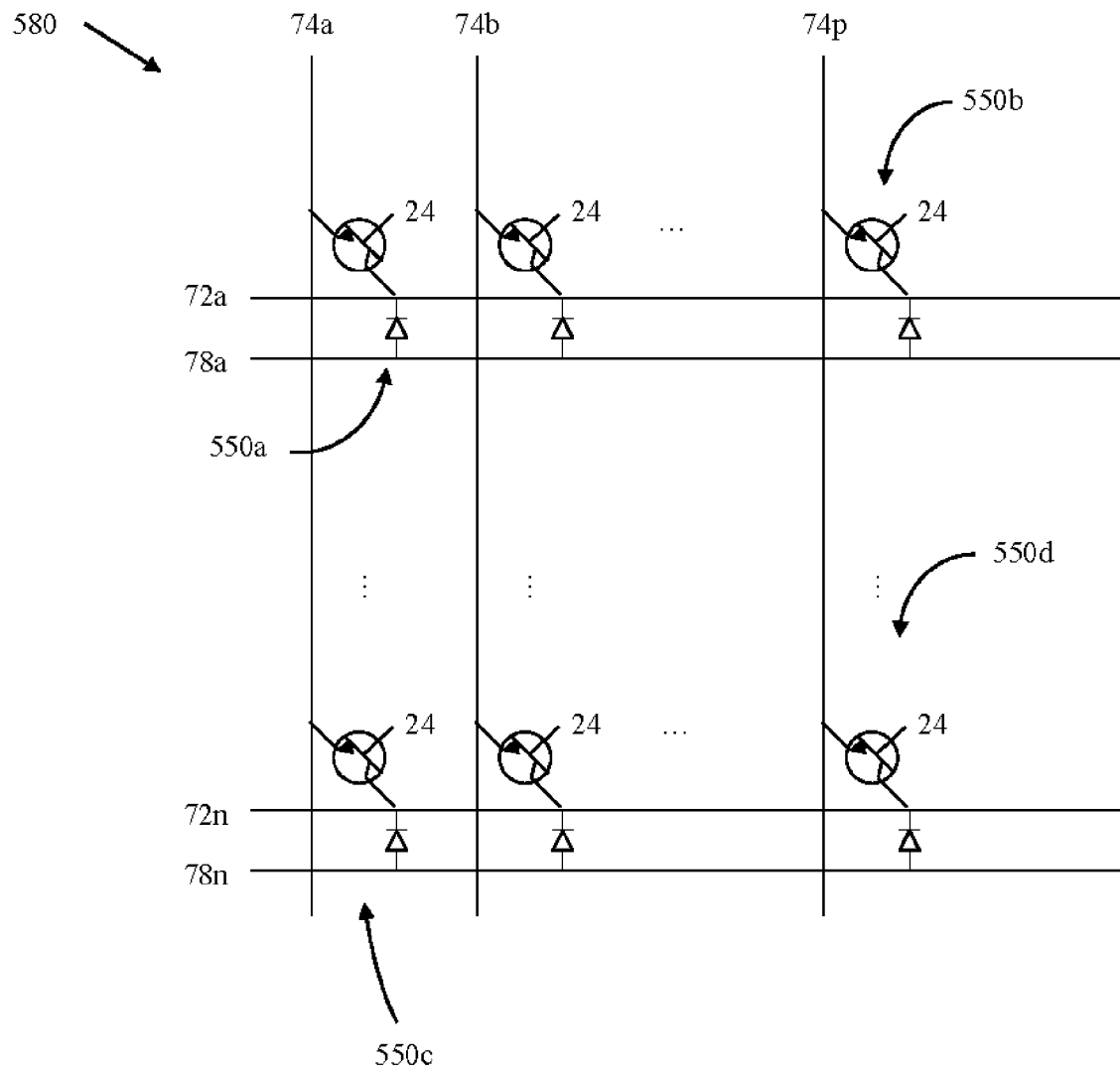


FIG. 77F

Array Hold Operation
(Memory Cells 550a, 550b, 550c and 550d)

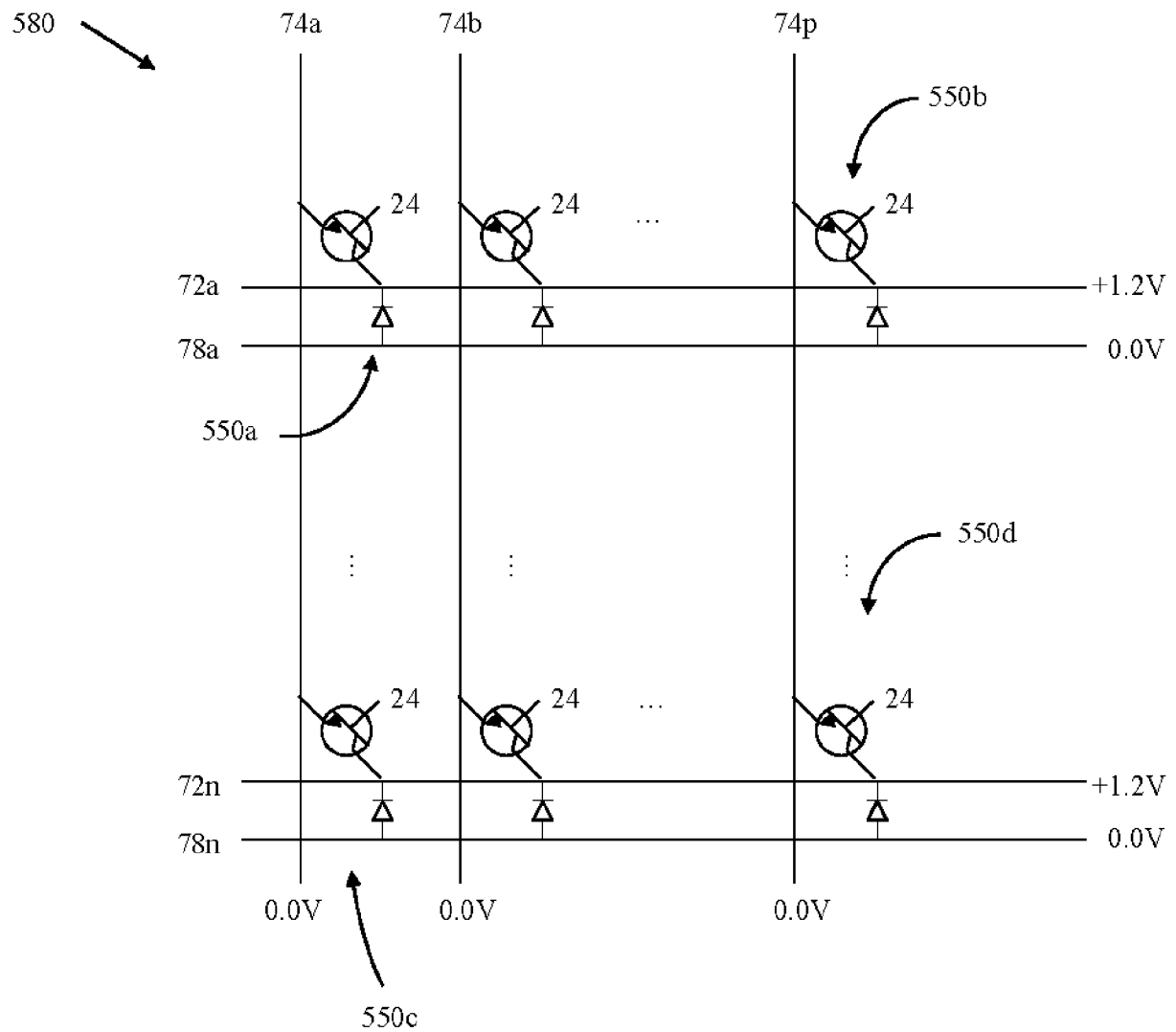


FIG. 78A

Row Hold Operation (Memory Cells 550a and 550b)

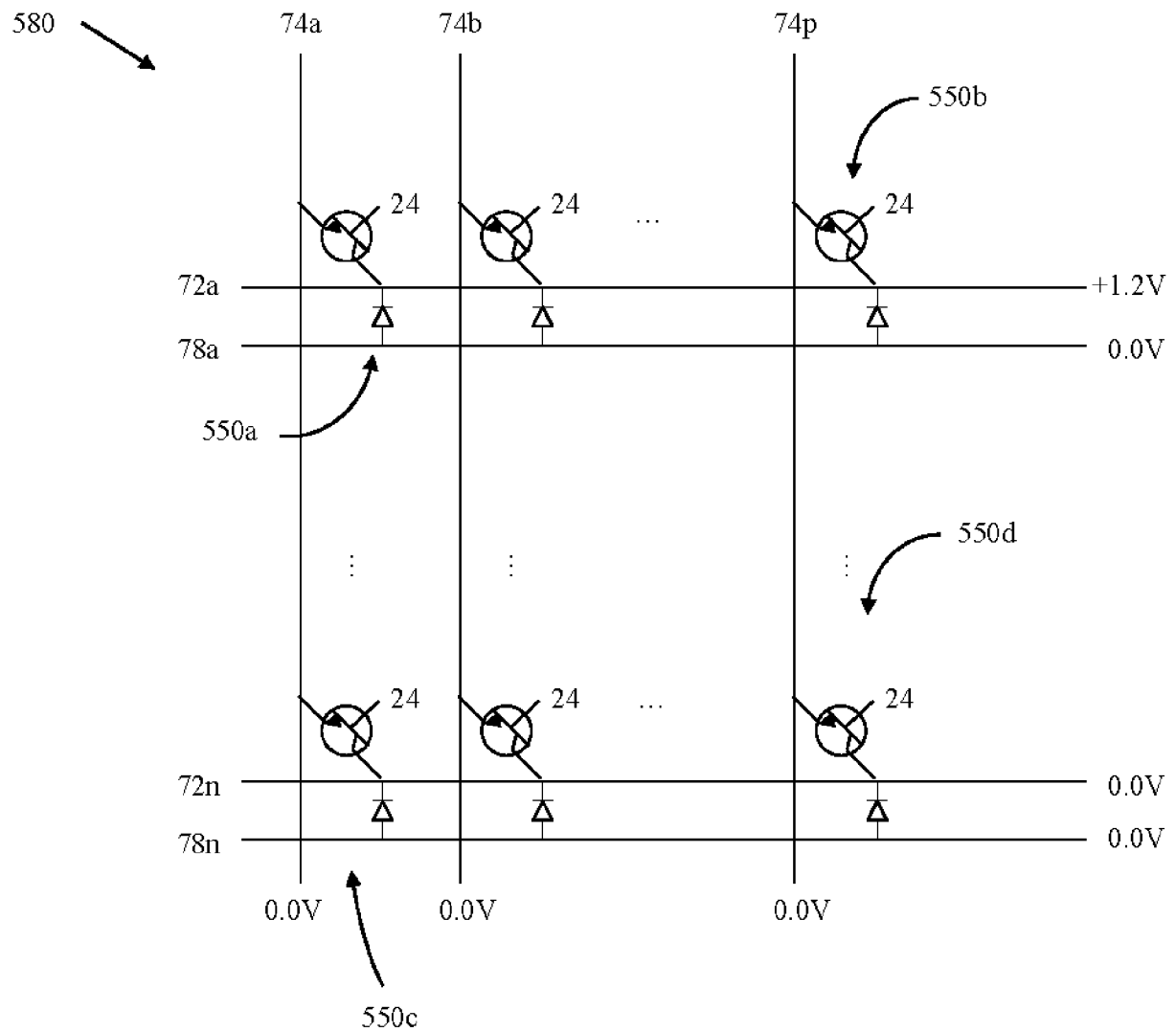


FIG. 78B

Read Operation (Single Memory Cell 550a)

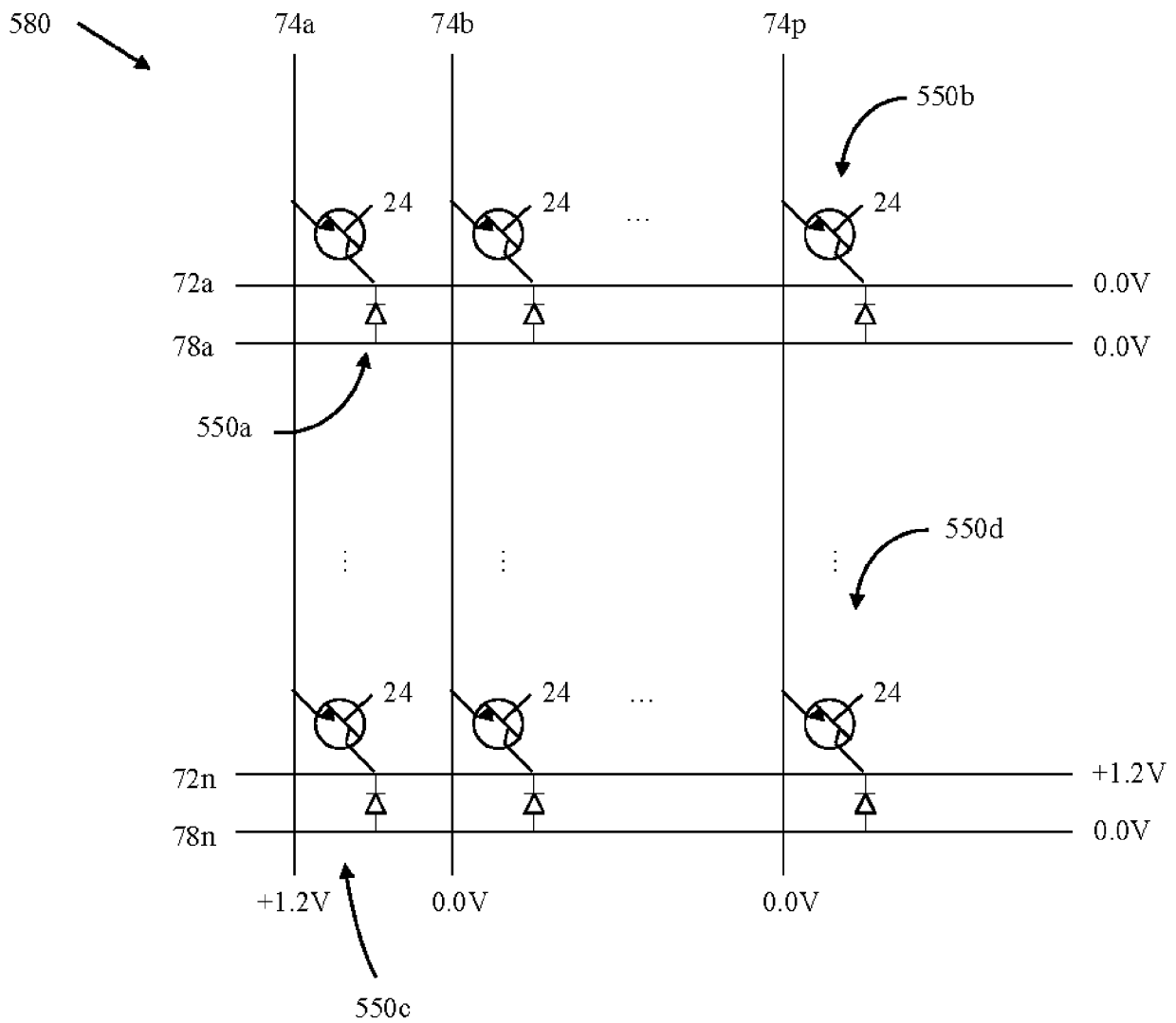


FIG. 79

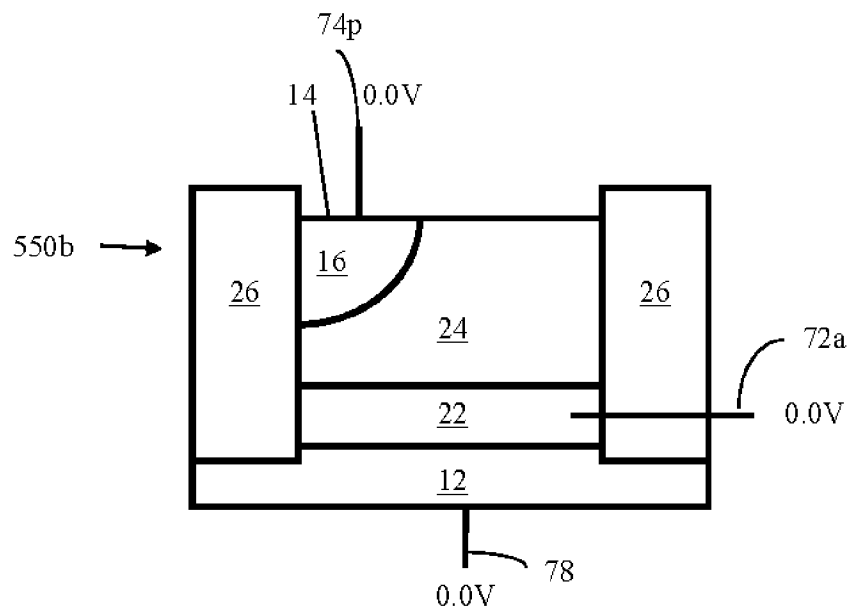


FIG. 80C

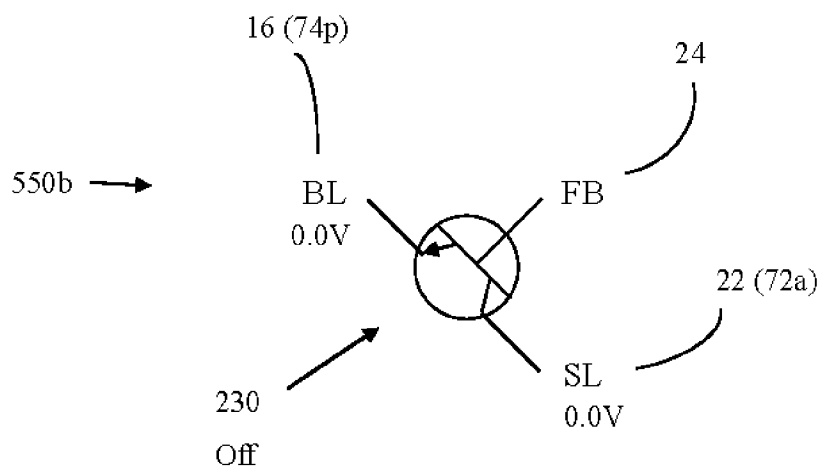


FIG. 80D

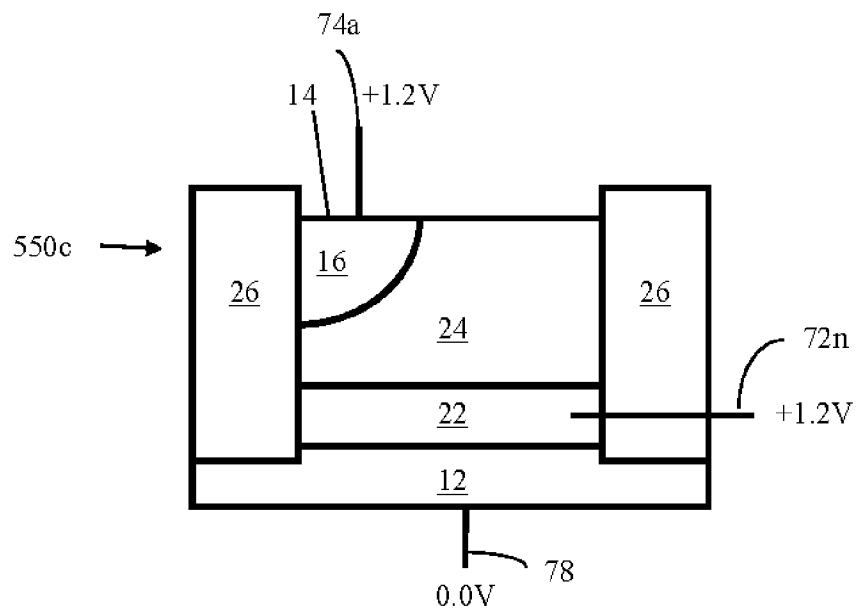


FIG. 80E

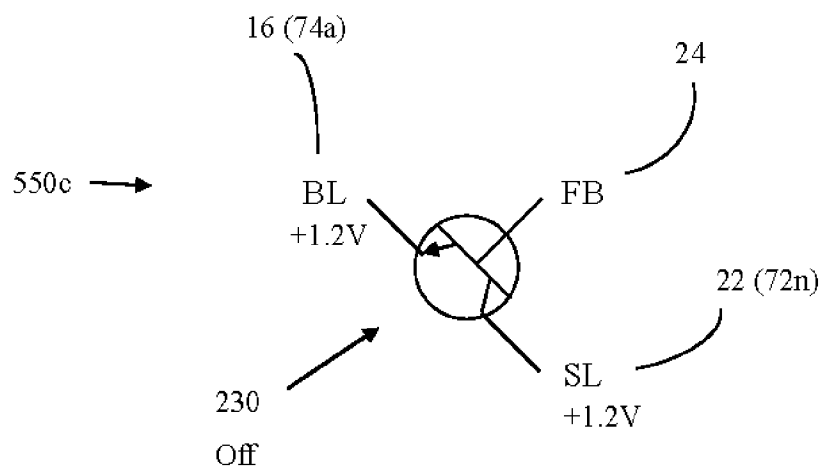


FIG. 80F

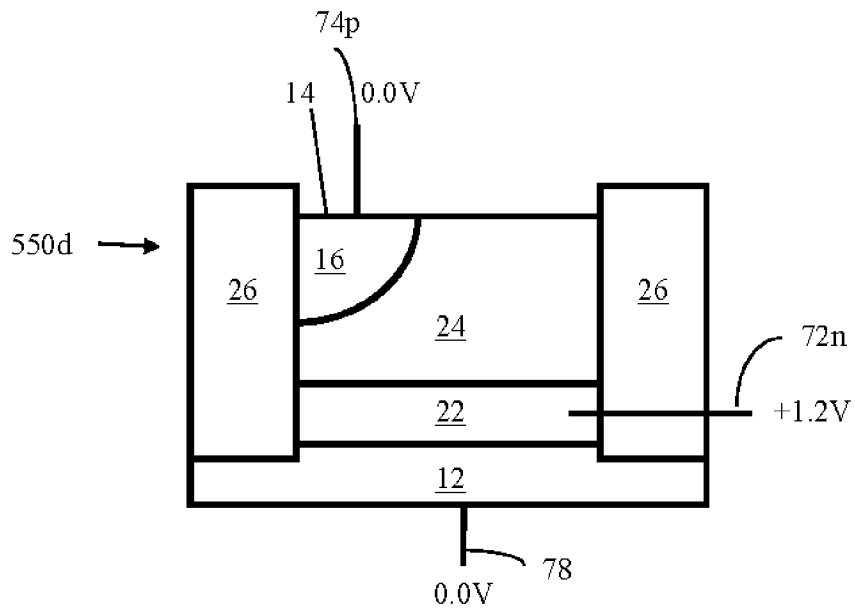


FIG. 80G

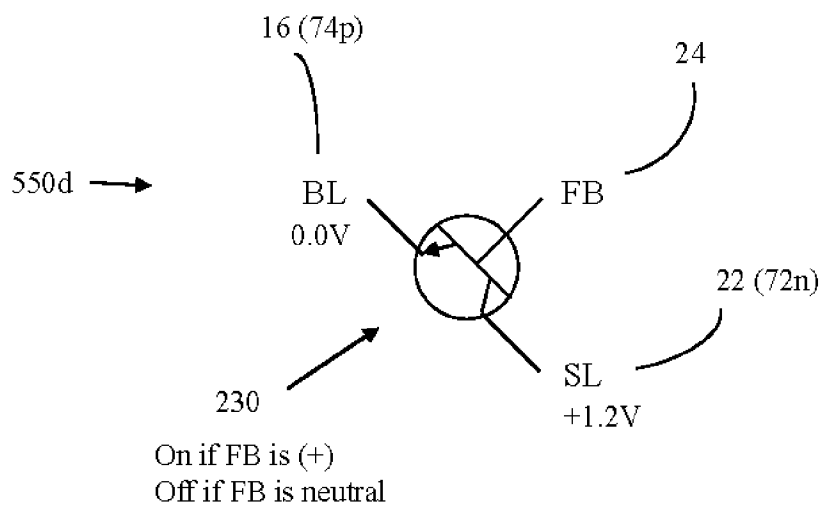


FIG. 80H

Singe Row Write Logic-0 Operation (Memory Cells 550a and 550b)

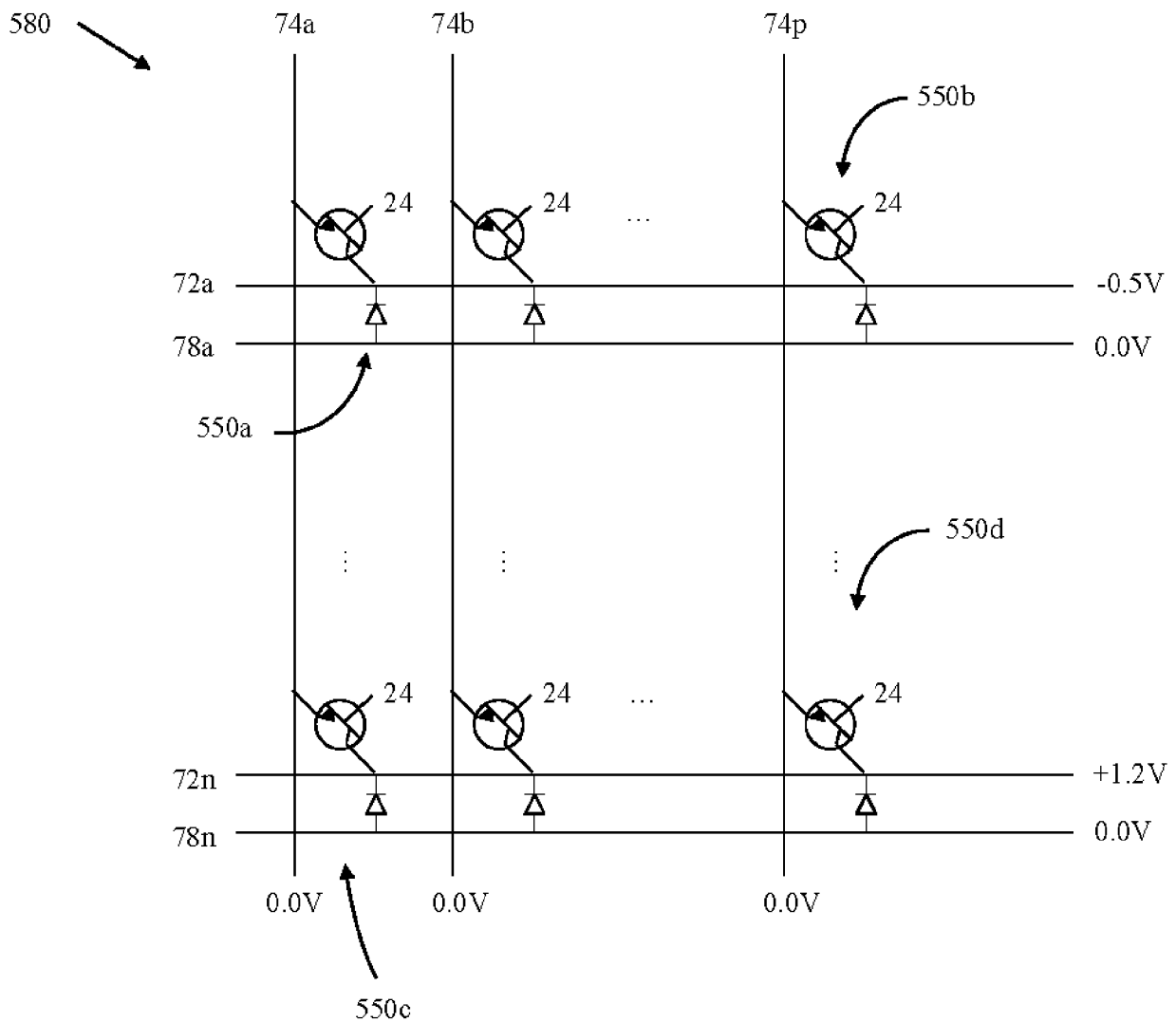


FIG. 81

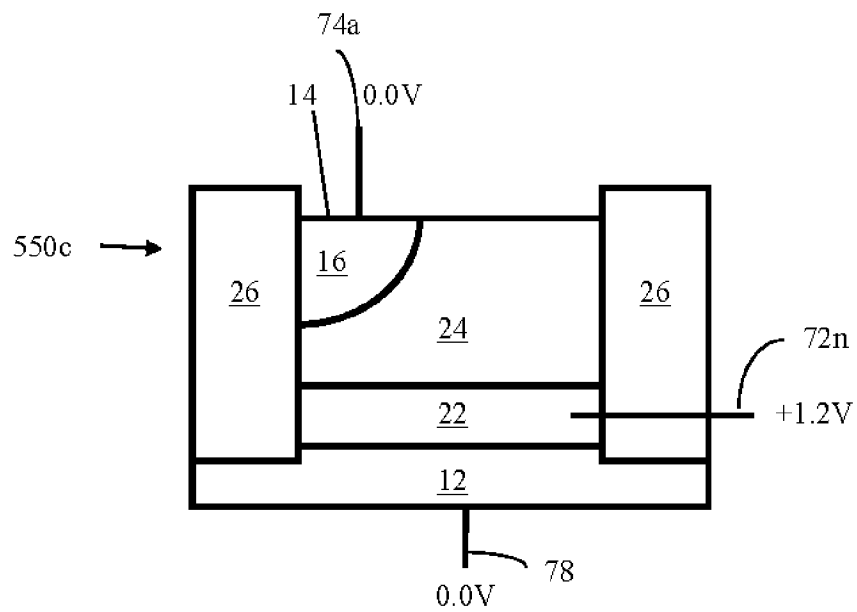


FIG. 82A

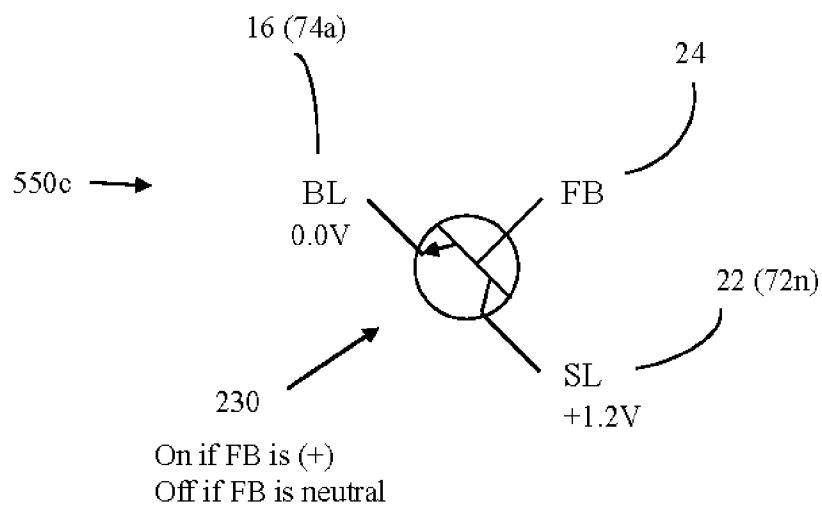


FIG. 82B

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 550a)

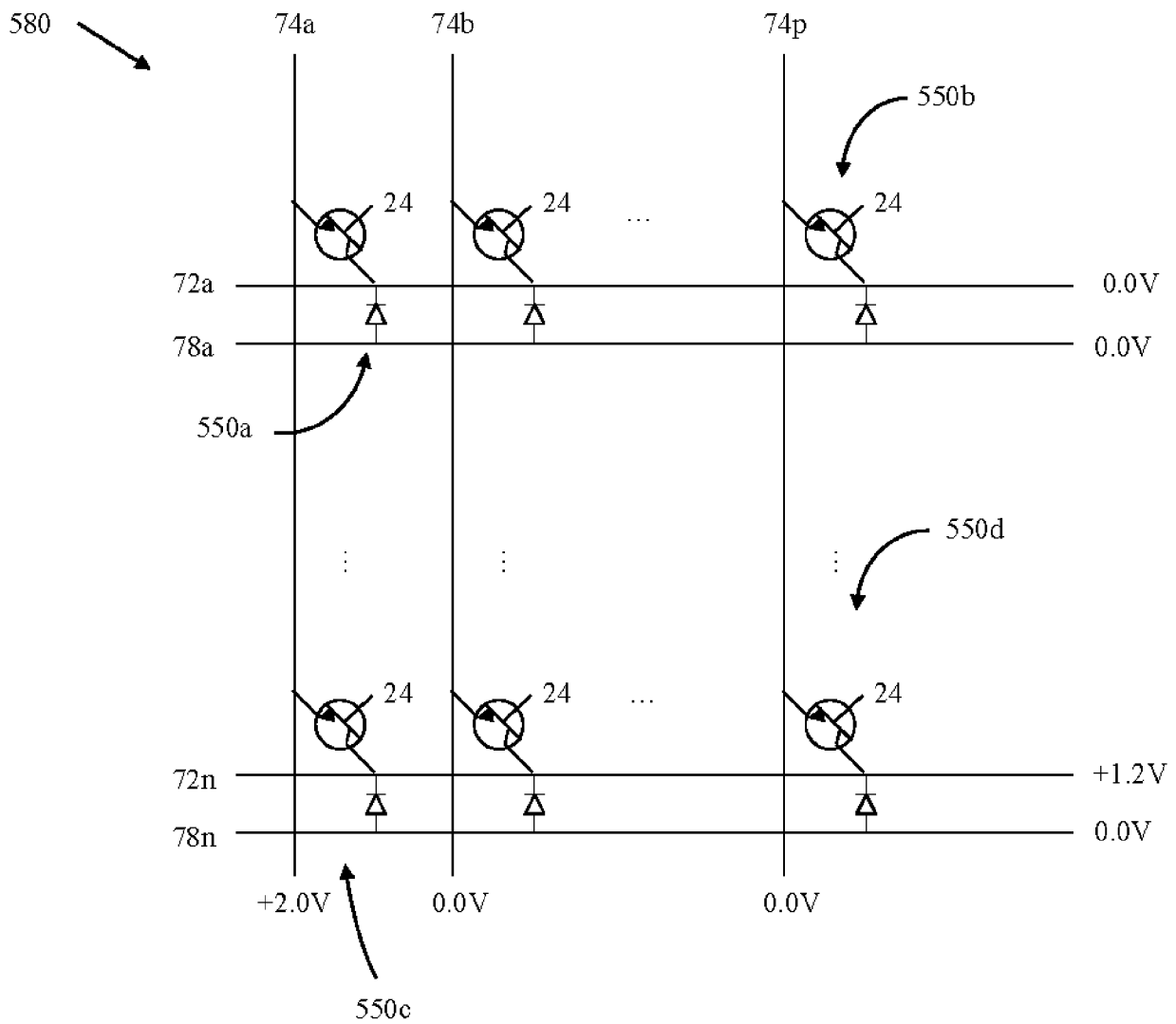


FIG. 83

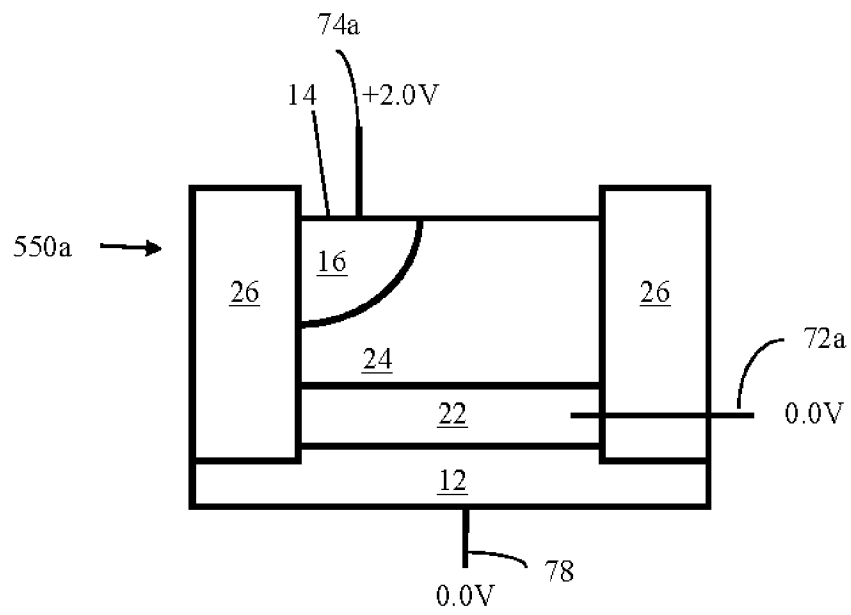


FIG. 84A

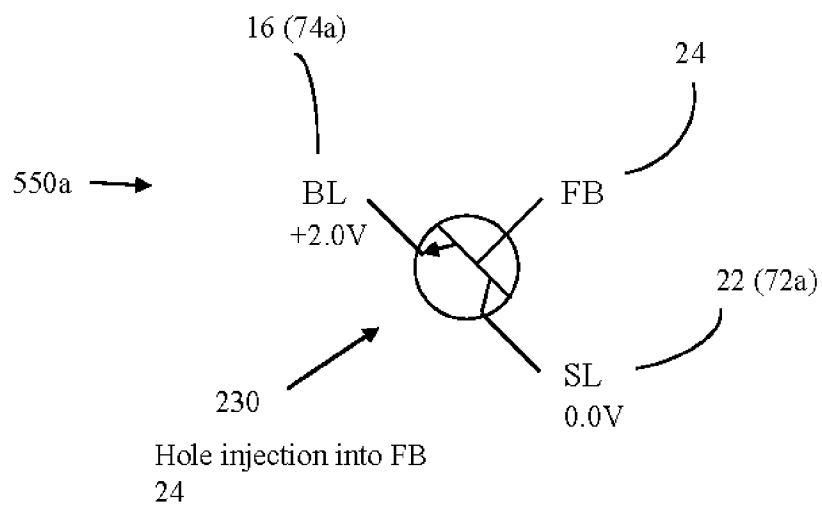


FIG. 84B

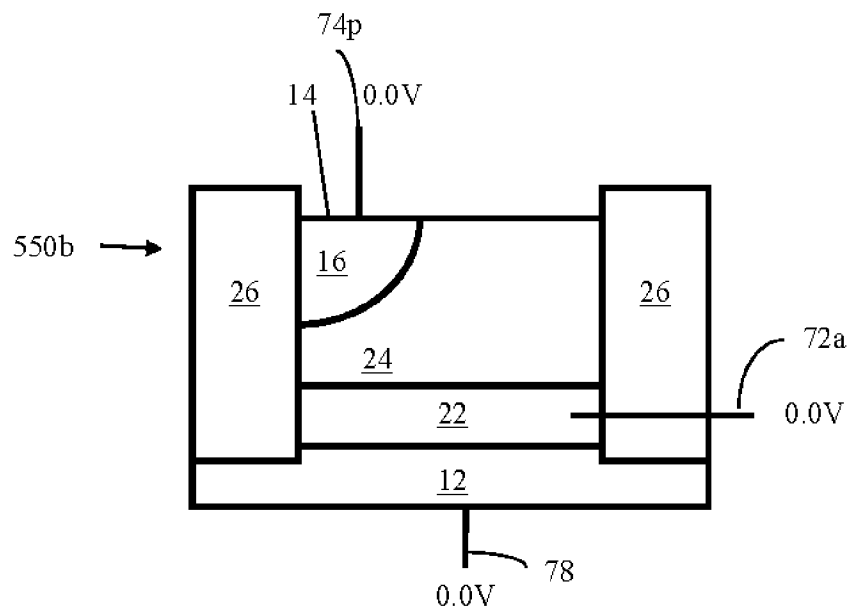


FIG. 84C

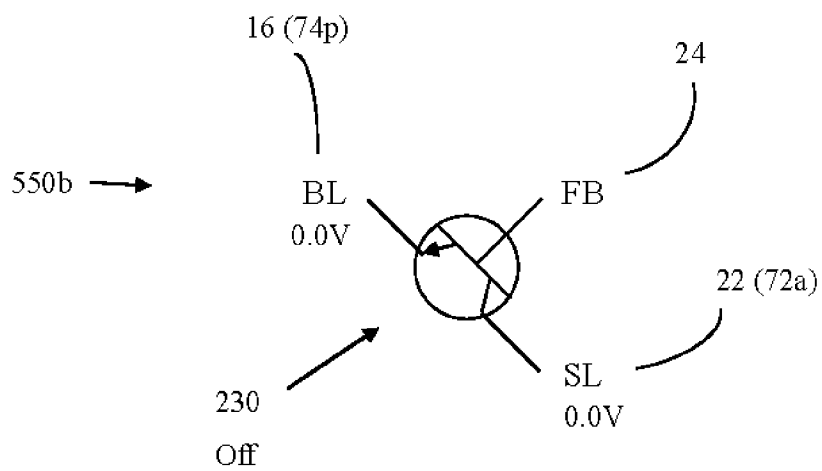


FIG. 84D

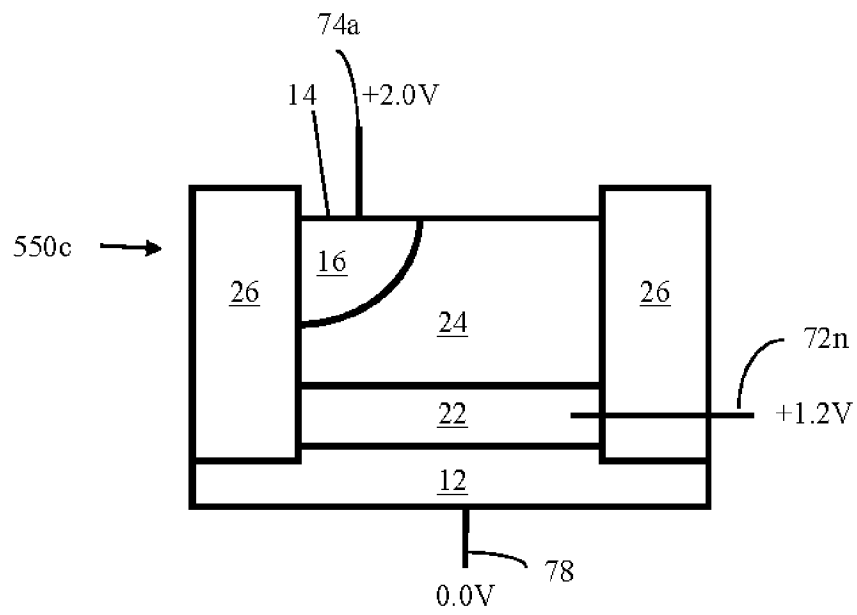


FIG. 84E

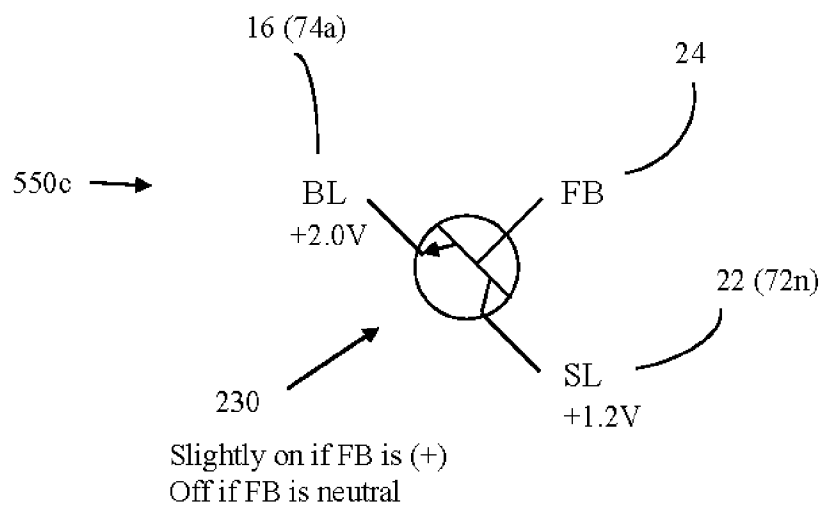


FIG. 84F

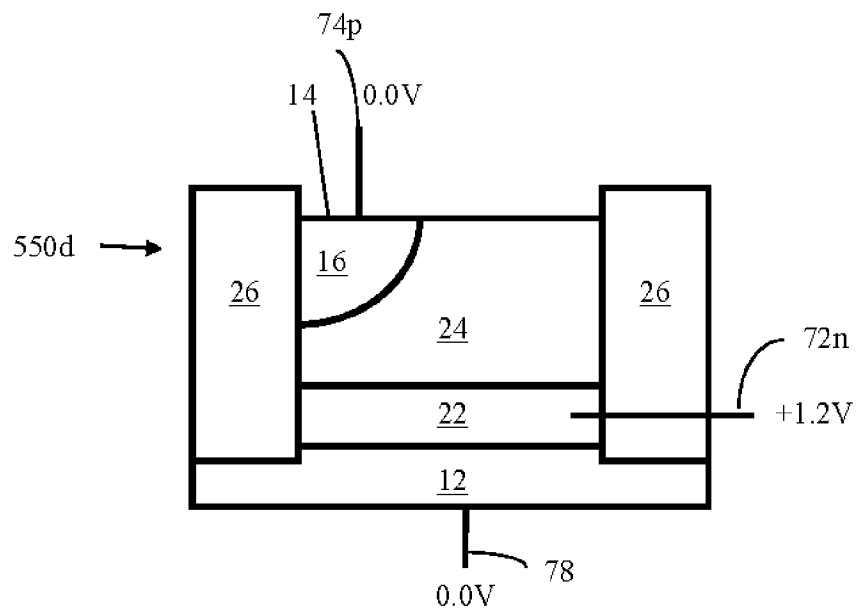


FIG. 84G

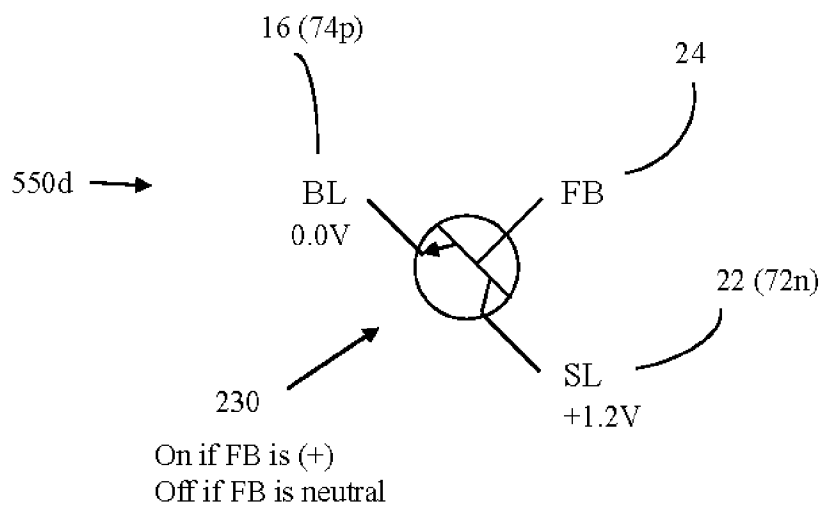


FIG. 84H

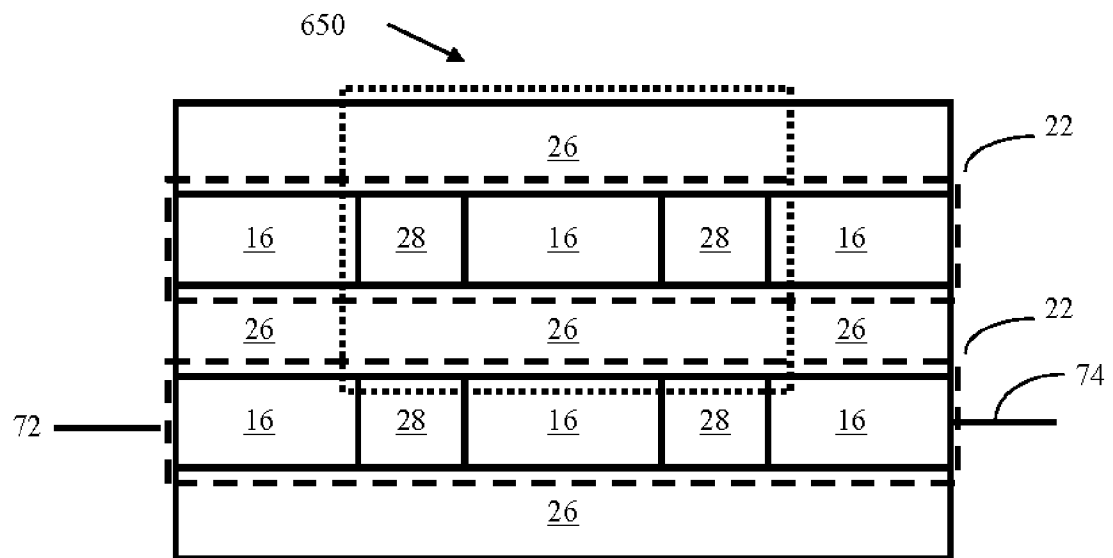


FIG. 85A

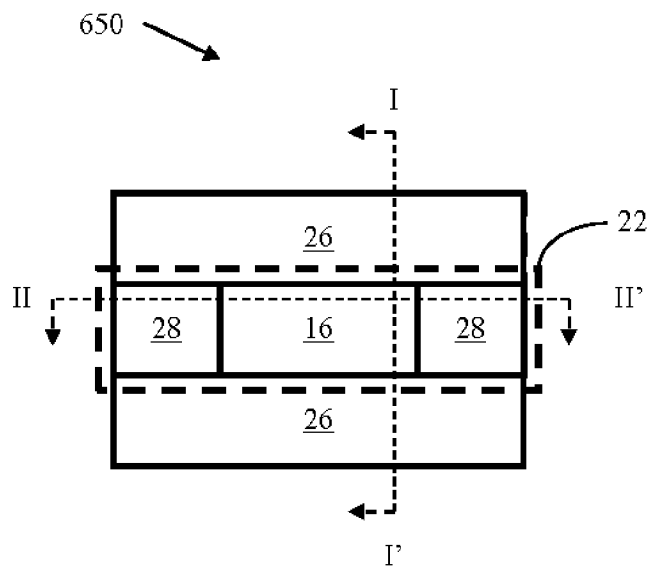


FIG. 85B

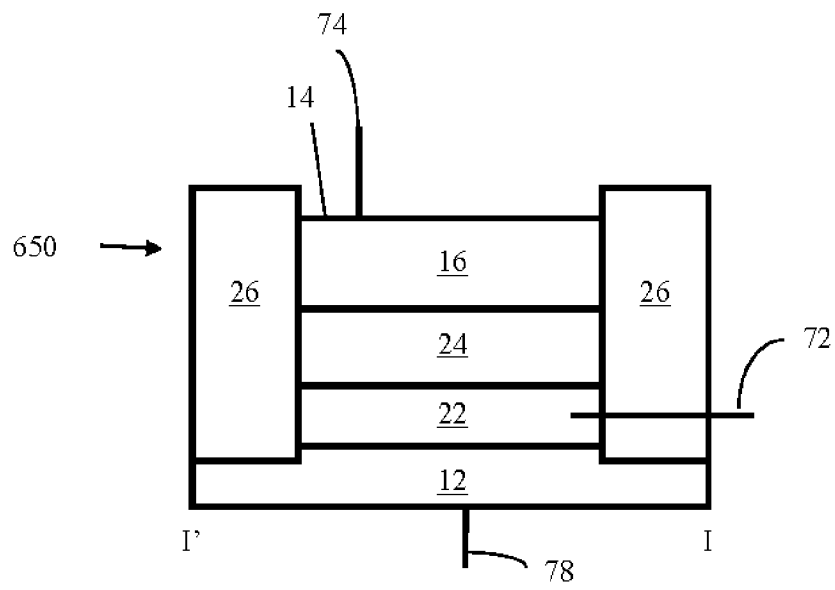


FIG. 85C

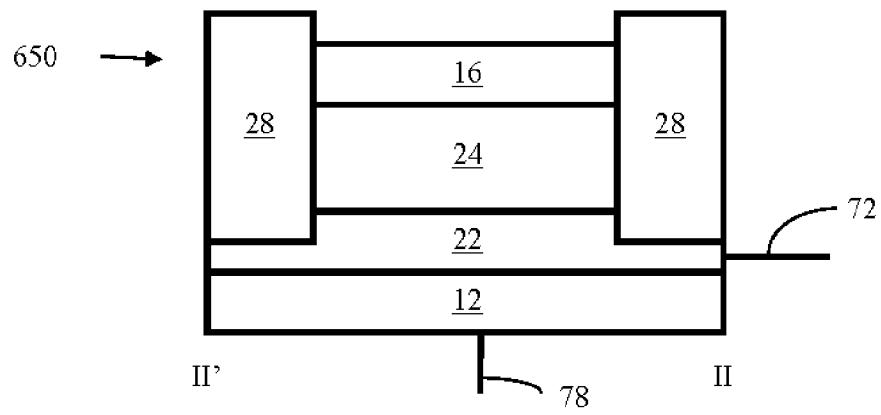


FIG. 85D

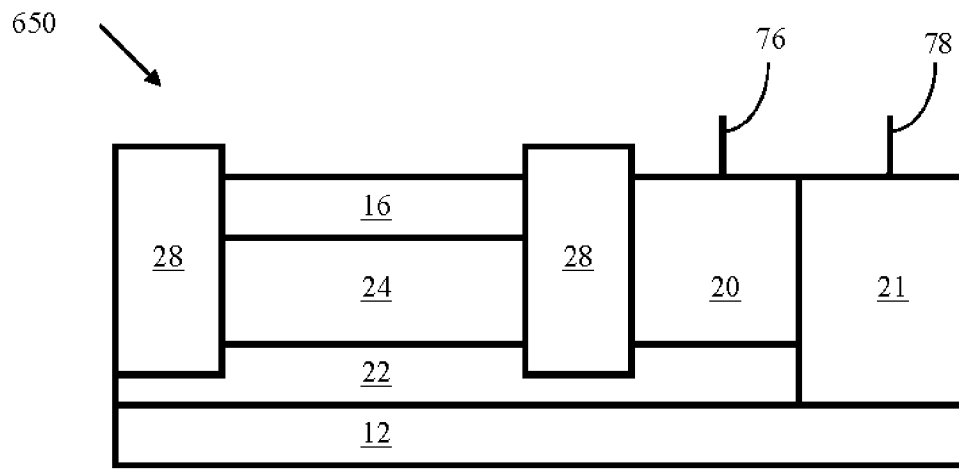


FIG. 85E

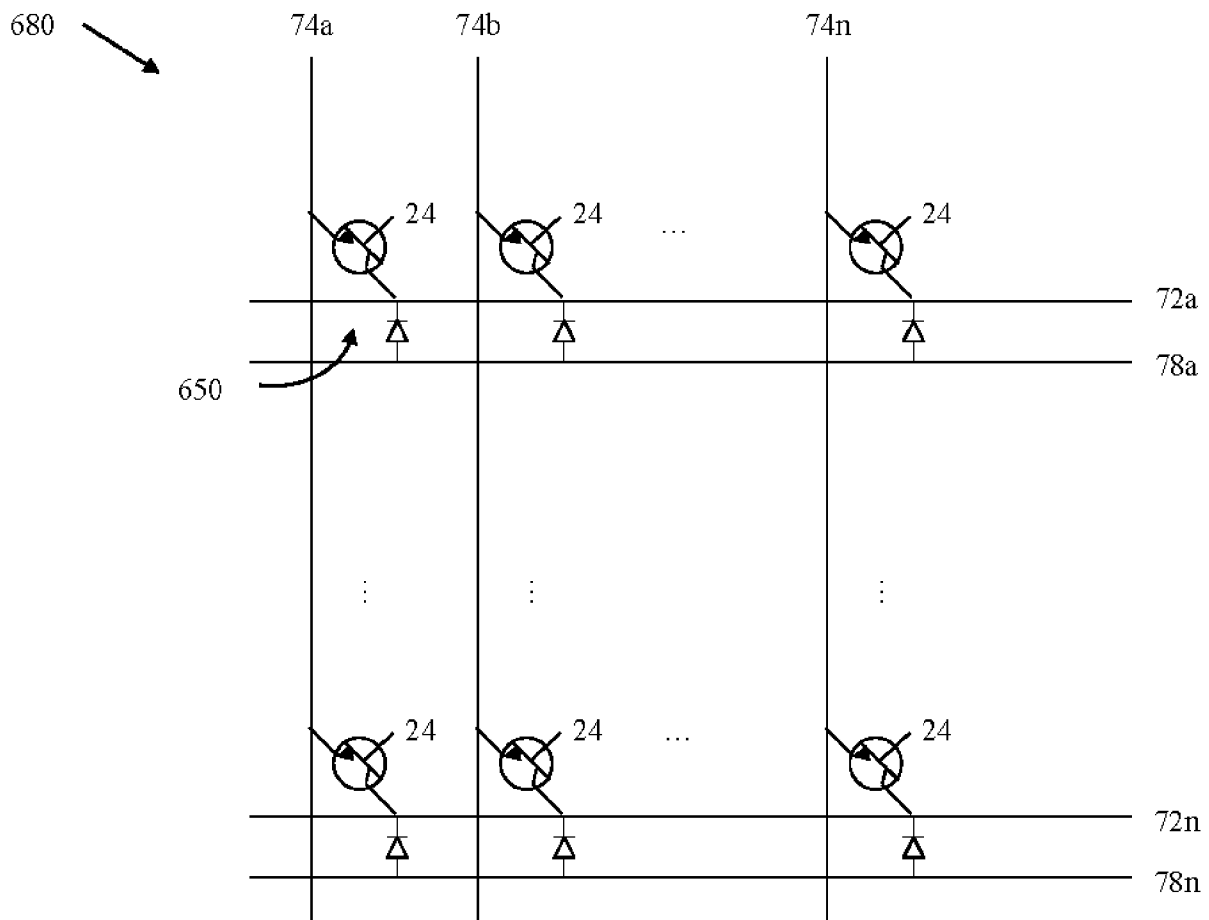


FIG. 85F

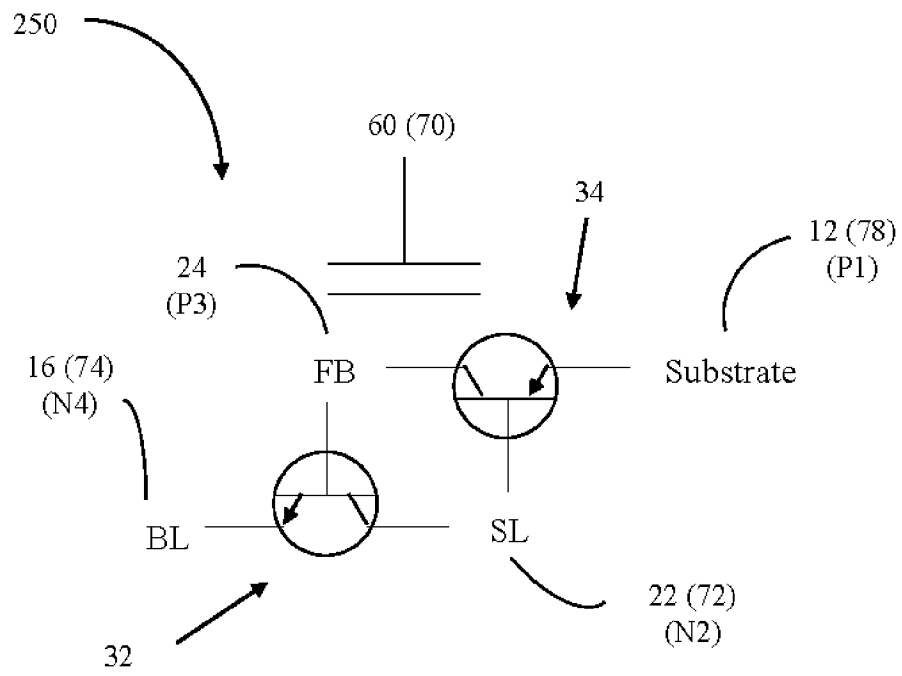


FIG. 86

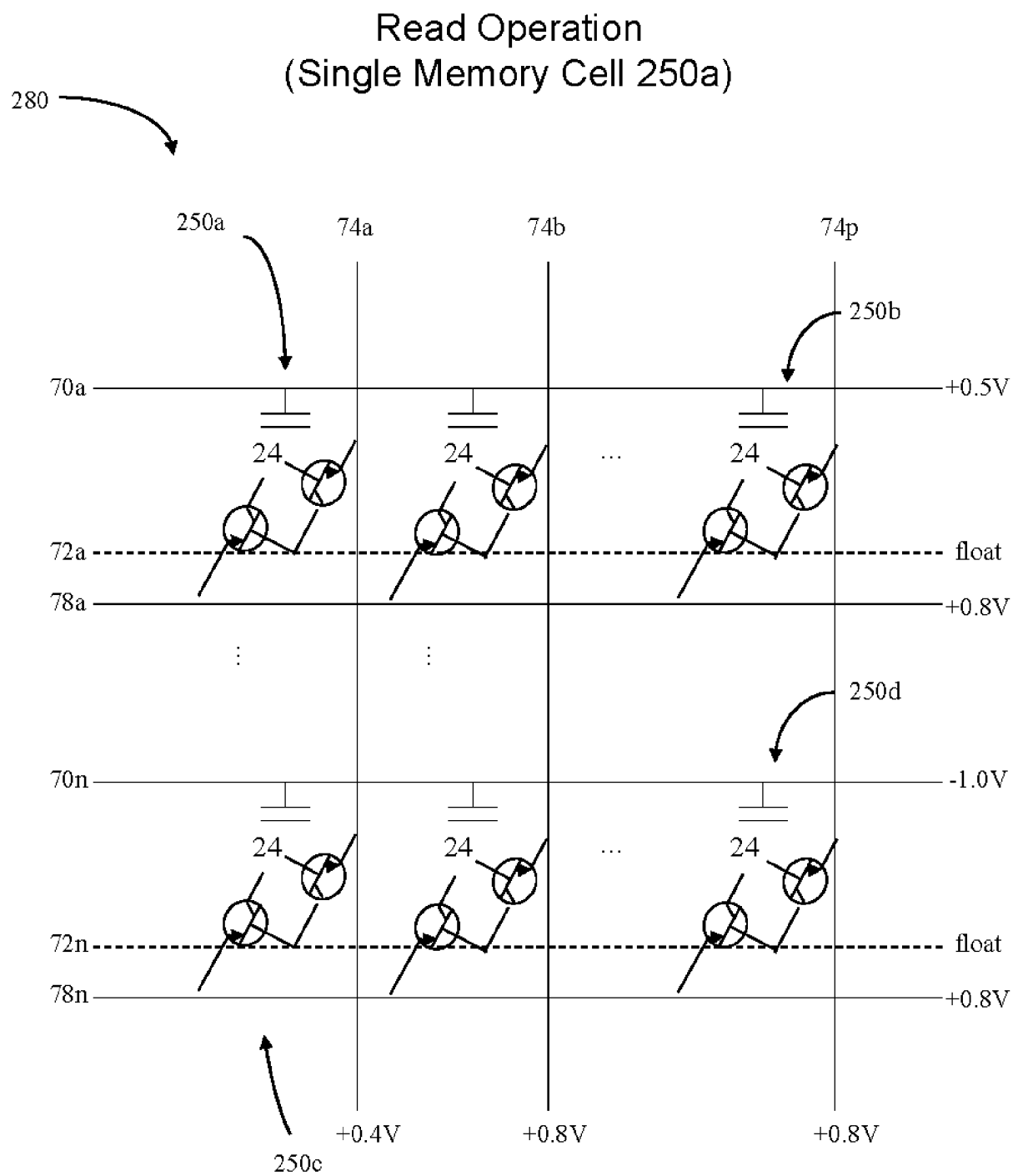


FIG. 87

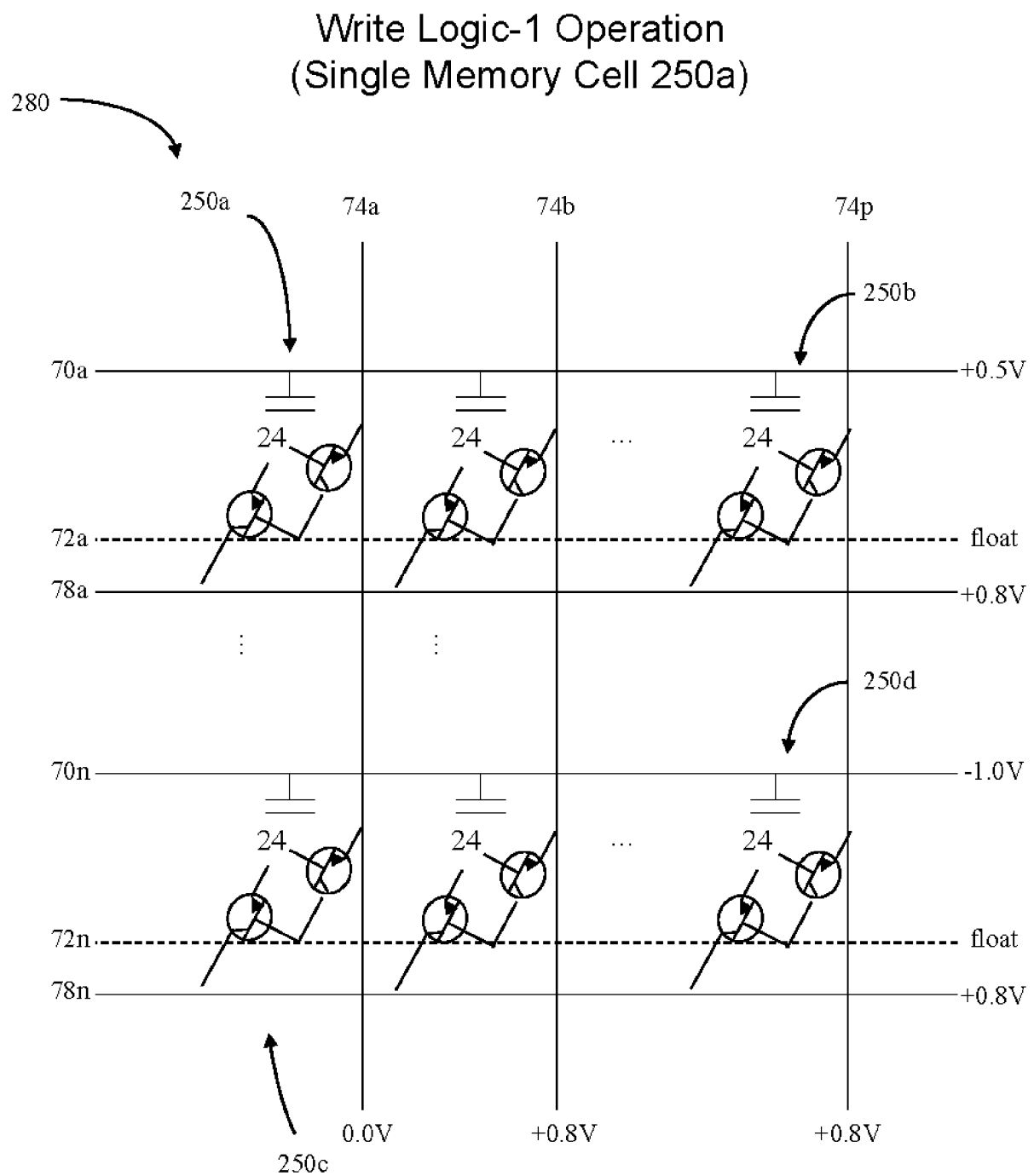


FIG. 88

Write Logic-0 Operation
(Single Memory Cell 250a)

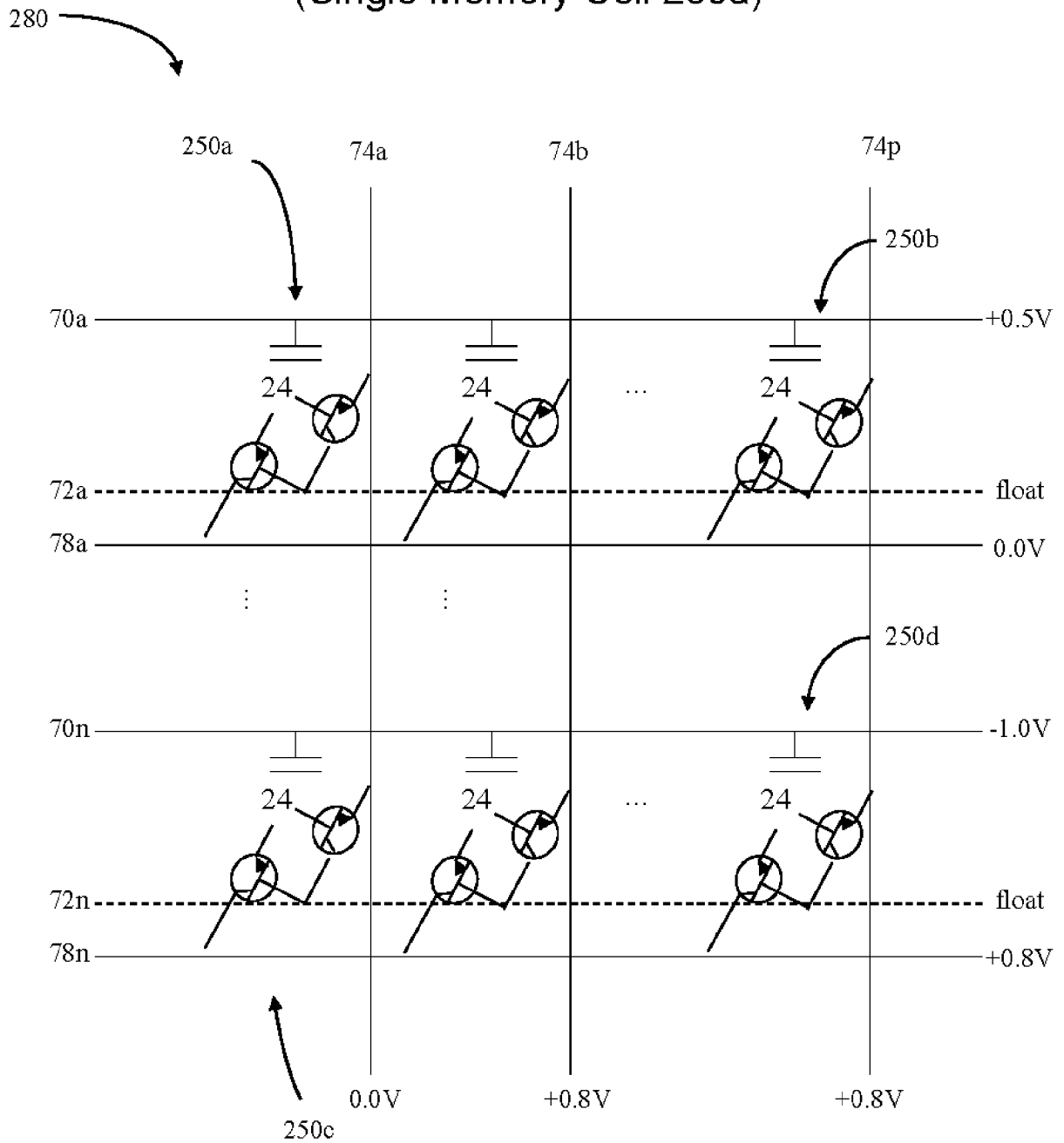


FIG. 89

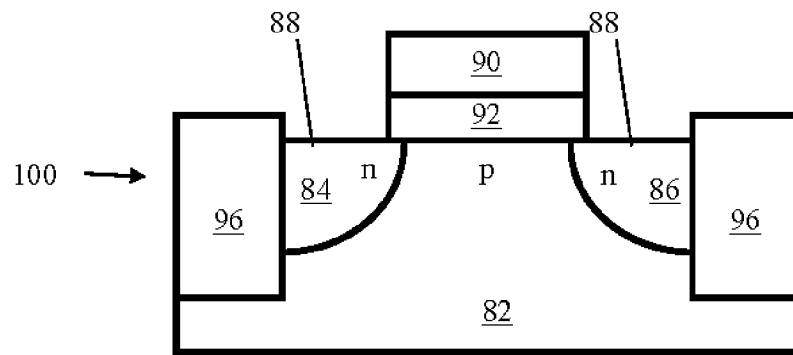


FIG. 90A (Prior Art)

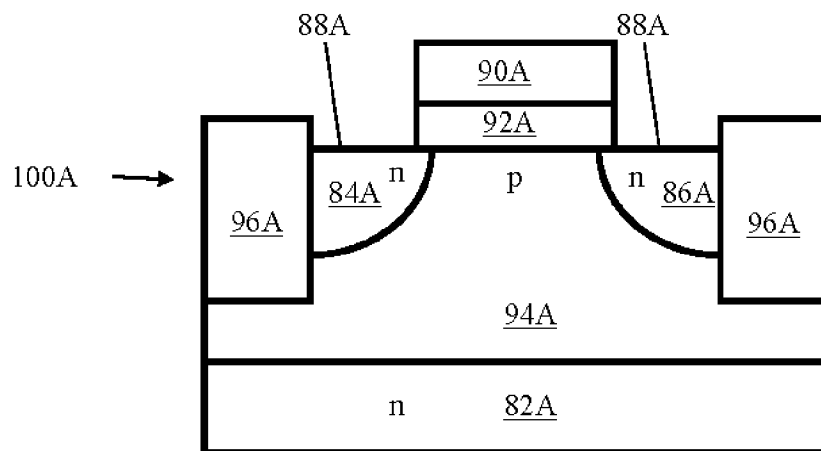


FIG. 90B (Prior Art)

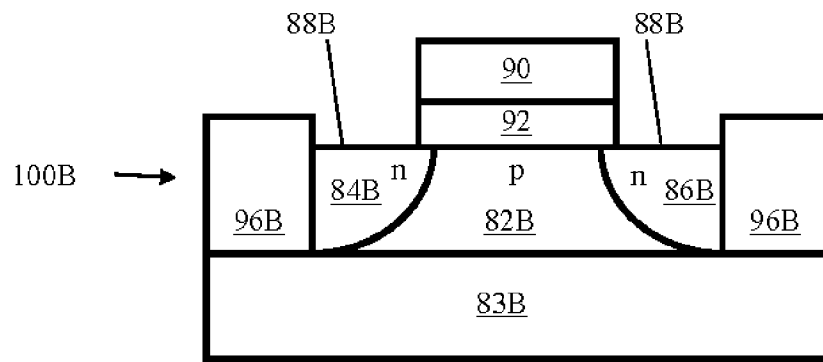


FIG. 90C (Prior Art)

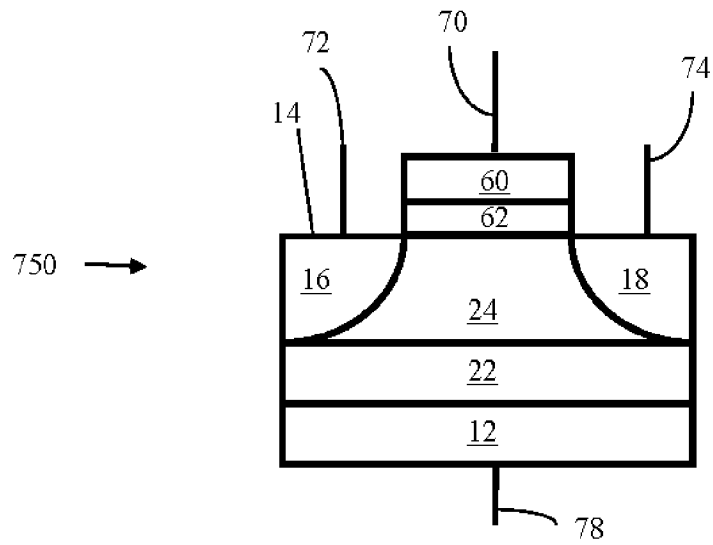


FIG. 91

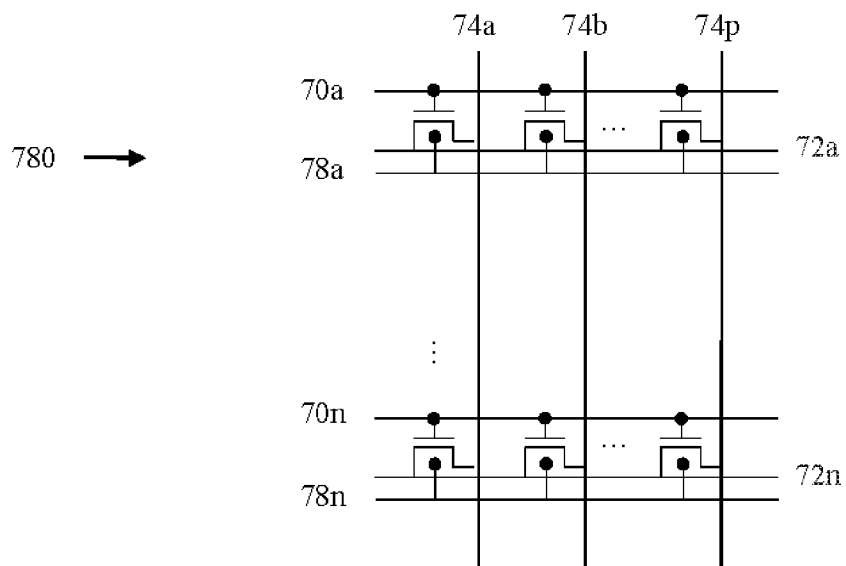


FIG. 92A

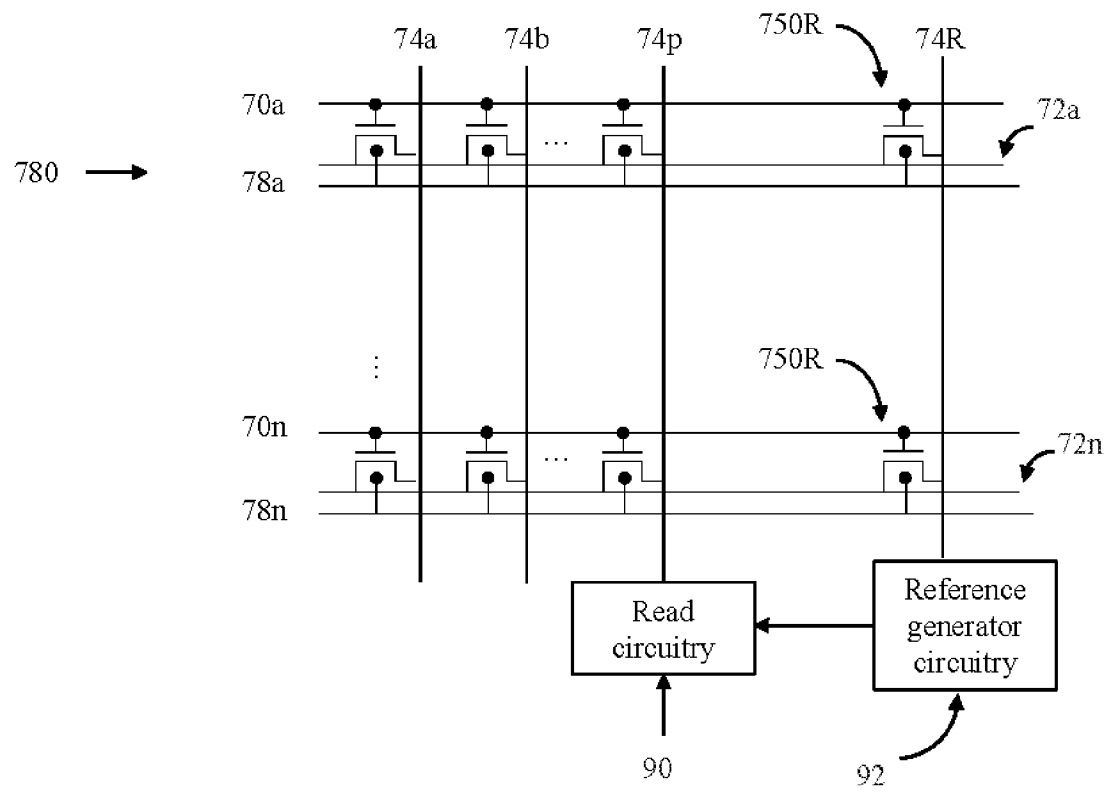


FIG. 92B

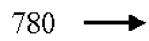


FIG. 93

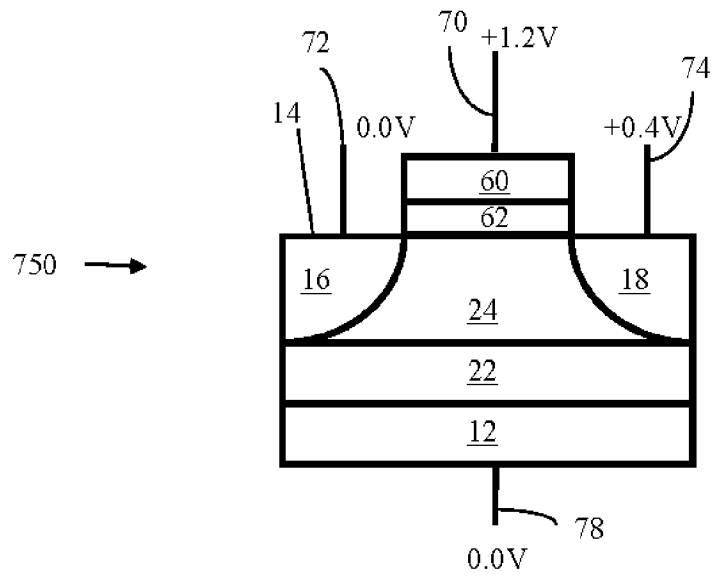


FIG. 94A

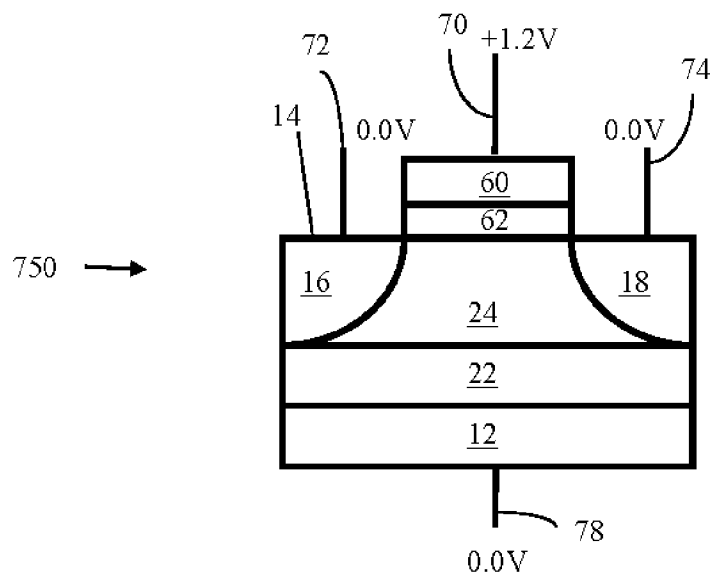


FIG. 94B

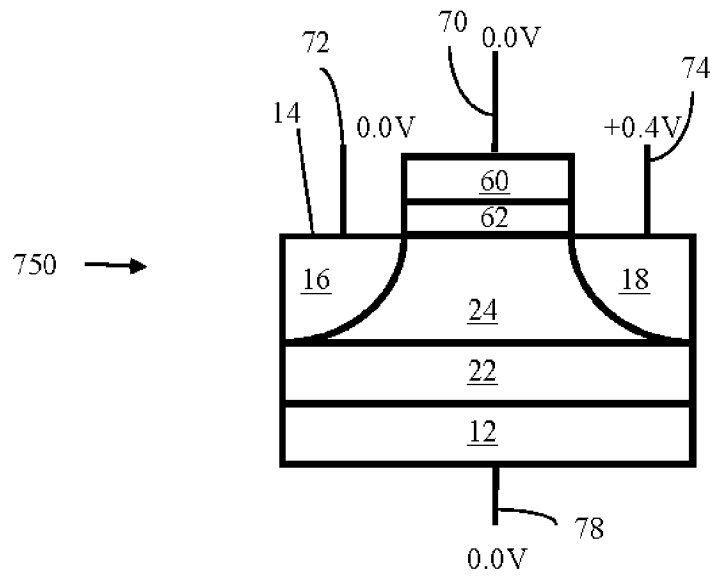


FIG. 94C

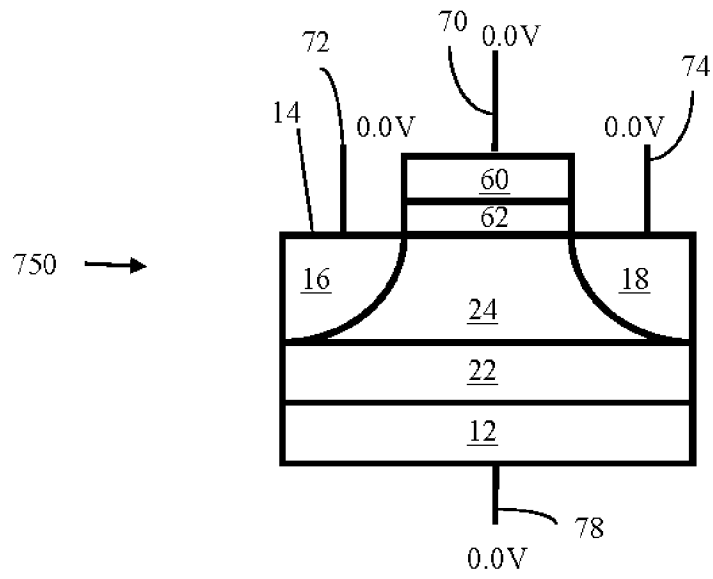


FIG. 94D

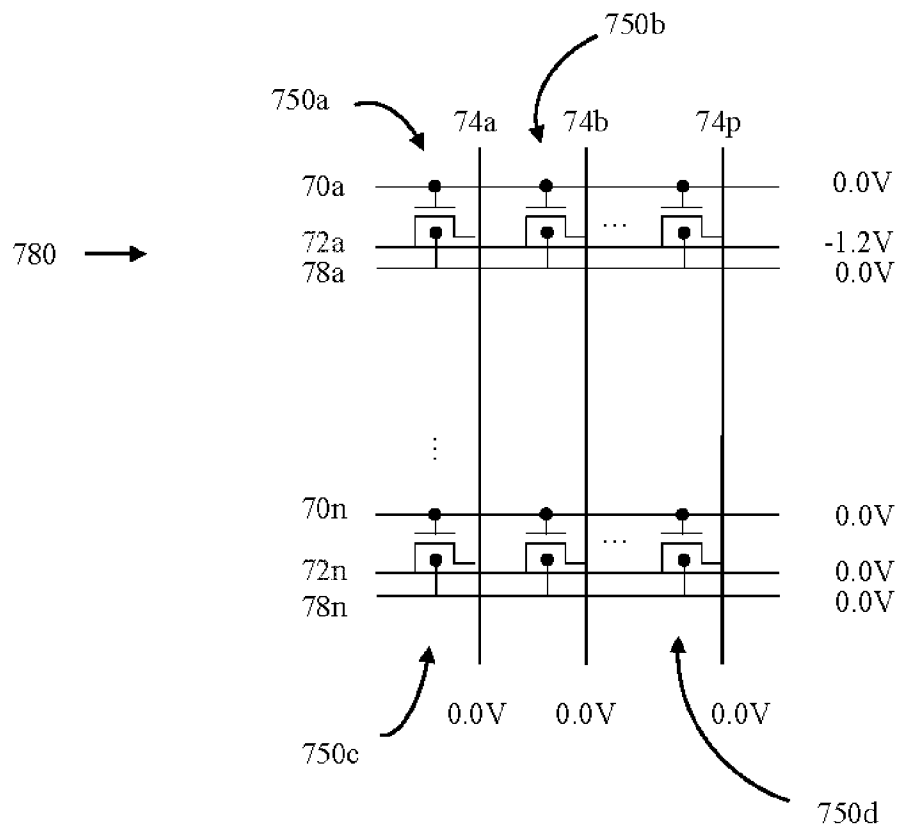


FIG. 95

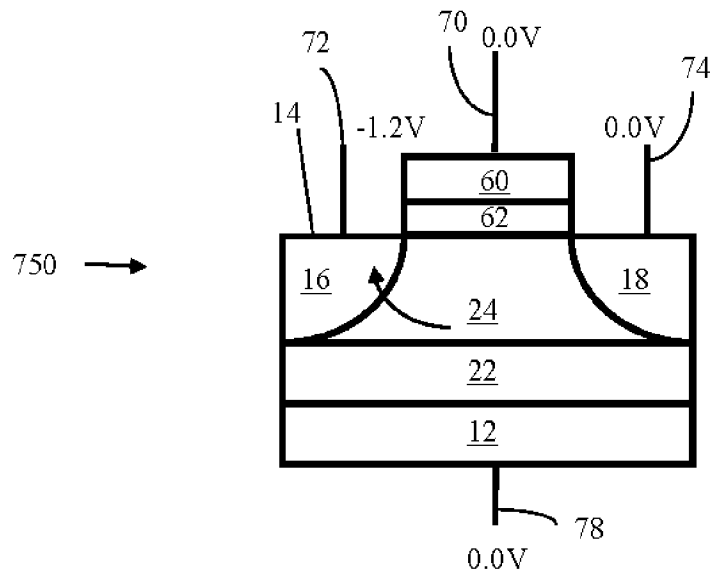


FIG. 96A

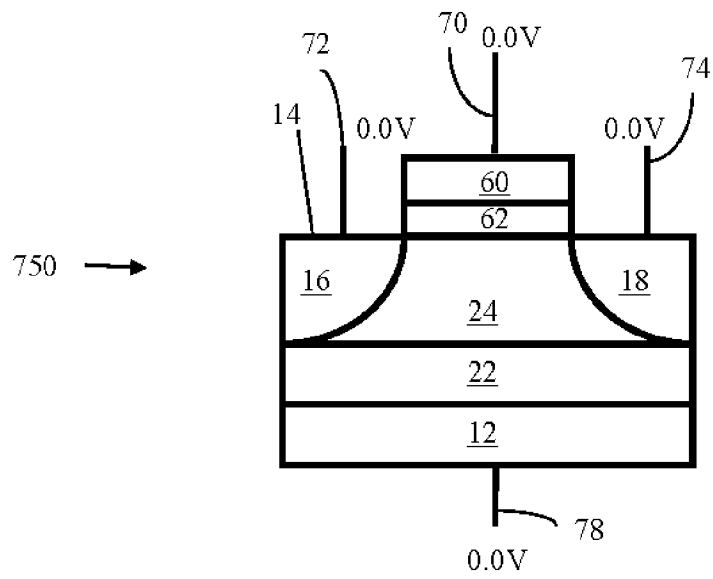


FIG. 96B

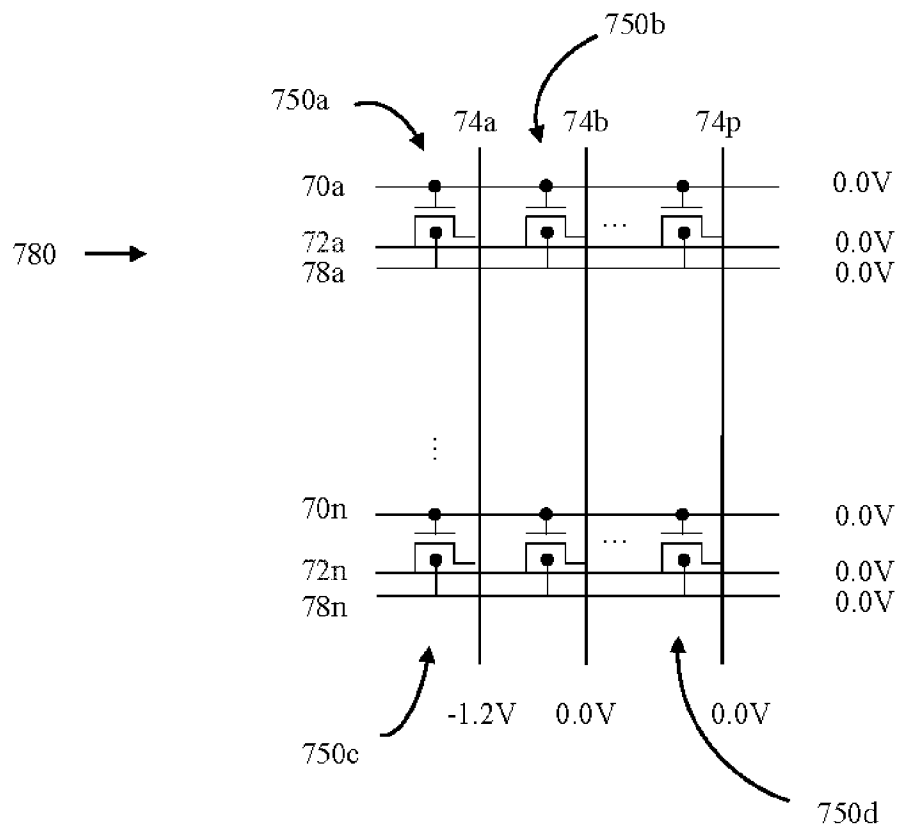


FIG. 97

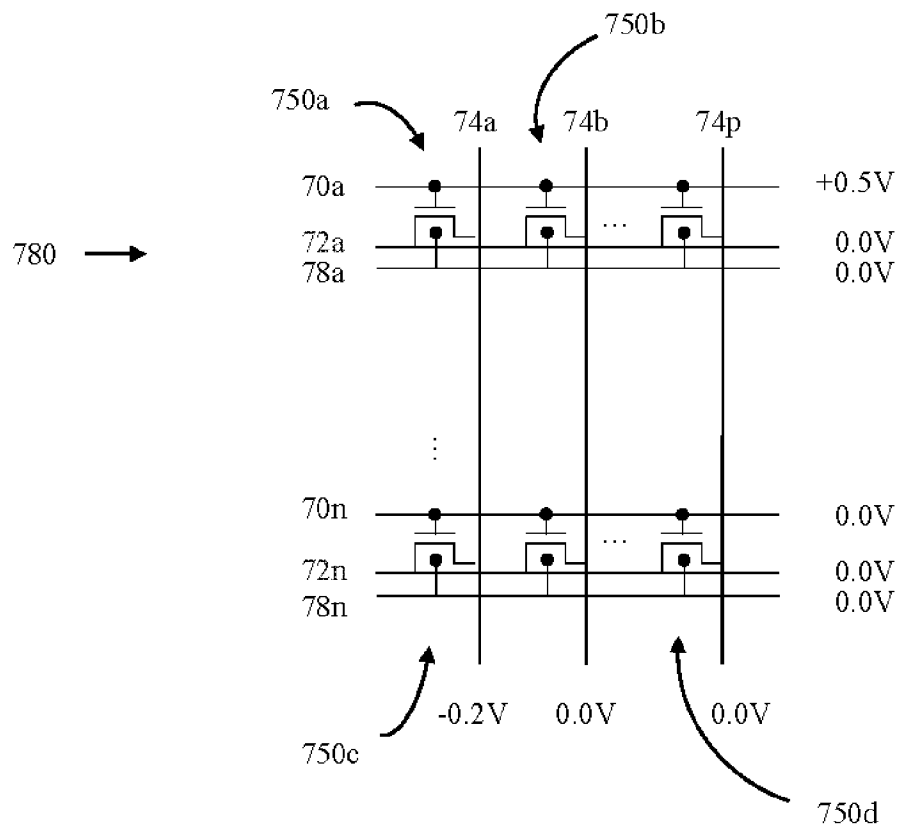


FIG. 98

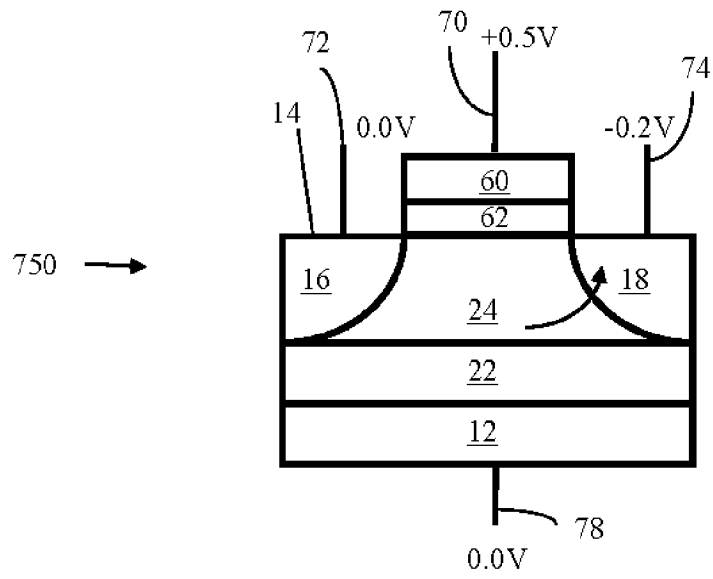


FIG. 99A

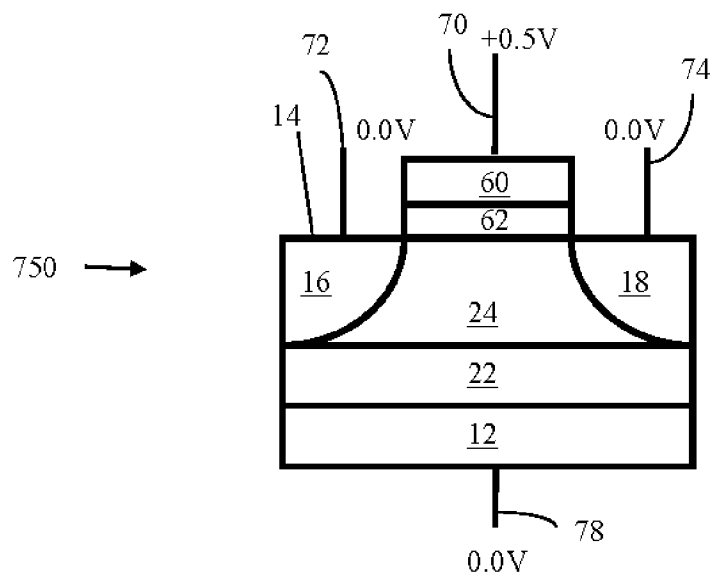


FIG. 99B

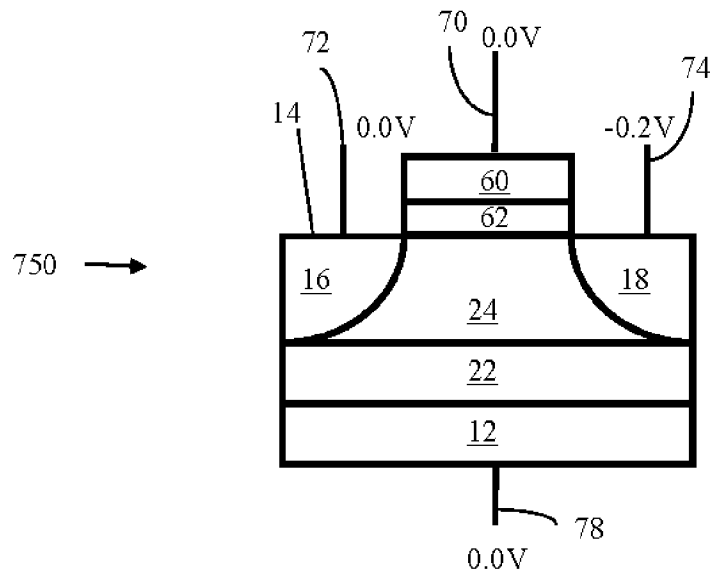


FIG. 99C

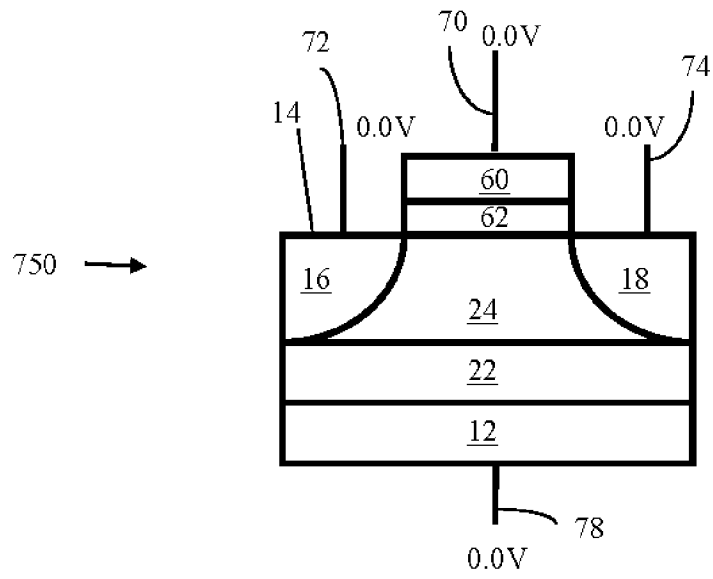


FIG. 99D

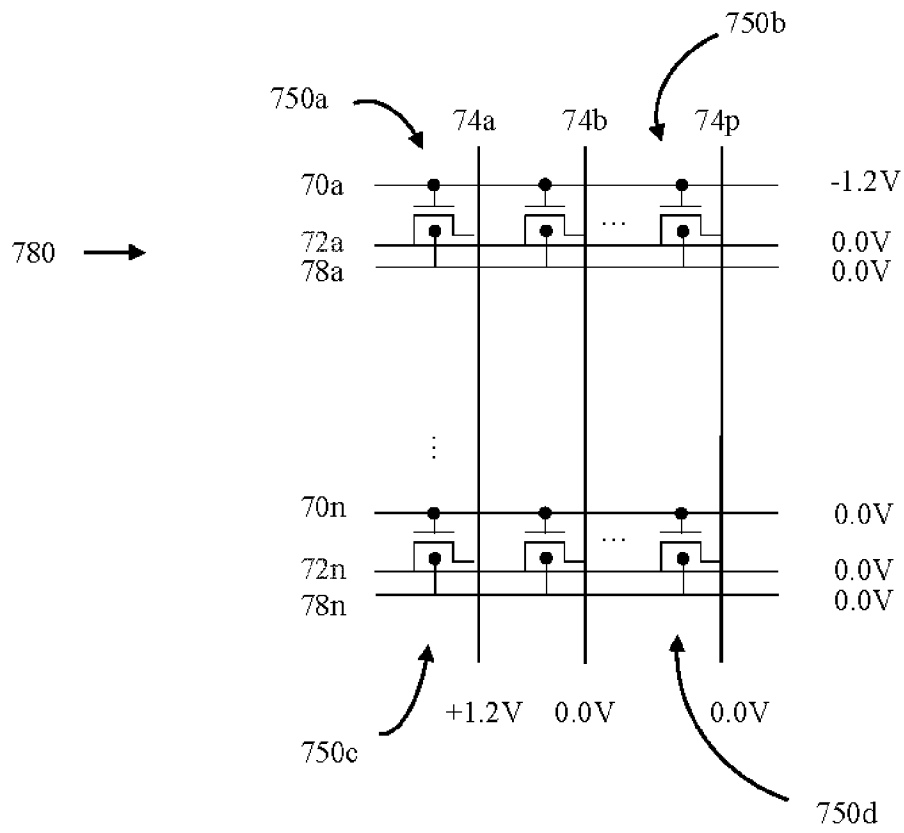


FIG. 100

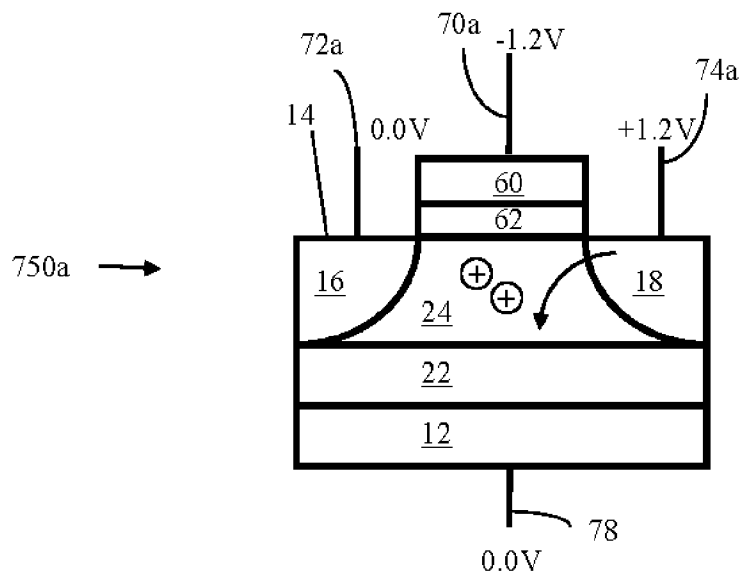


FIG. 101A

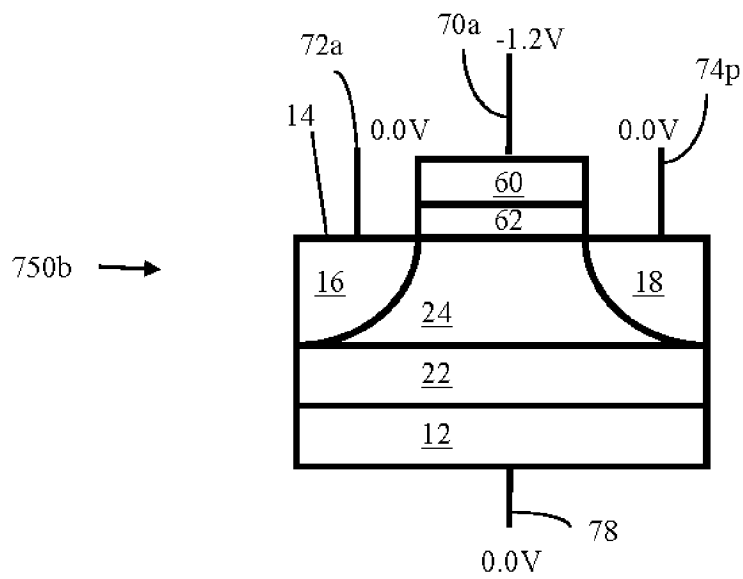


FIG. 101B

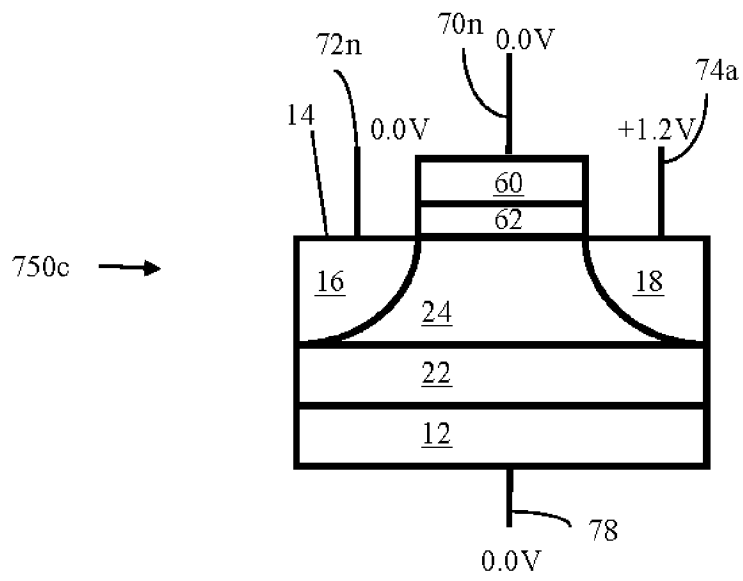


FIG. 101C

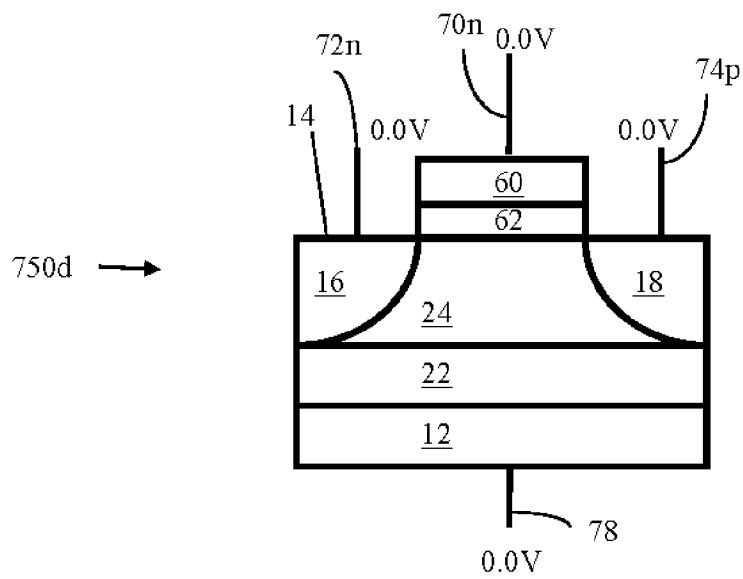


FIG. 101D

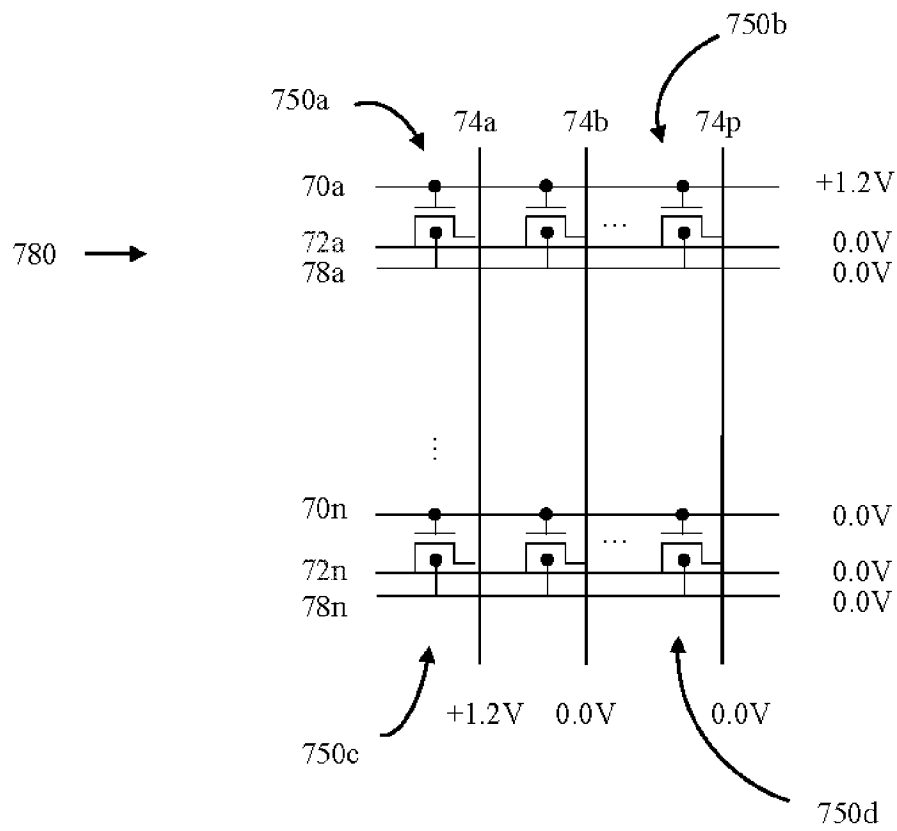


FIG. 102

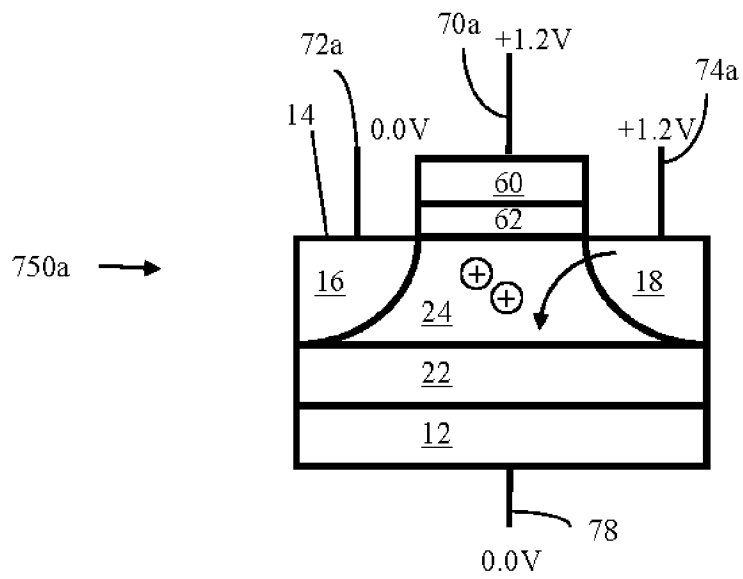


FIG. 103A

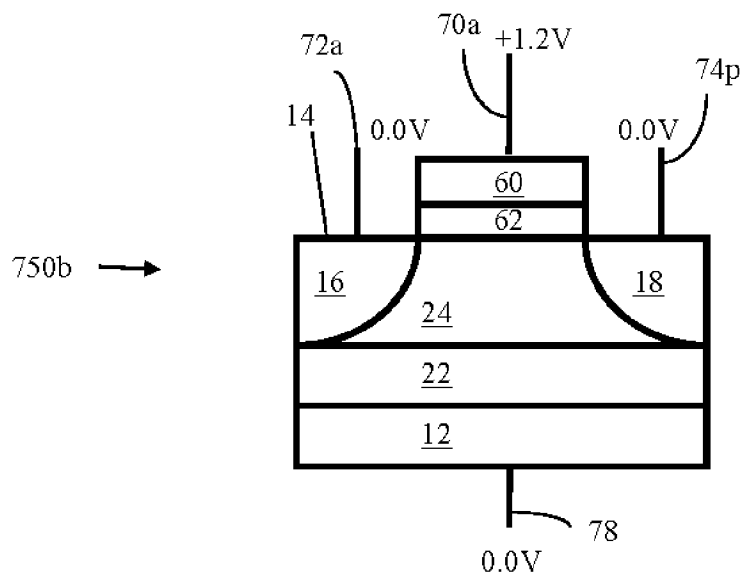


FIG. 103B

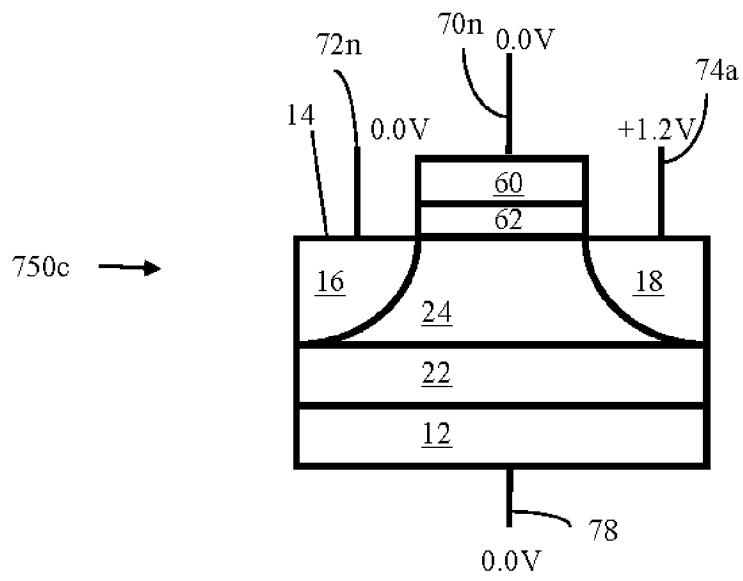


FIG. 103C

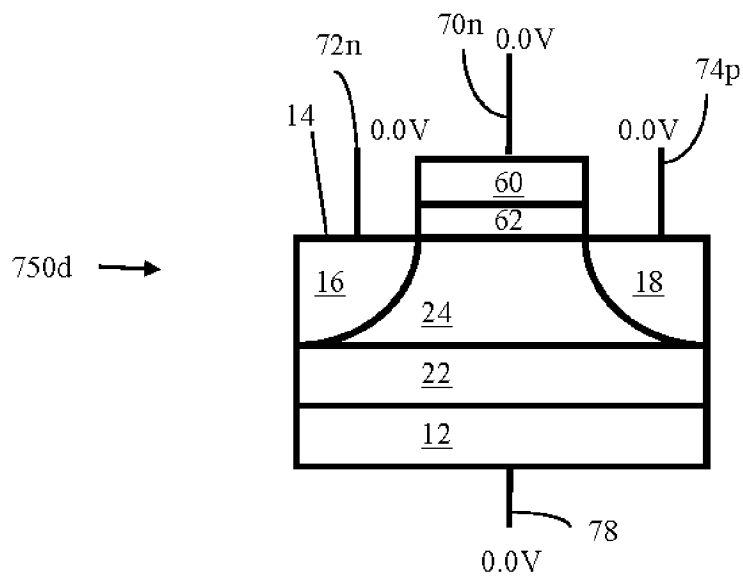


FIG. 103D

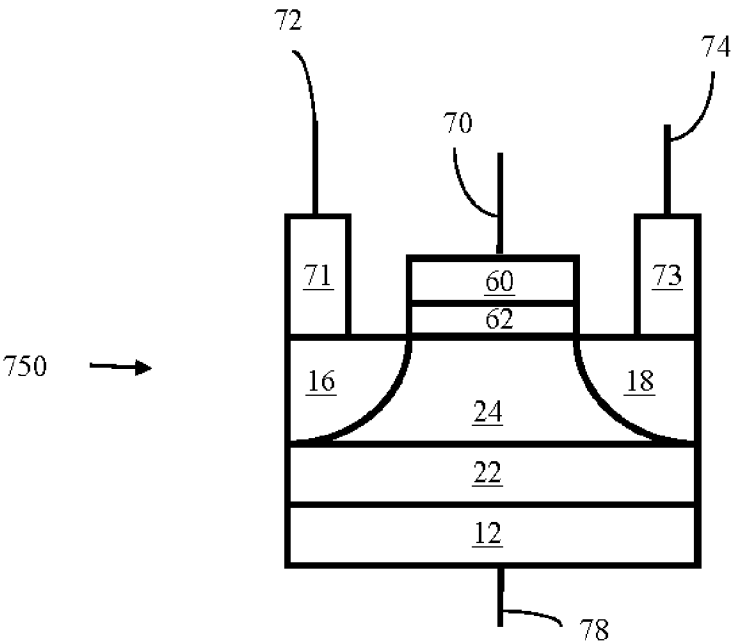


FIG. 104

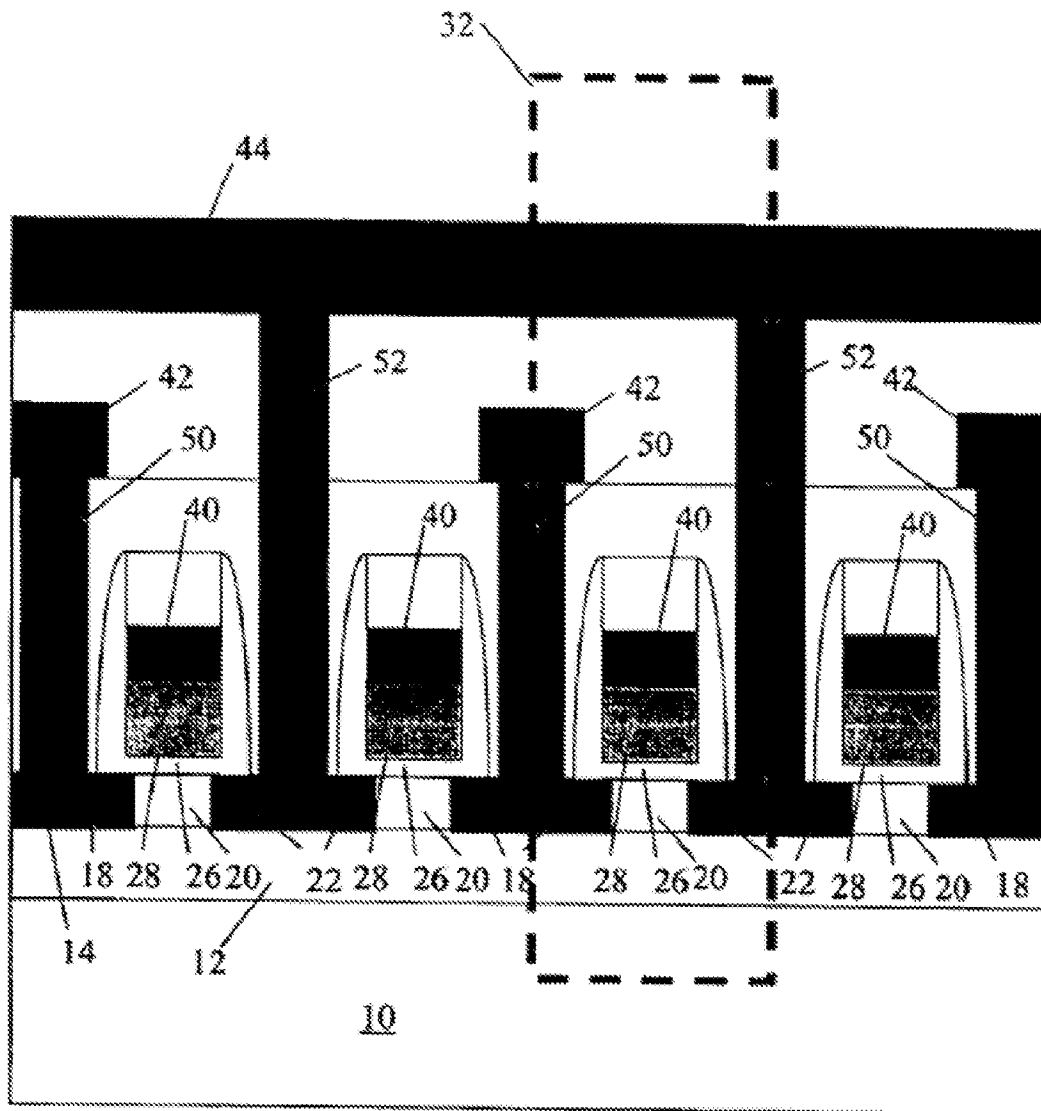


FIG. 105
(Prior Art)

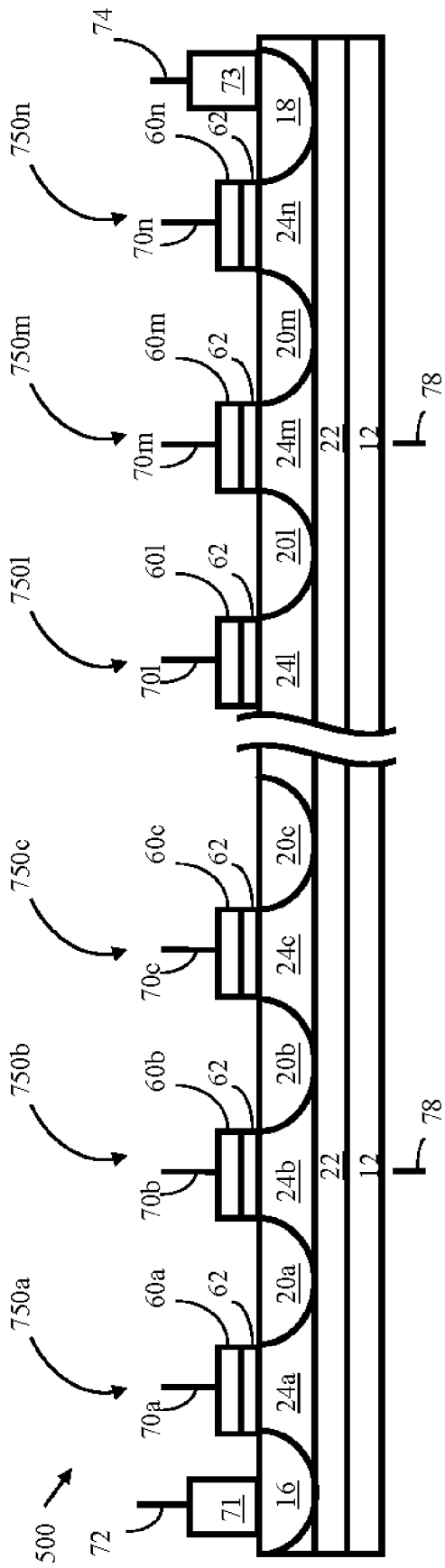


FIG. 106A

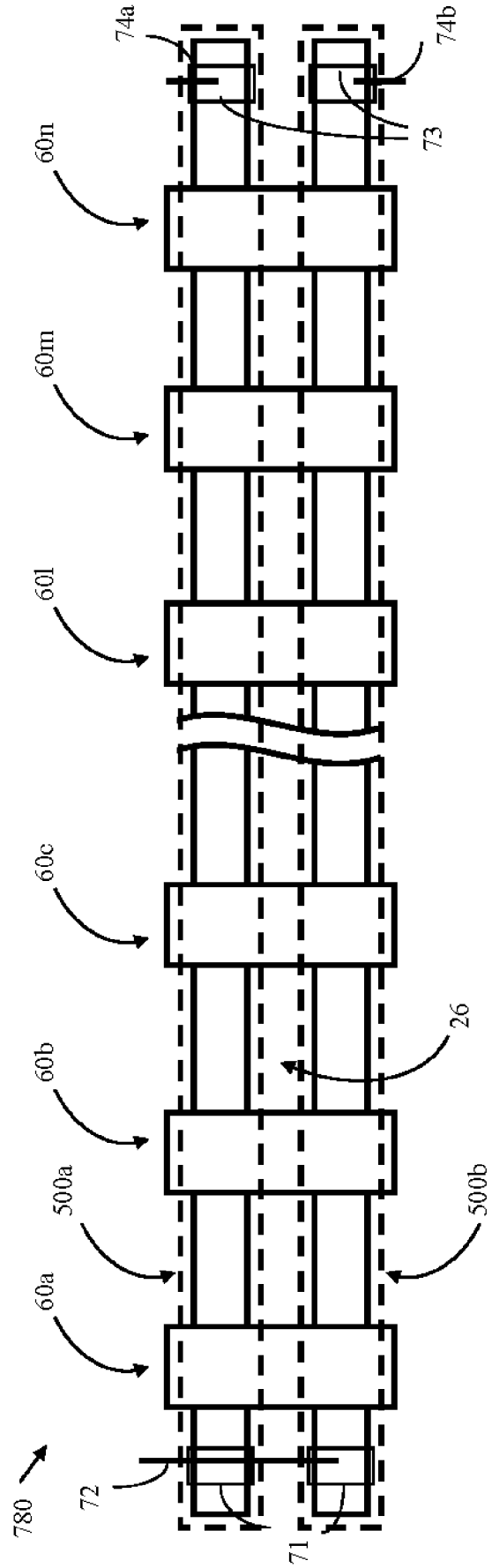


FIG. 106B

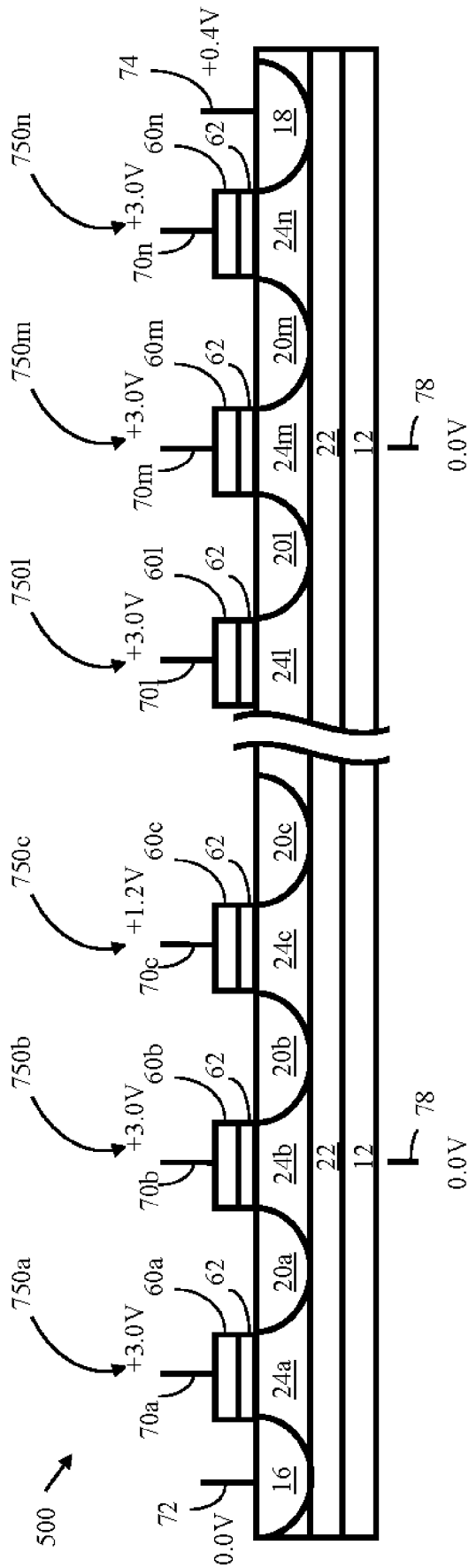


FIG. 108

780 

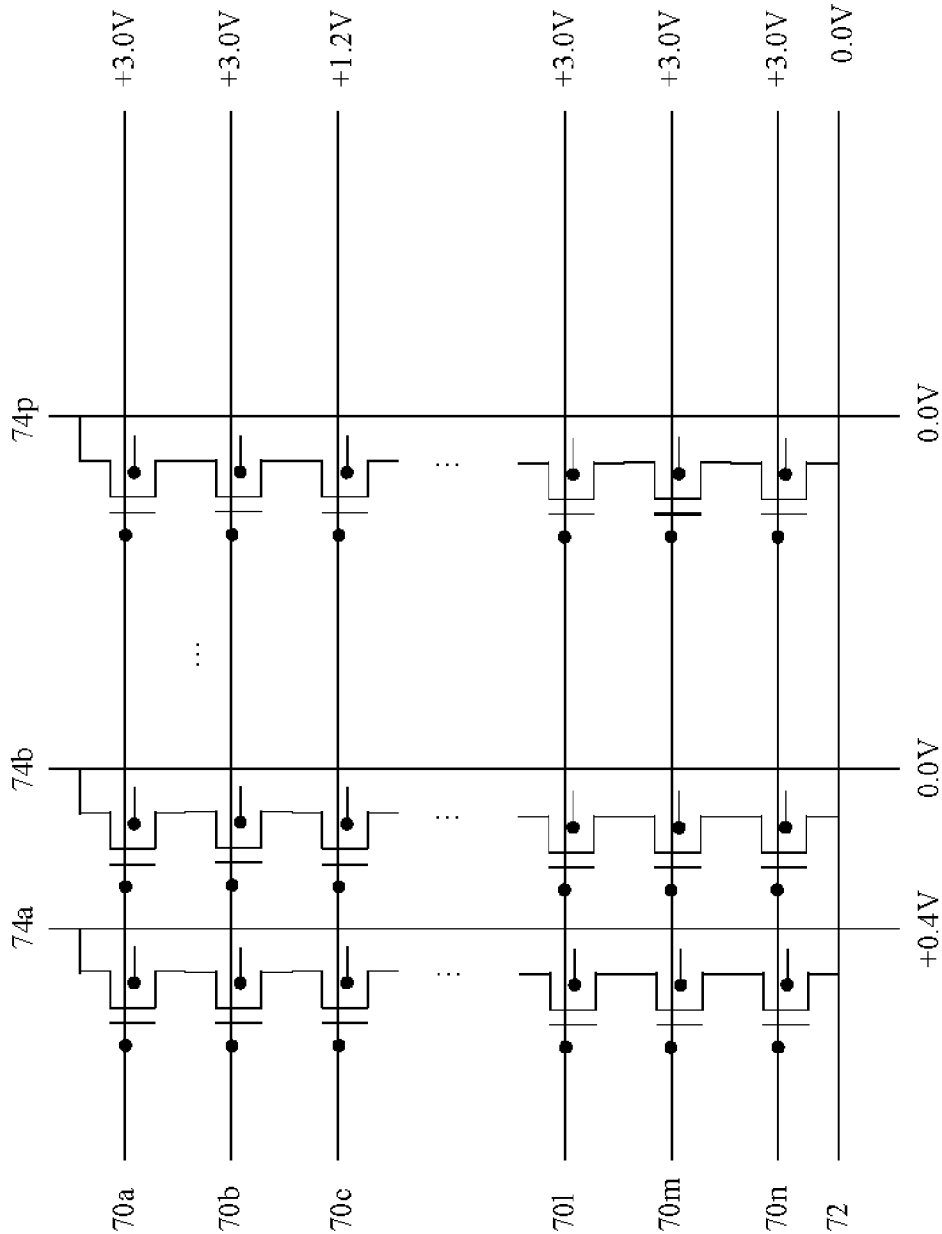
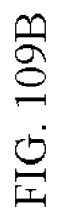


FIG. 109A



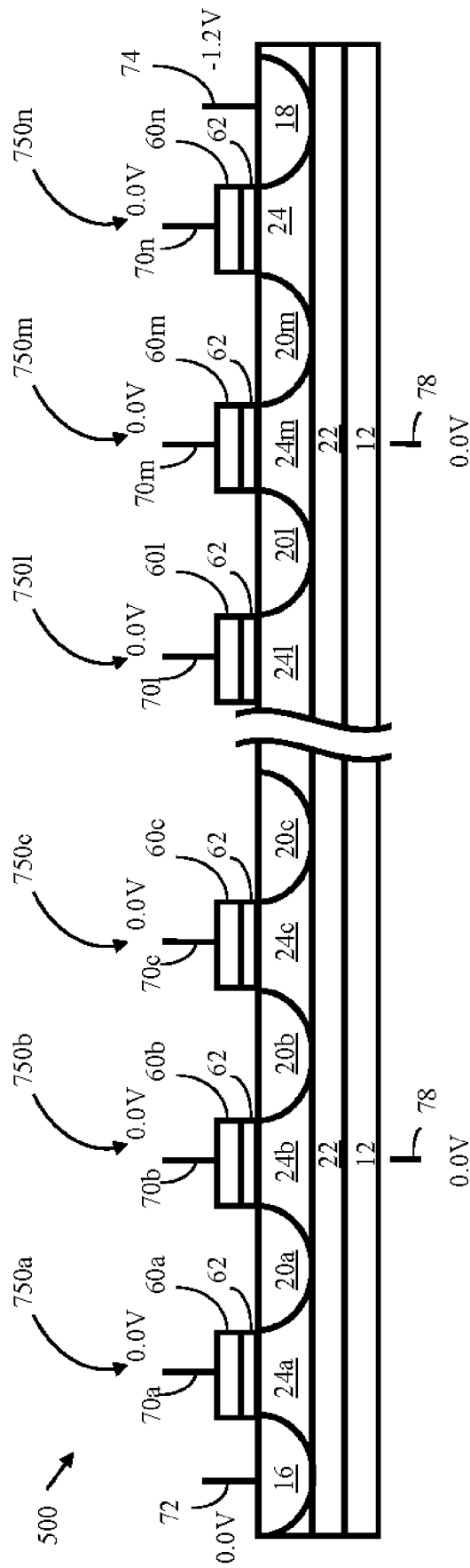


FIG. 110

780 

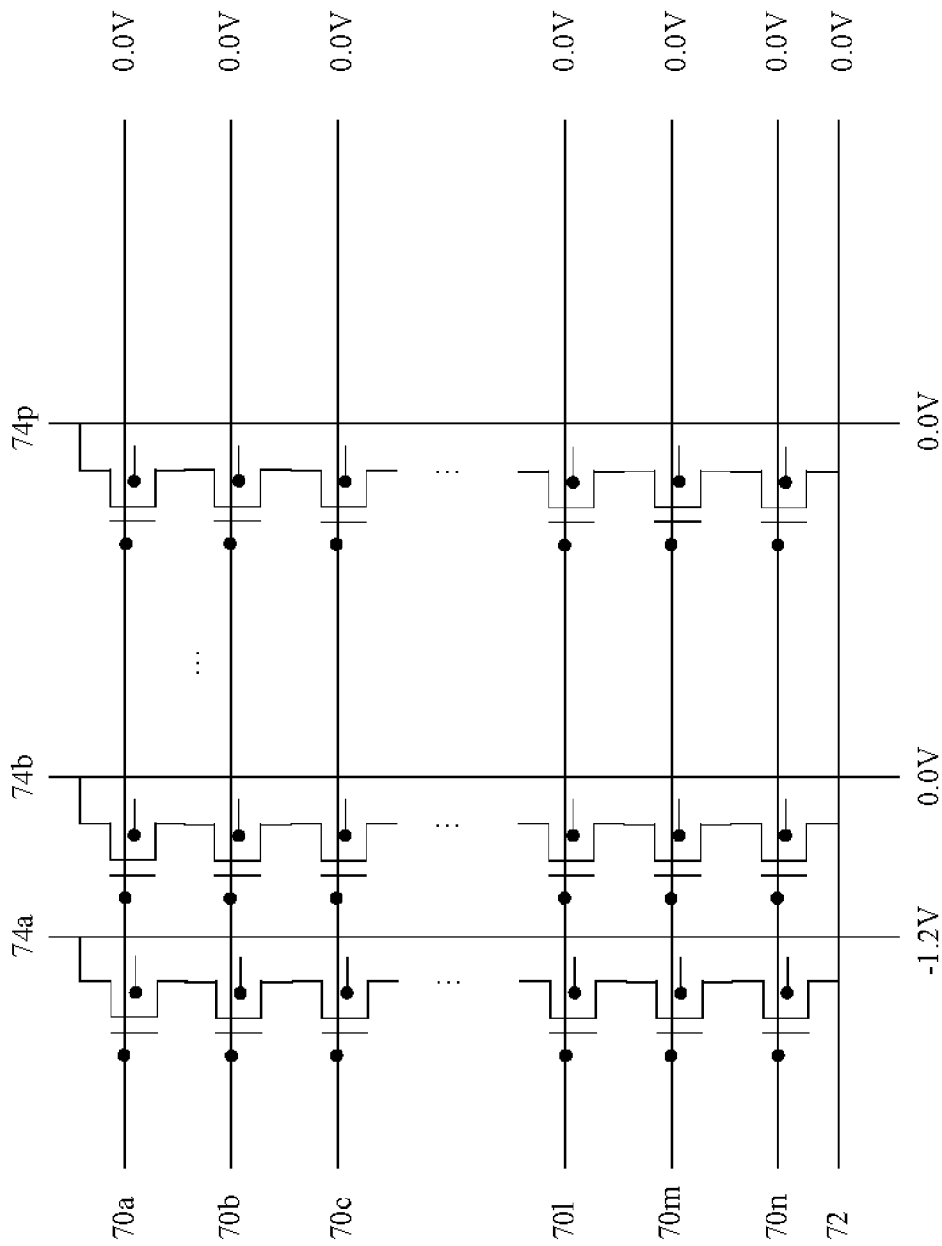


FIG. 111

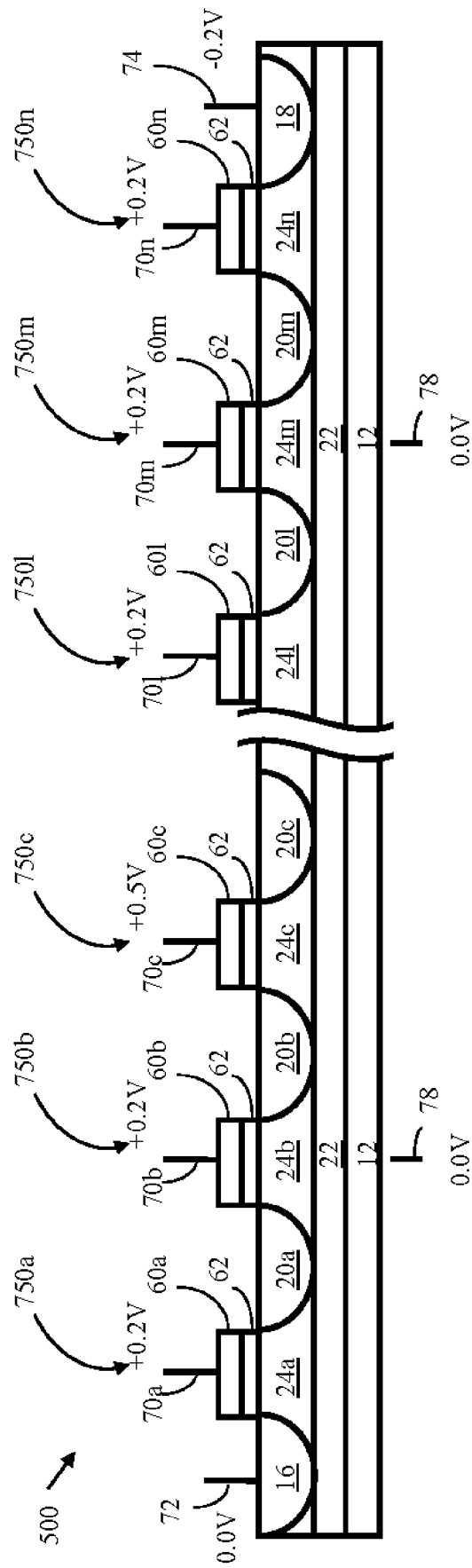
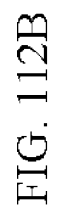


FIG. 112A



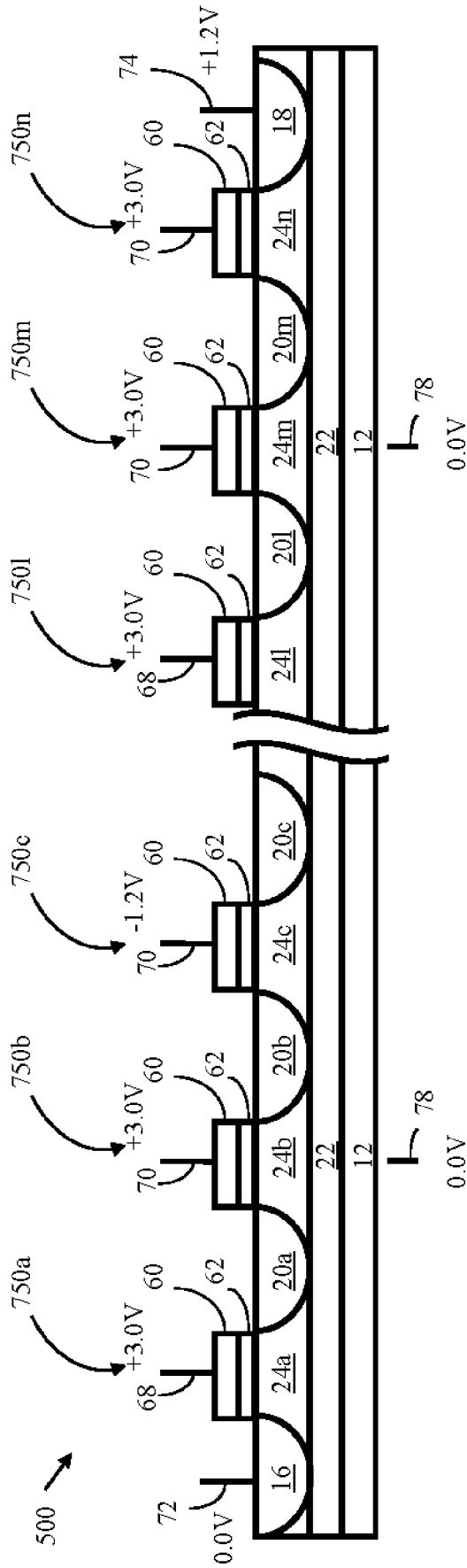


FIG. 113A

780 

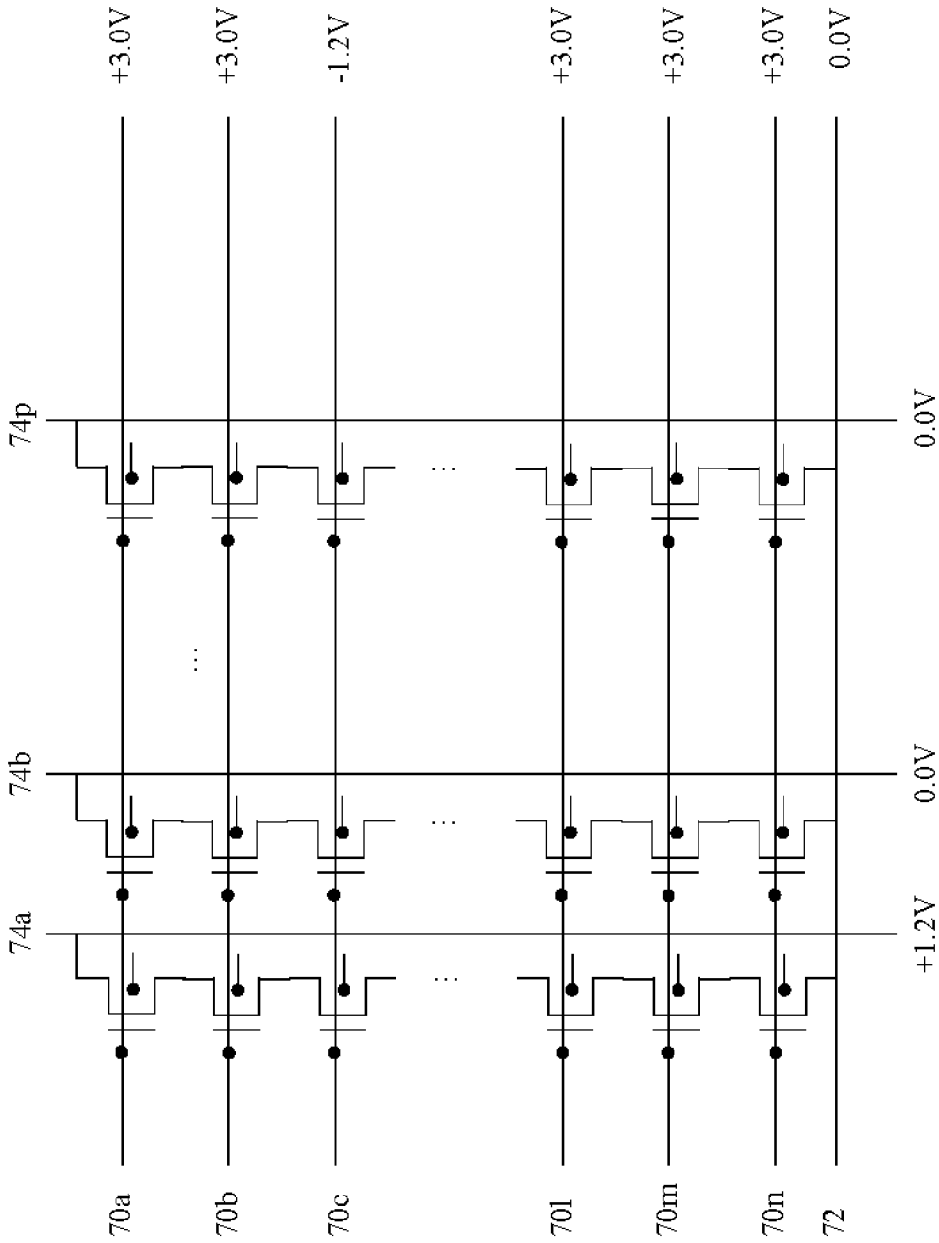


FIG. 113B

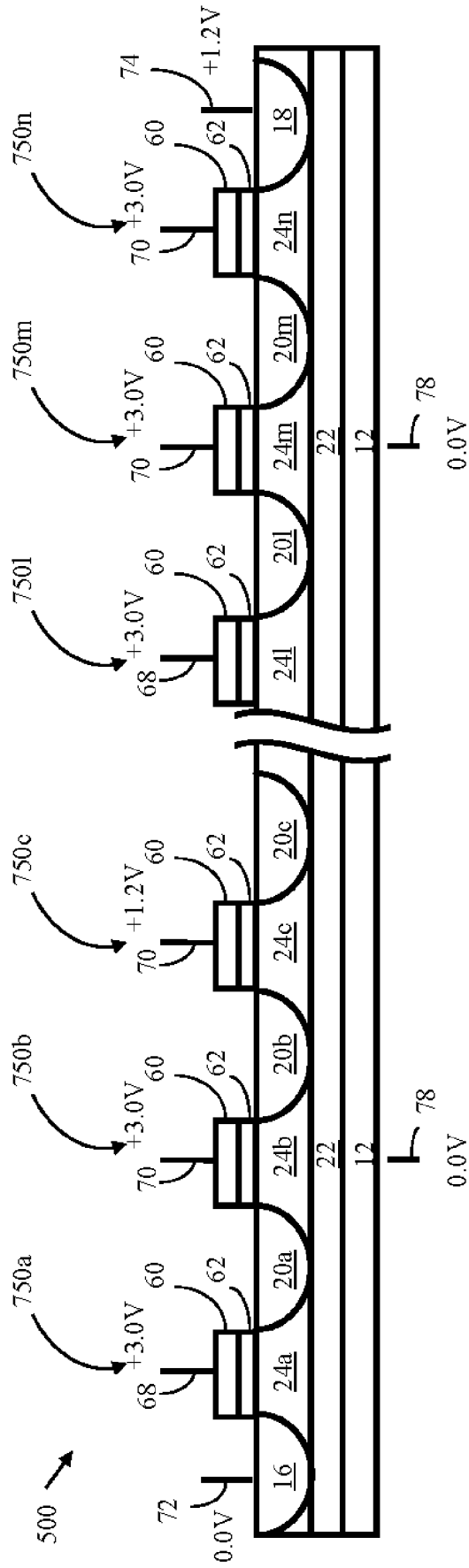


FIG. 114A

780 

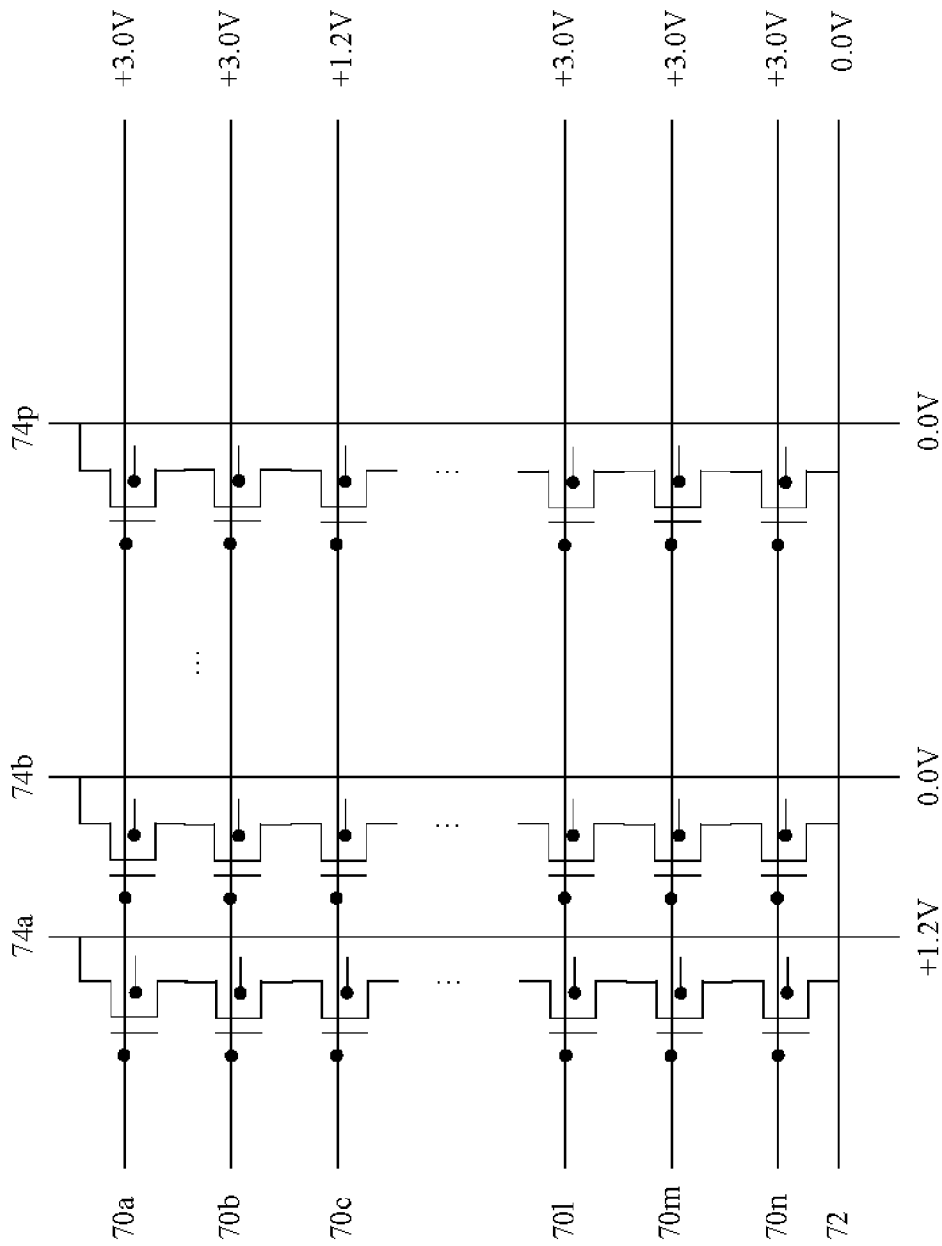


FIG. 114B

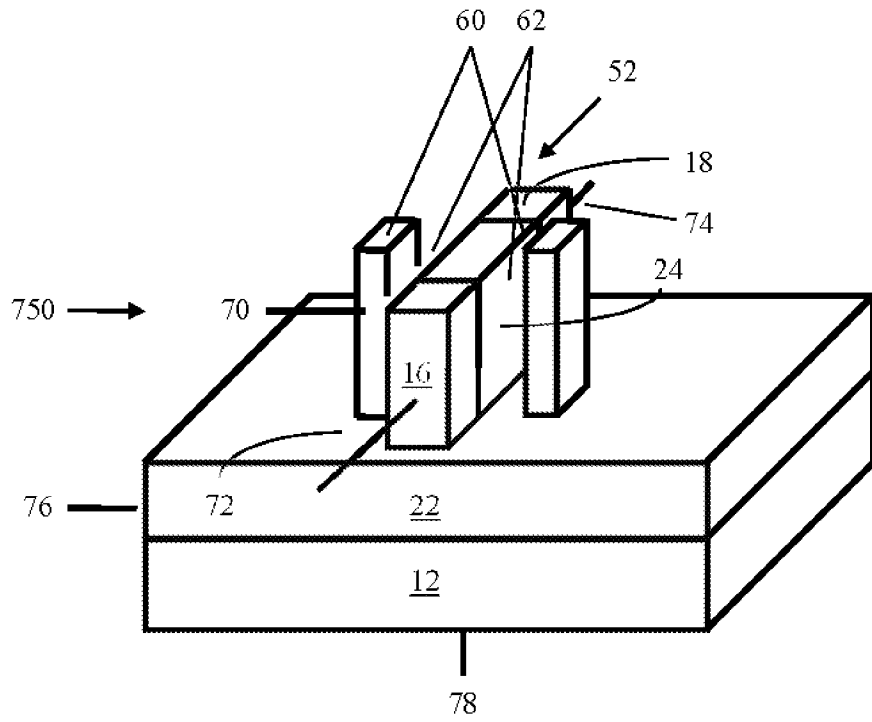


FIG. 115A

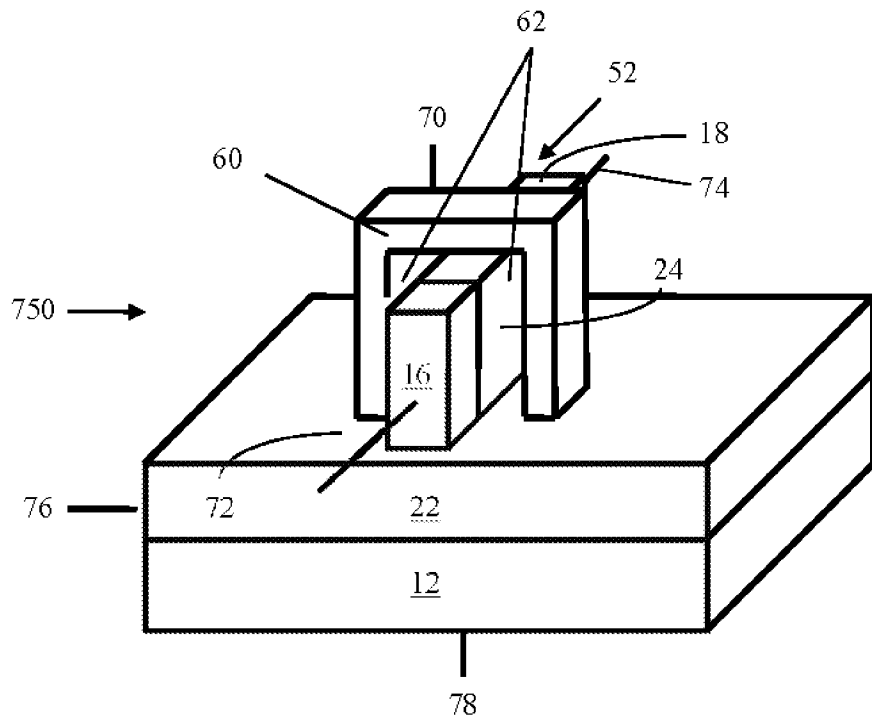


FIG. 115B

Floating Body 24 is positively charged

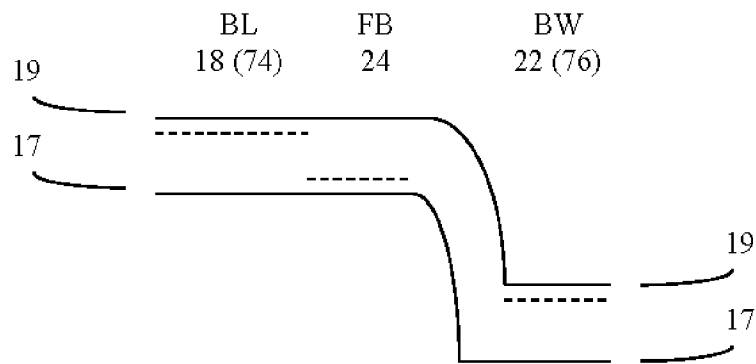


FIG. 116A

FB is neutrally charged: $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

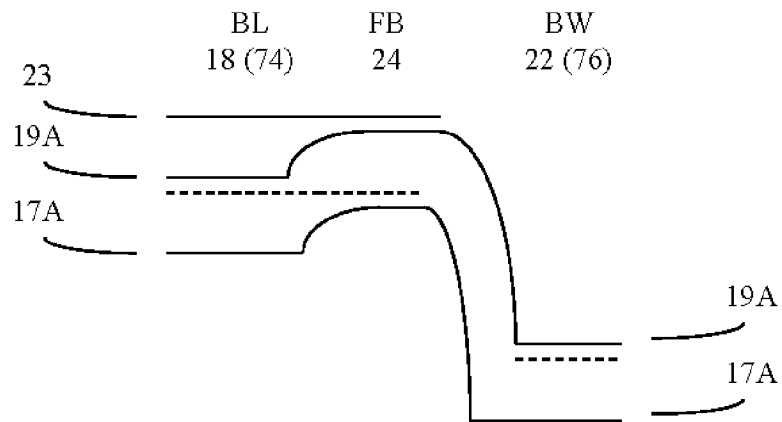


FIG. 116B

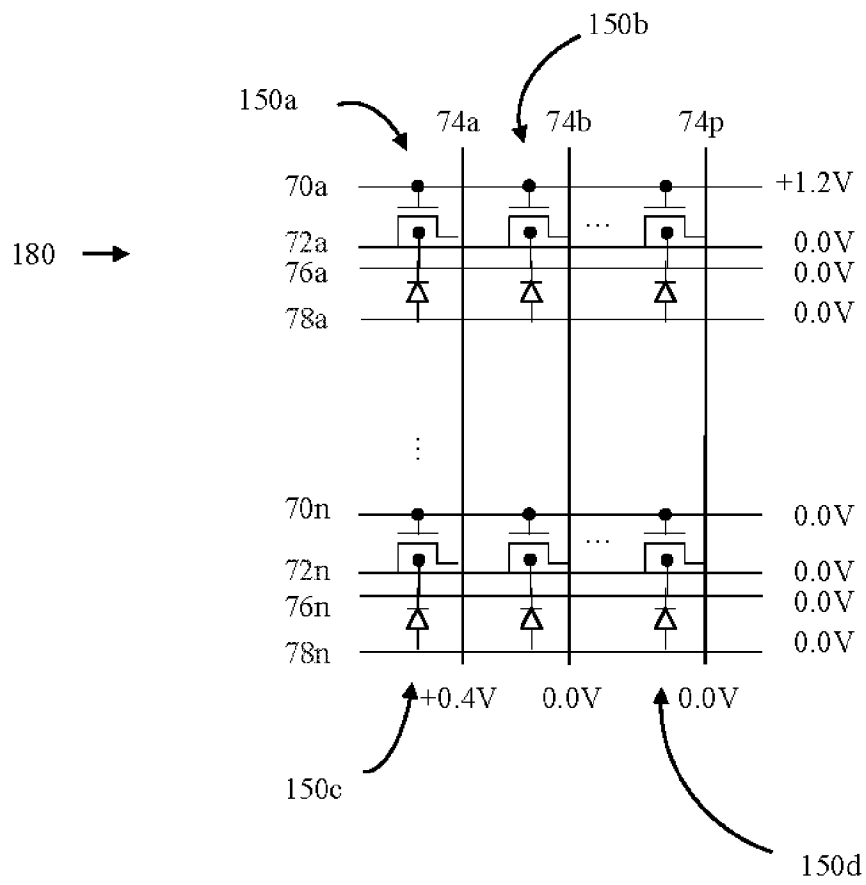


FIG. 117

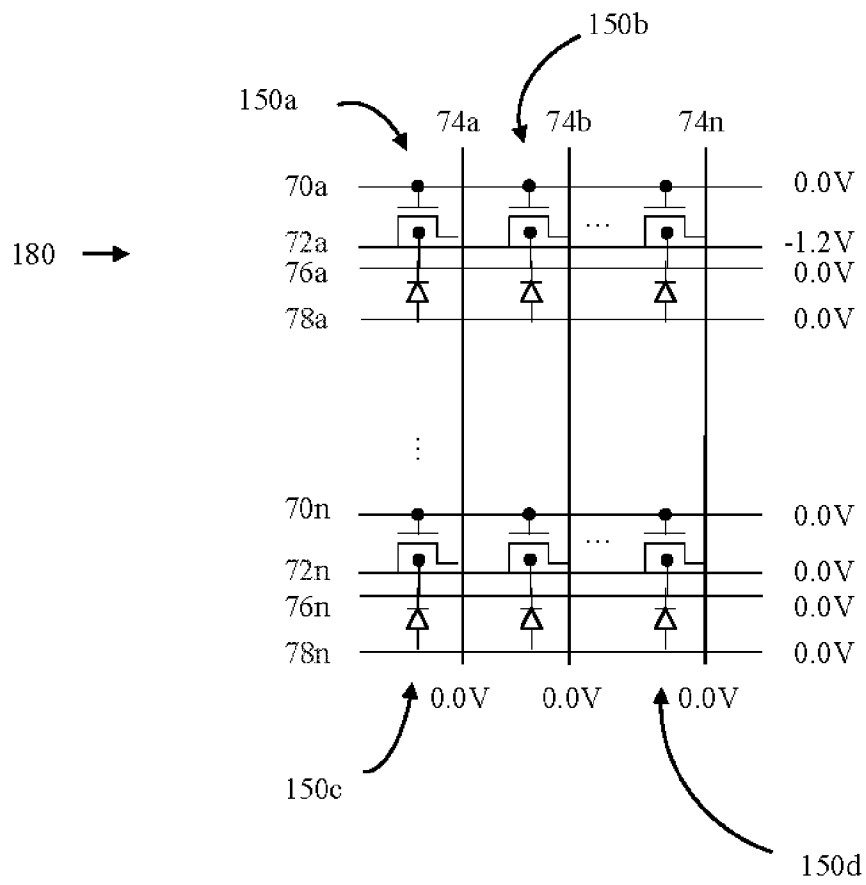


FIG. 118

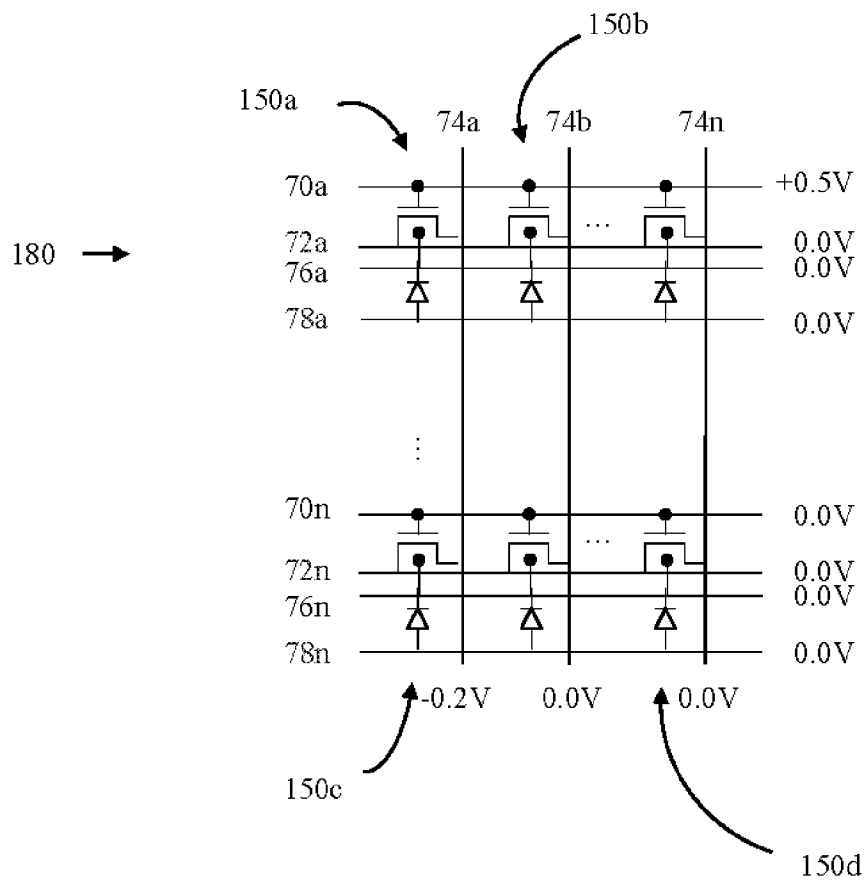


FIG. 119

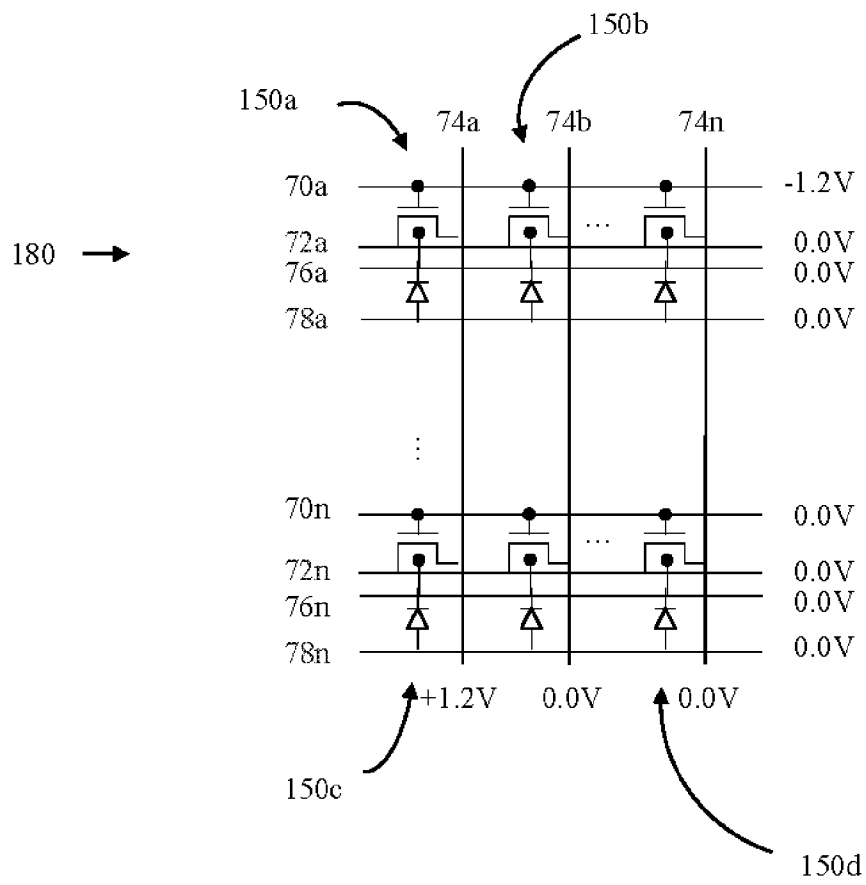


FIG. 120A

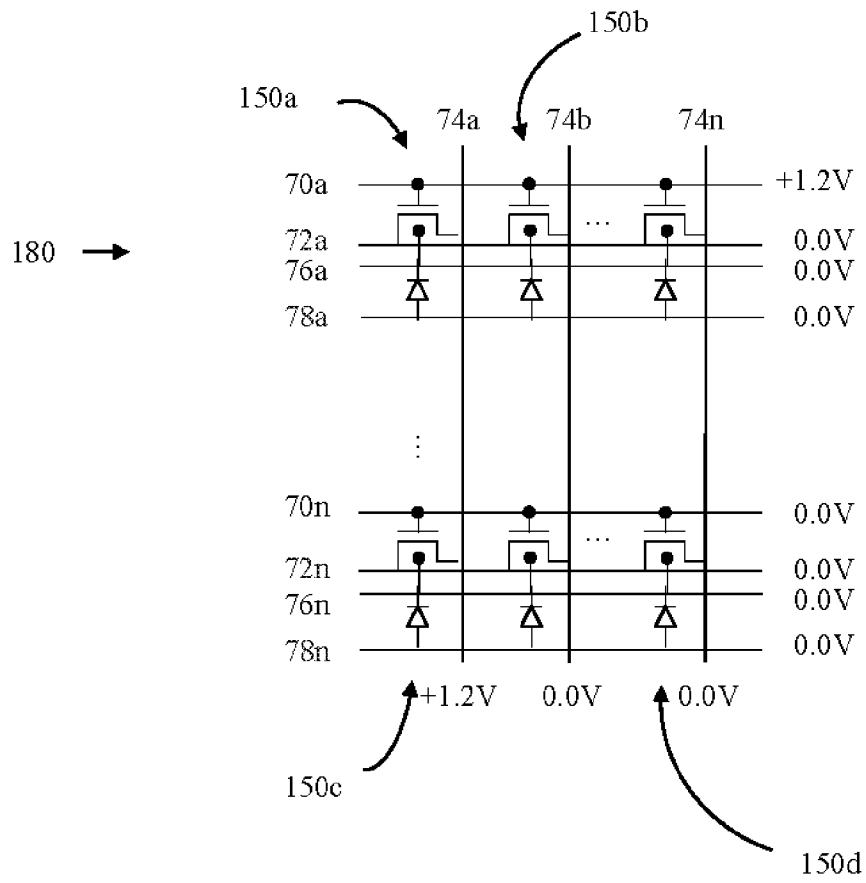


FIG. 120B

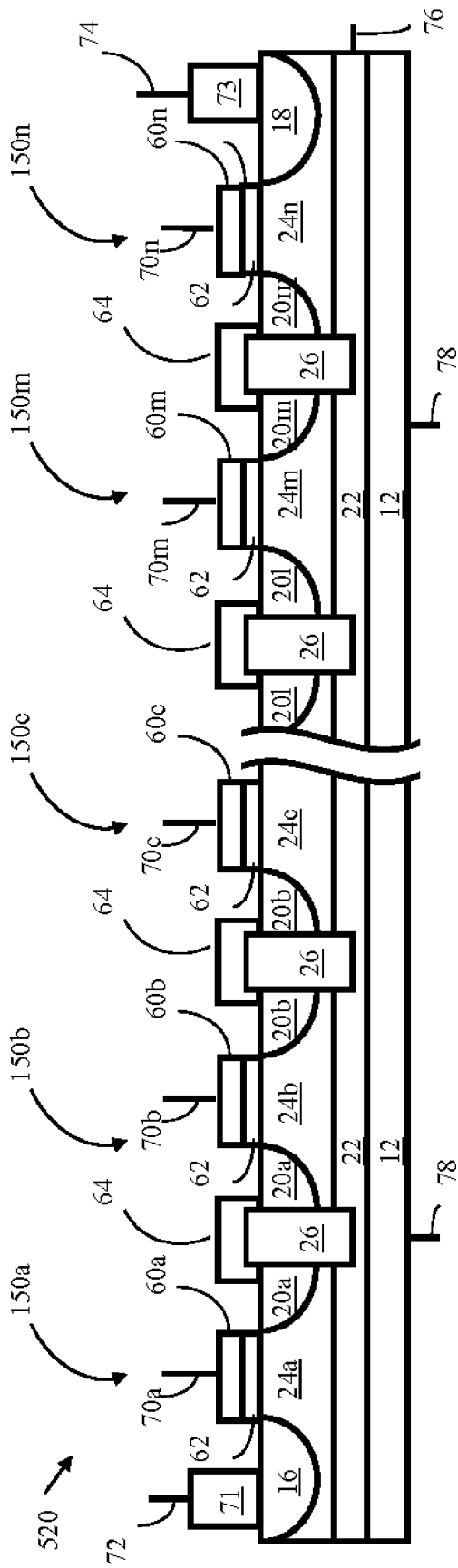


FIG. 121A

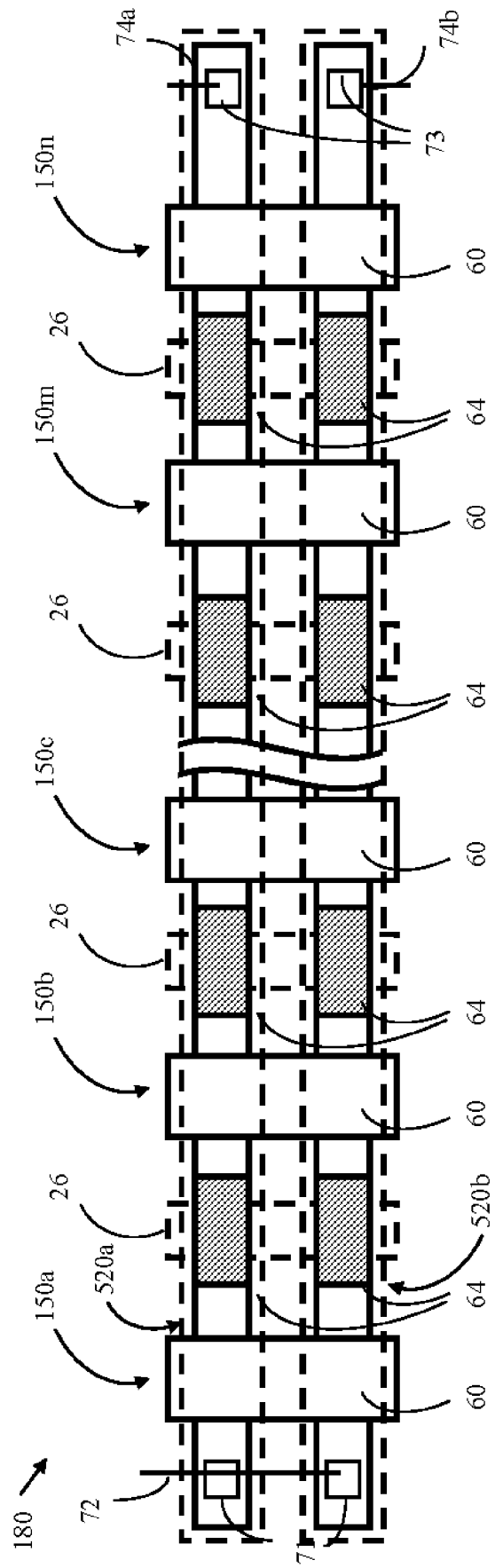


FIG. 121B

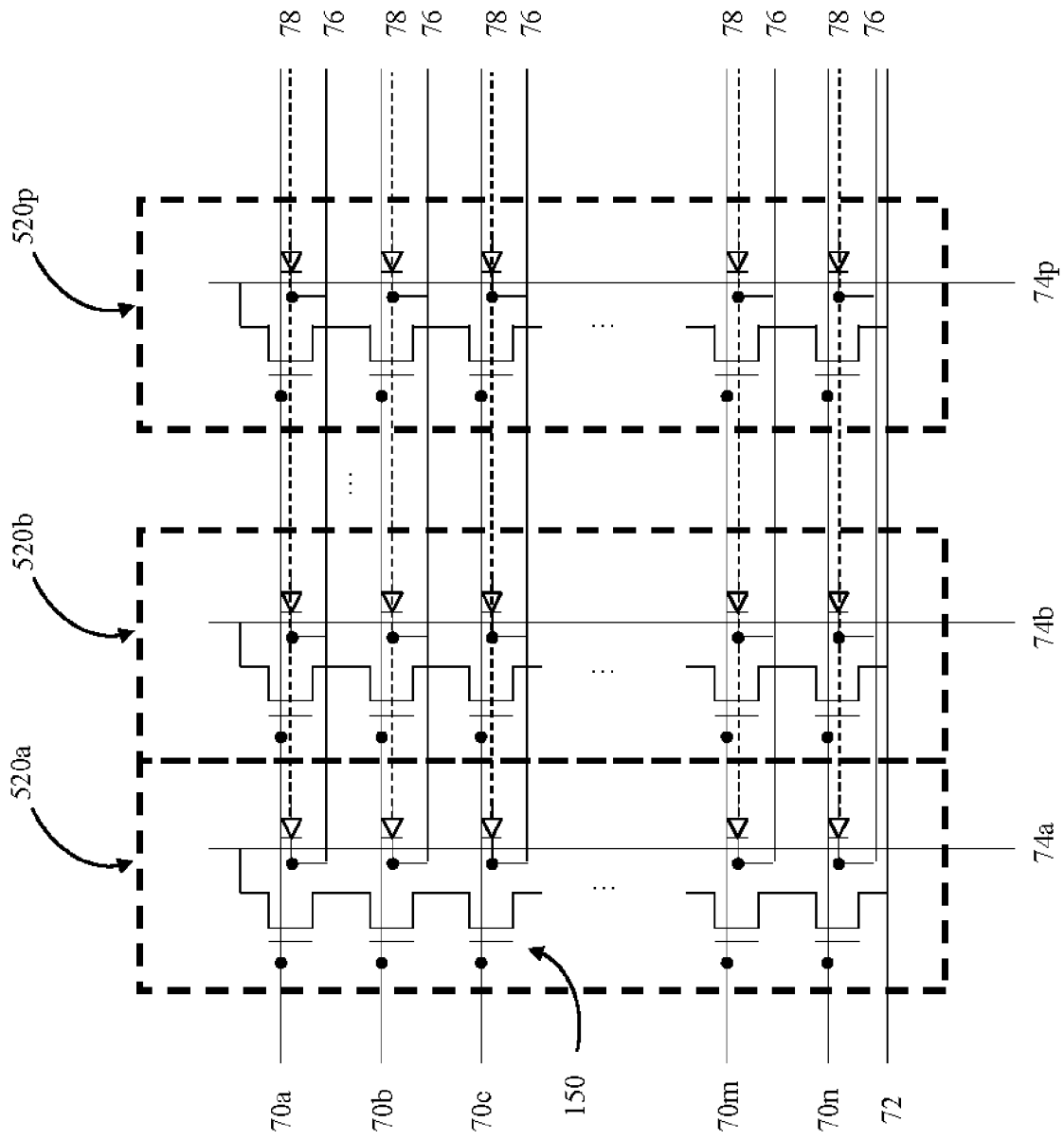


FIG. 121C

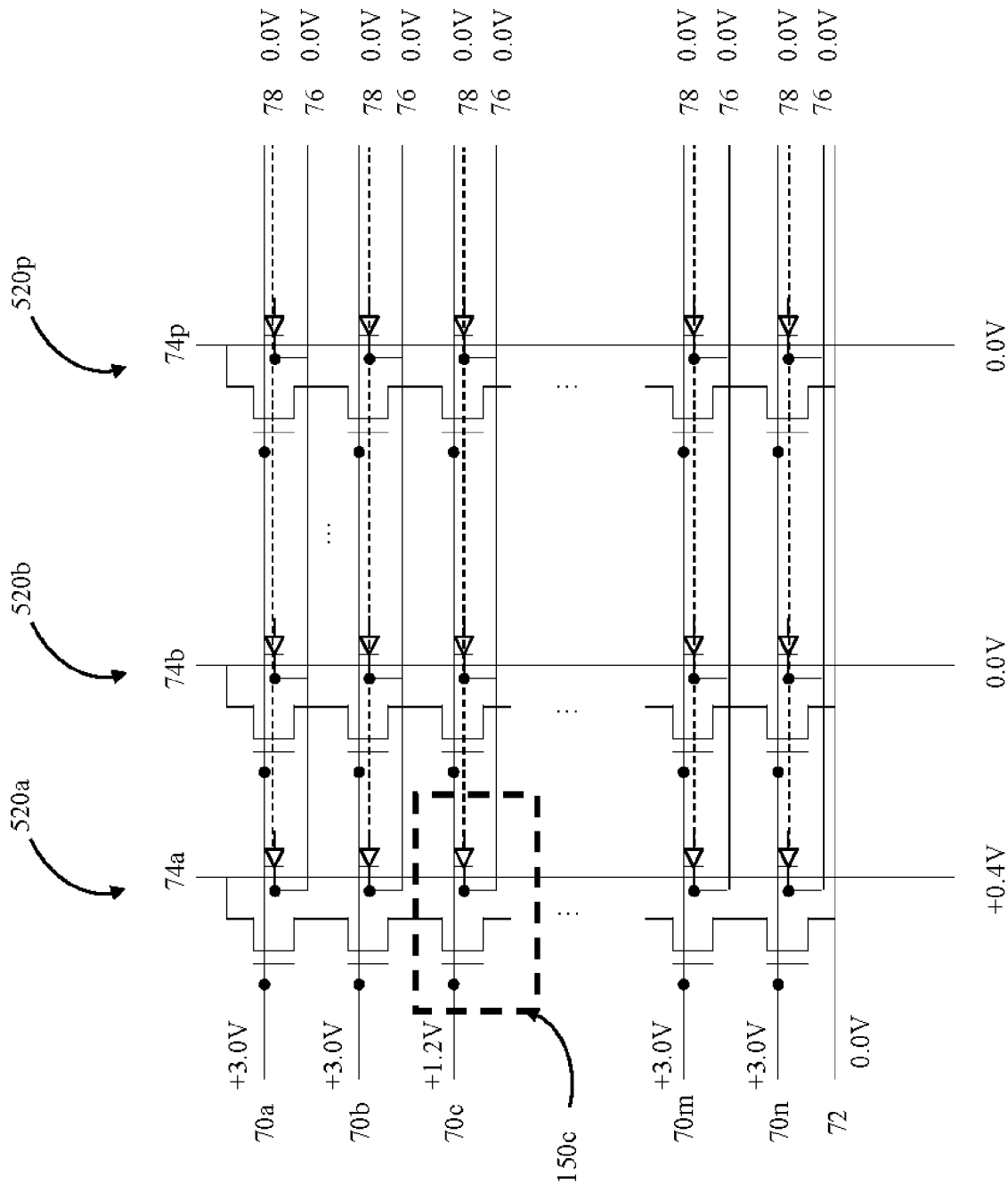


FIG. 123A

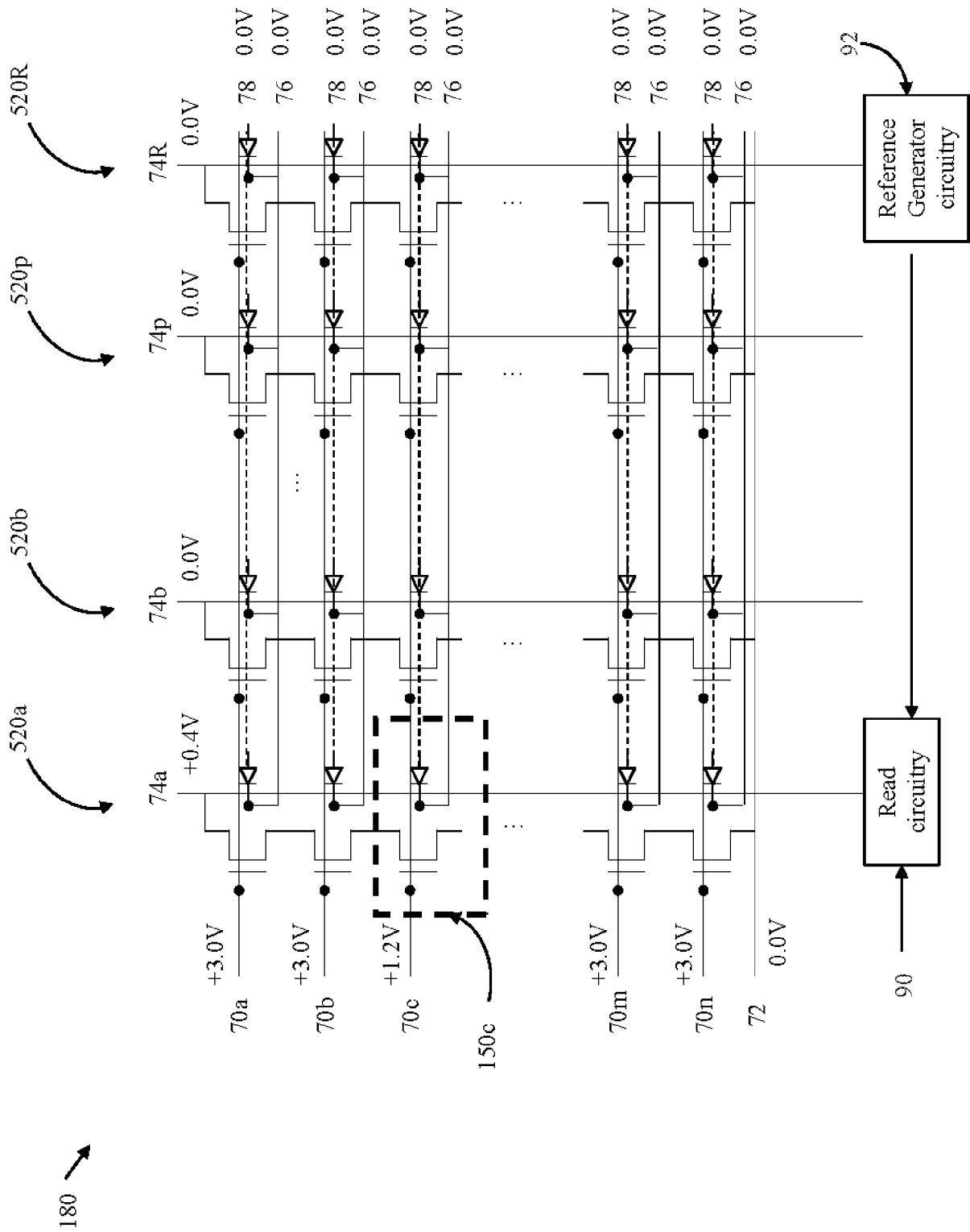


FIG. 123B

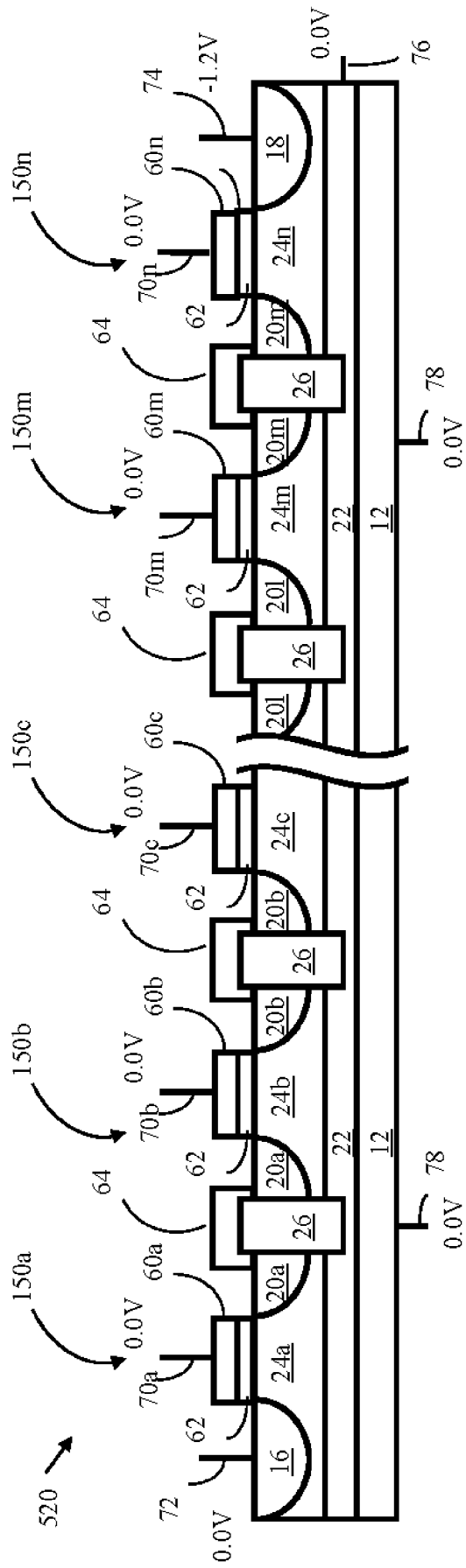


FIG. 124

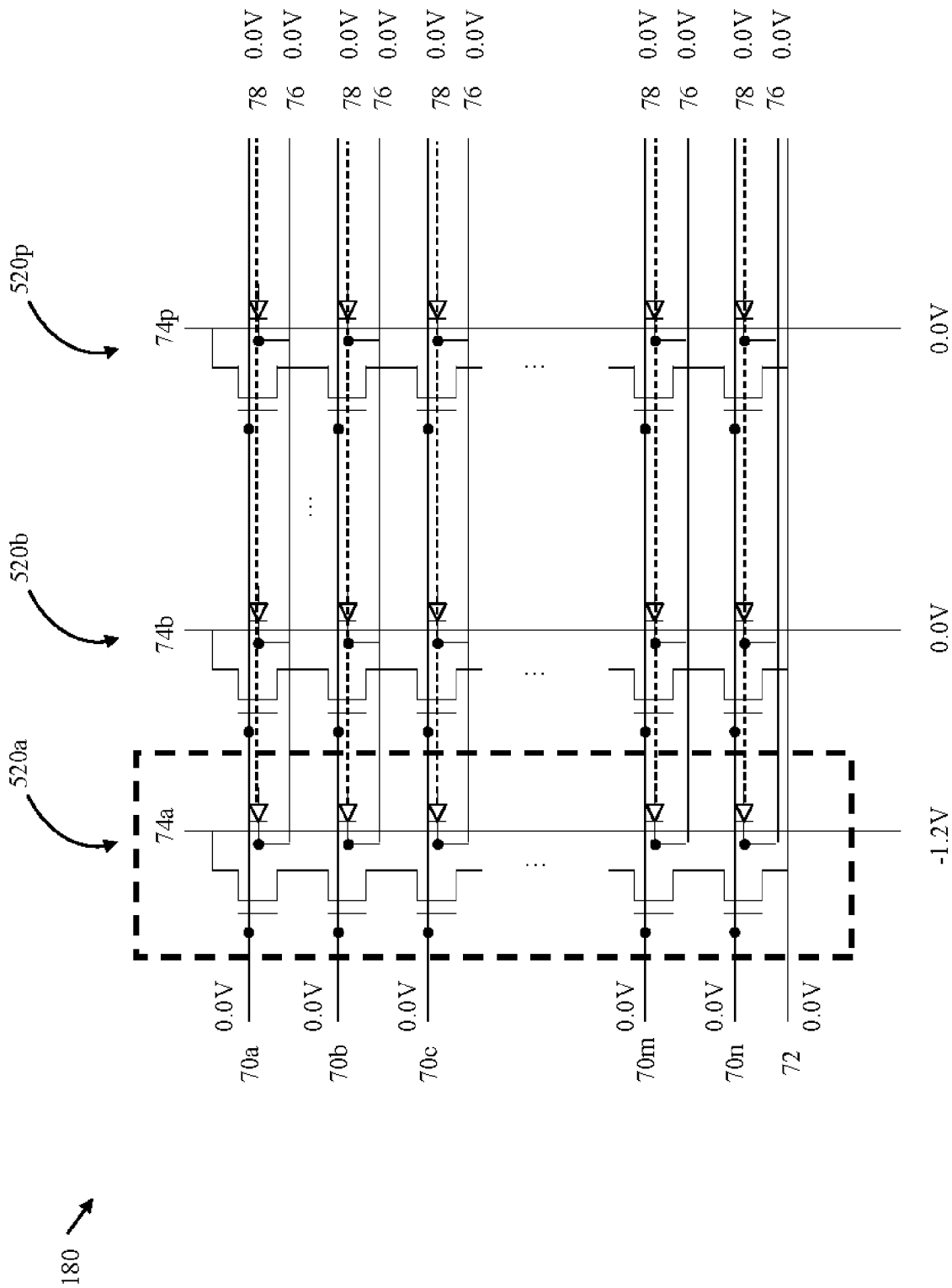


FIG. 125

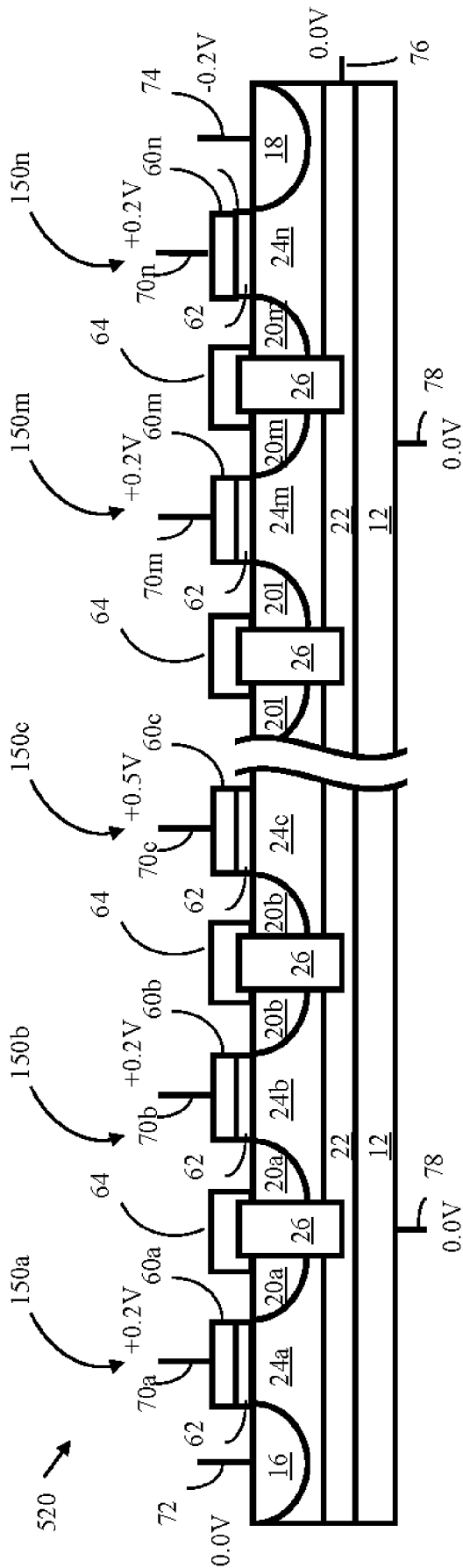


FIG. 126

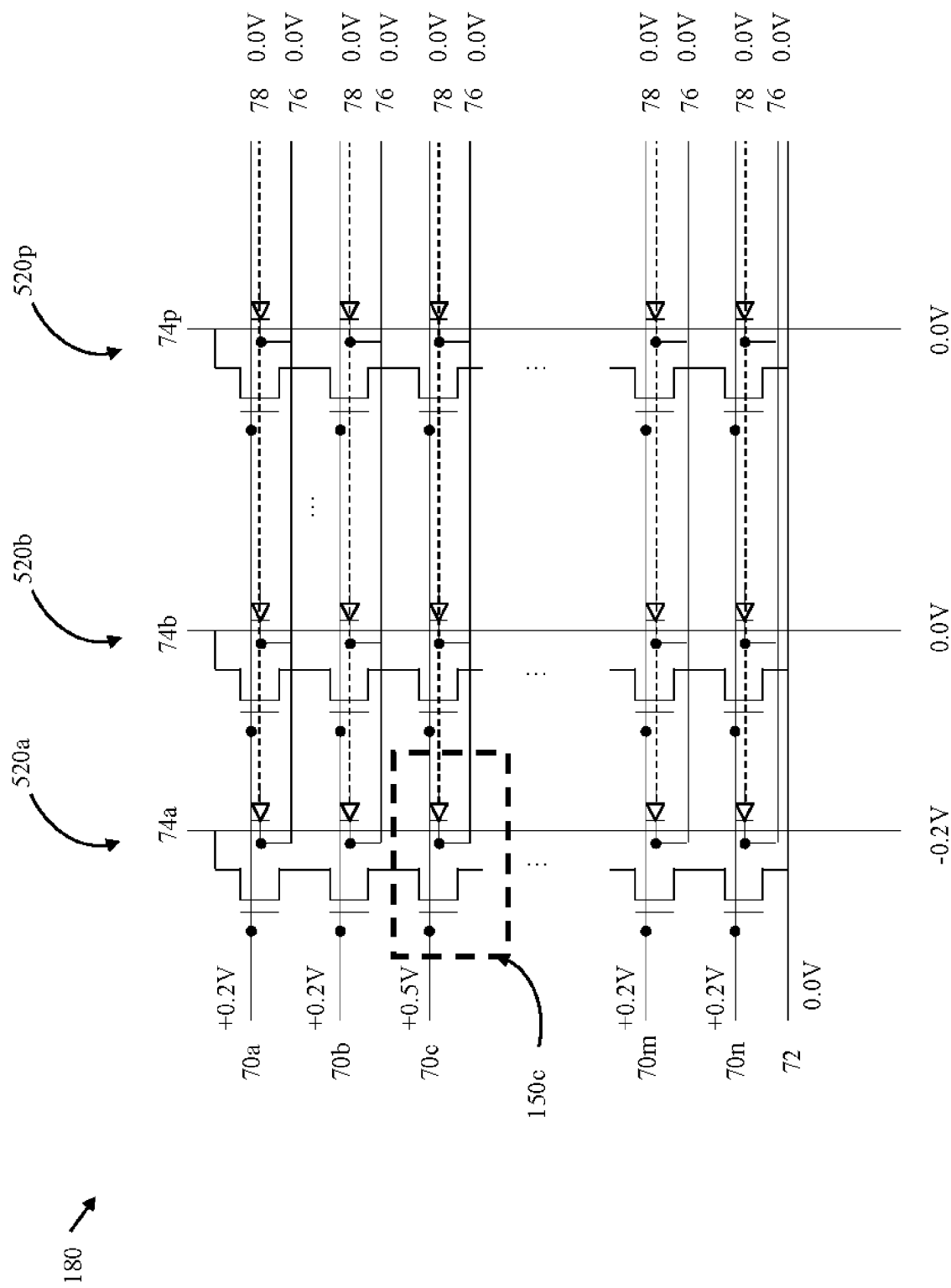


FIG. 127

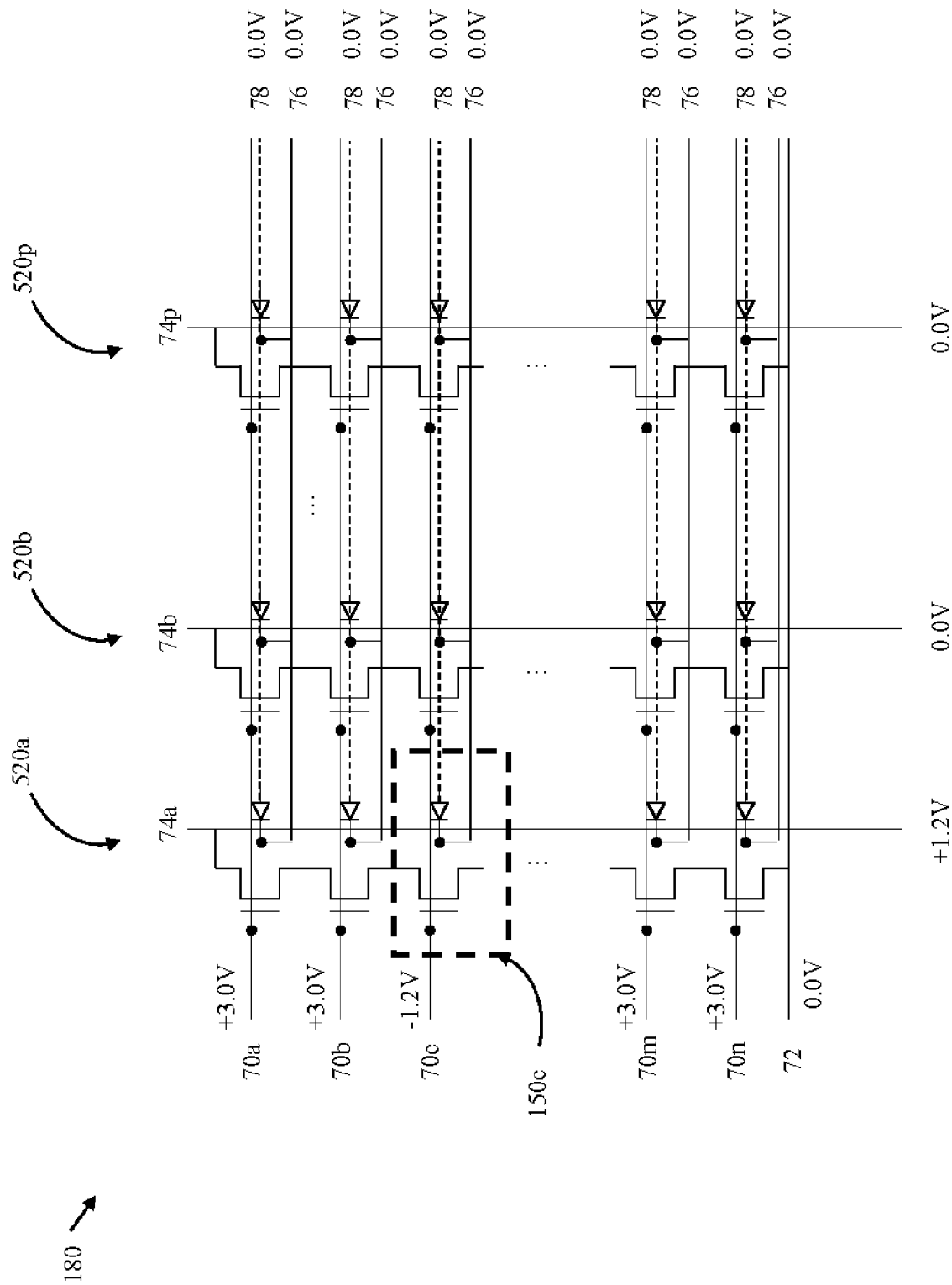


FIG. 129

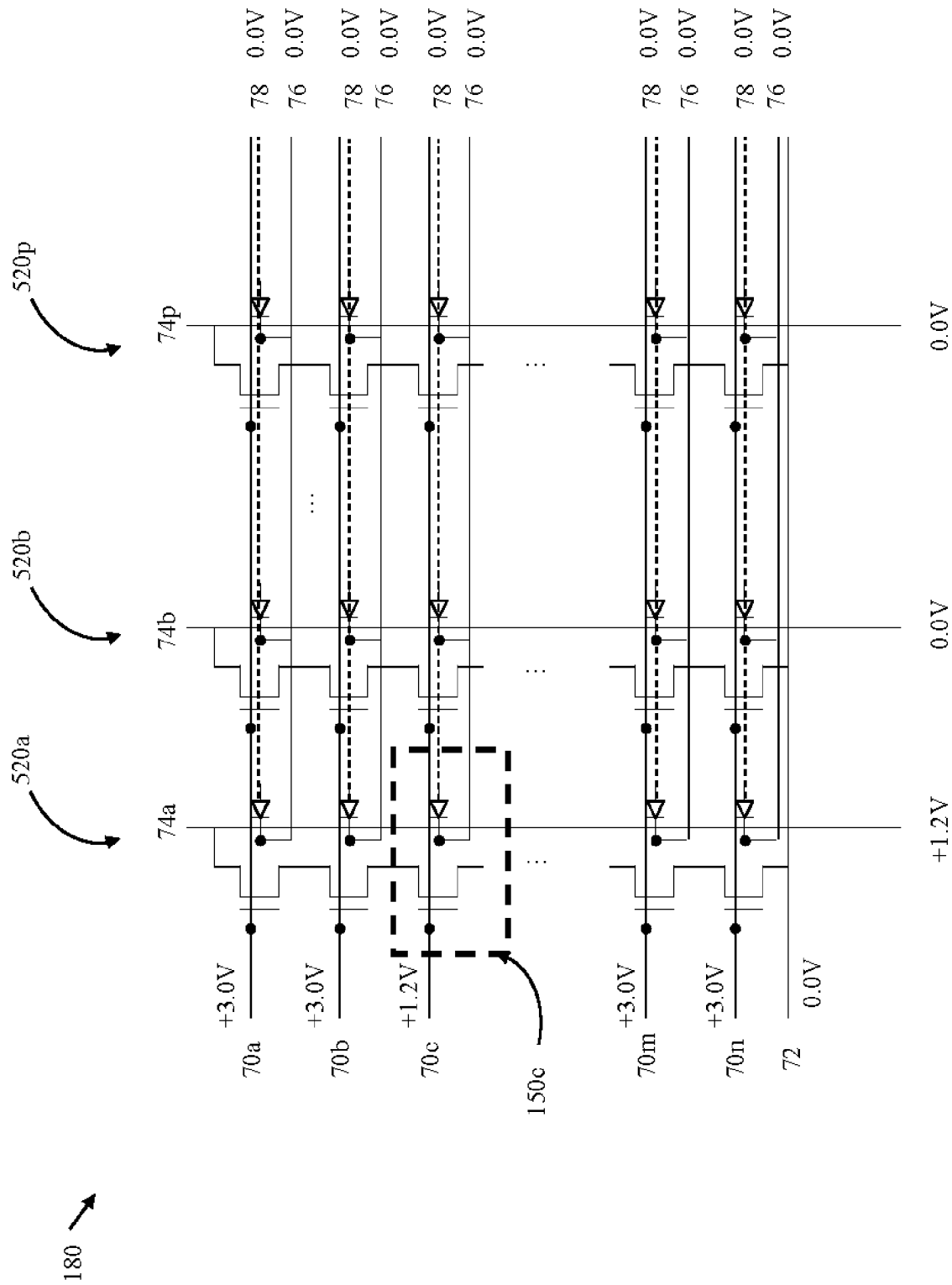


FIG. 130B

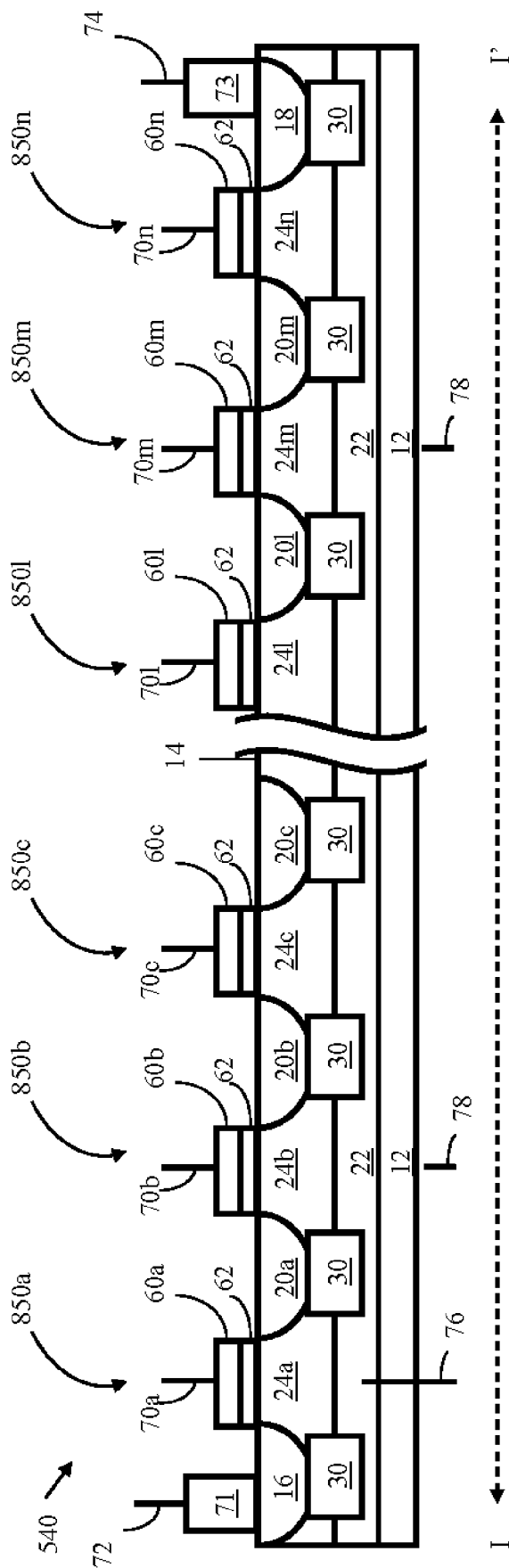


FIG. 131B

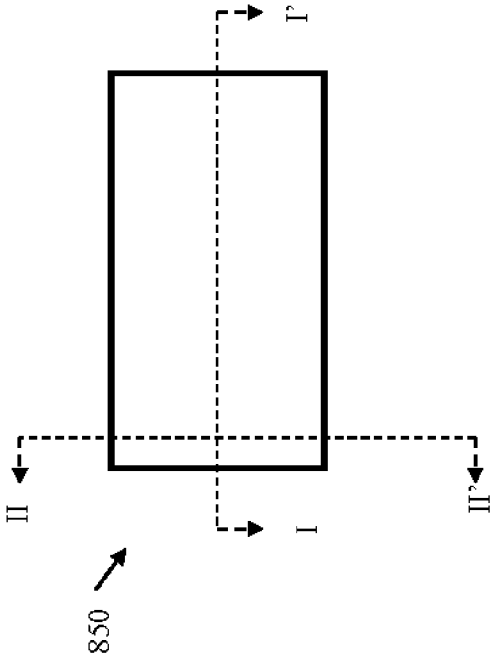


FIG. 132A

850

850

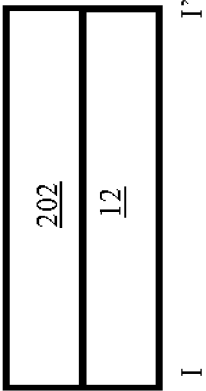


FIG. 132B

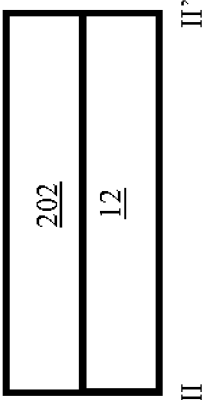


FIG. 132C

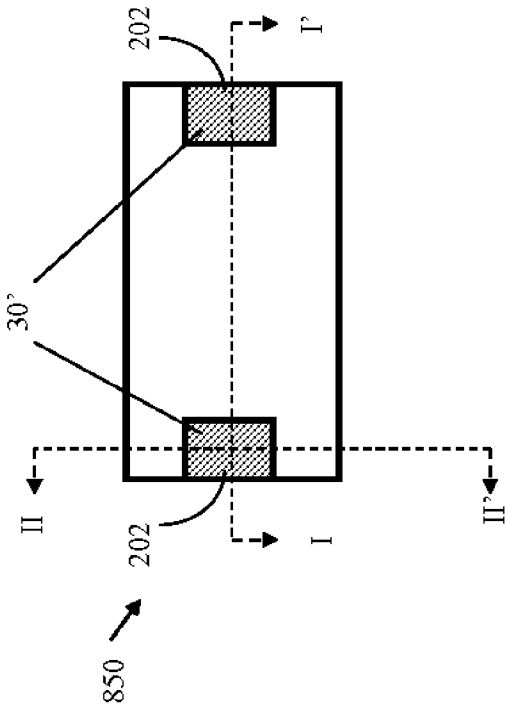


FIG. 132D

850 ↗

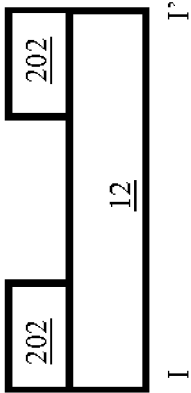


FIG. 132E

850 ↗

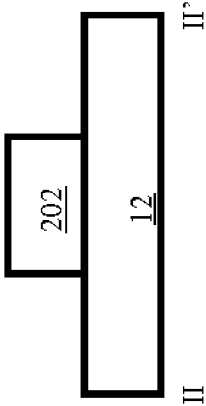


FIG. 132F

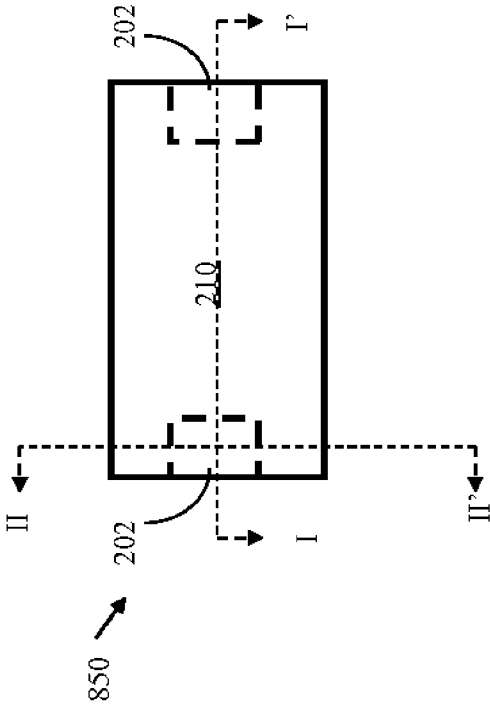


FIG. 132G

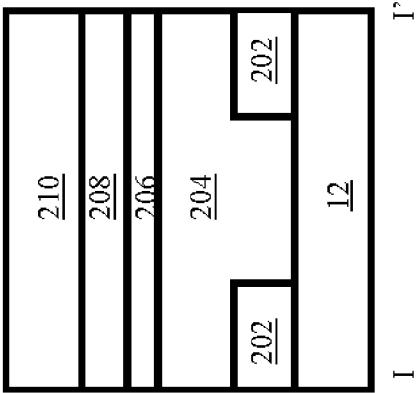


FIG. 132H

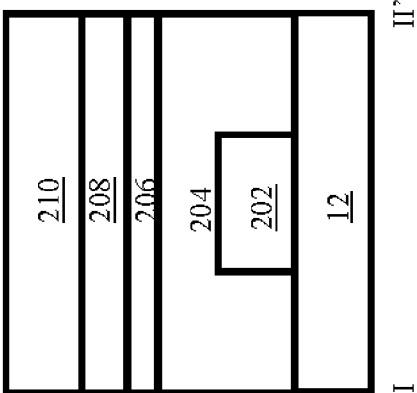


FIG. 132I

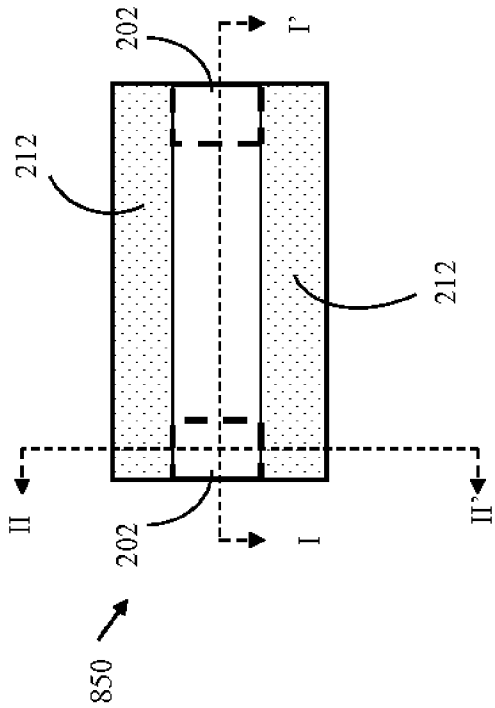


FIG. 132J

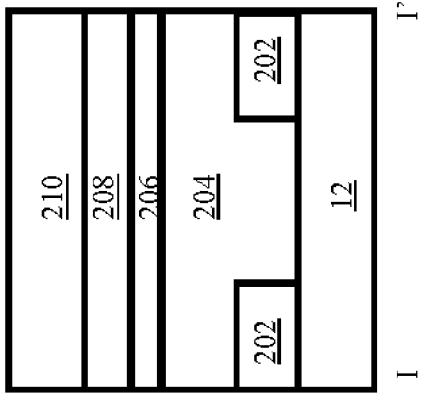


FIG. 132K

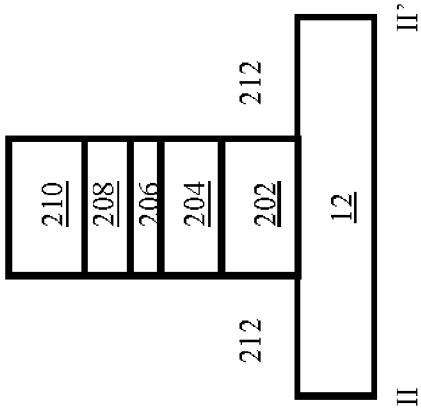


FIG. 132L

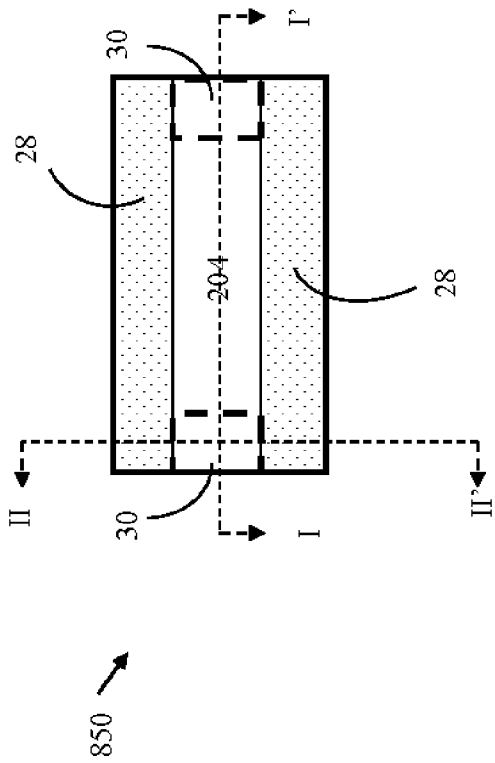


FIG. 132M

850 ↗

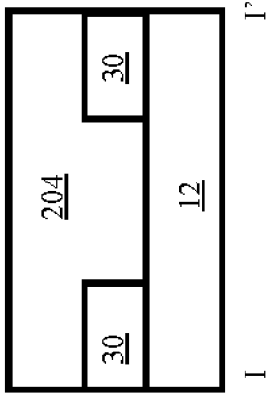


FIG. 132N

850 ↗

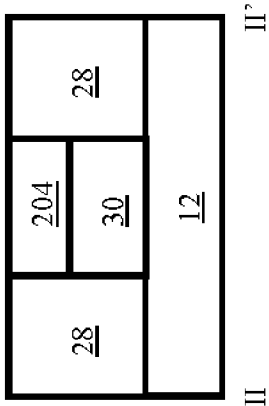


FIG. 132O

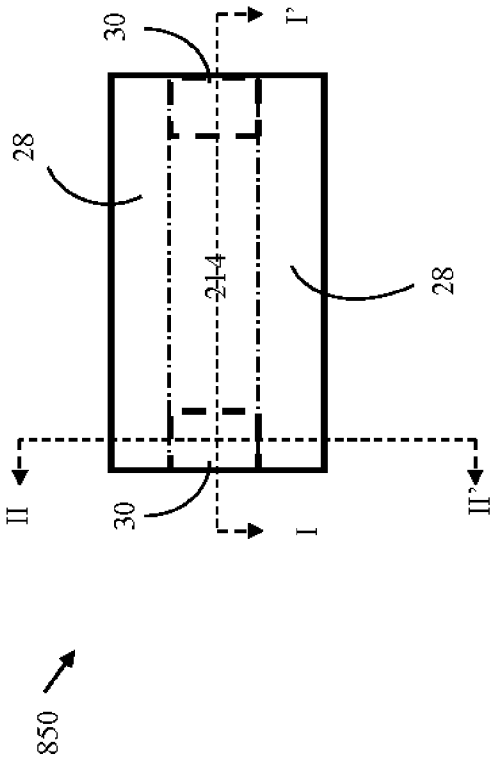


FIG. 132P

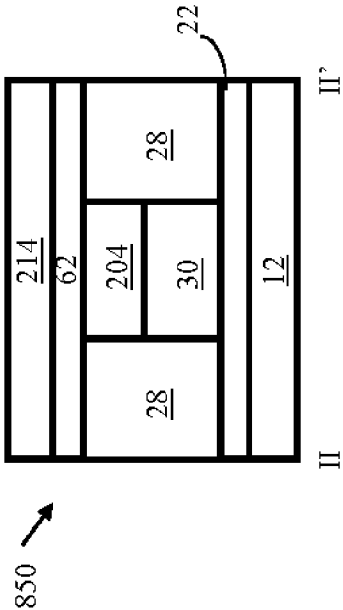


FIG. 132R

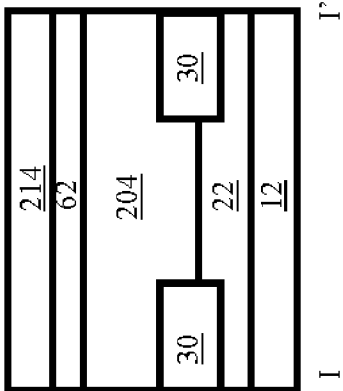


FIG. 132Q

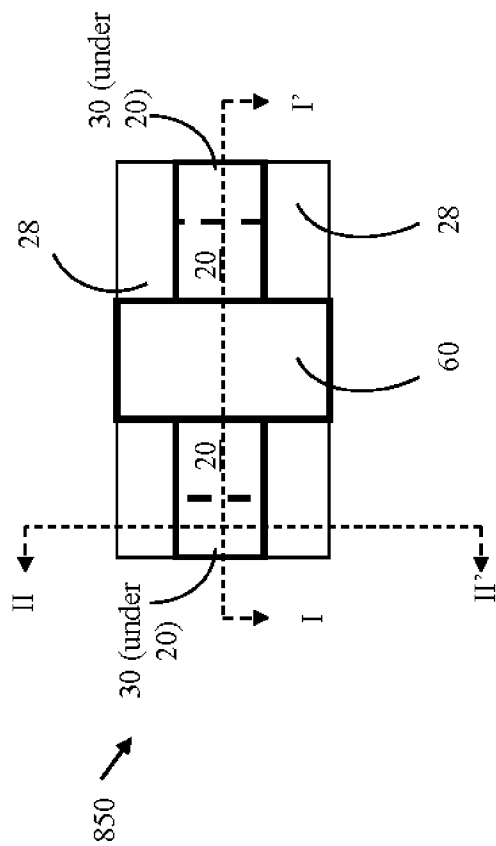


FIG. 132S

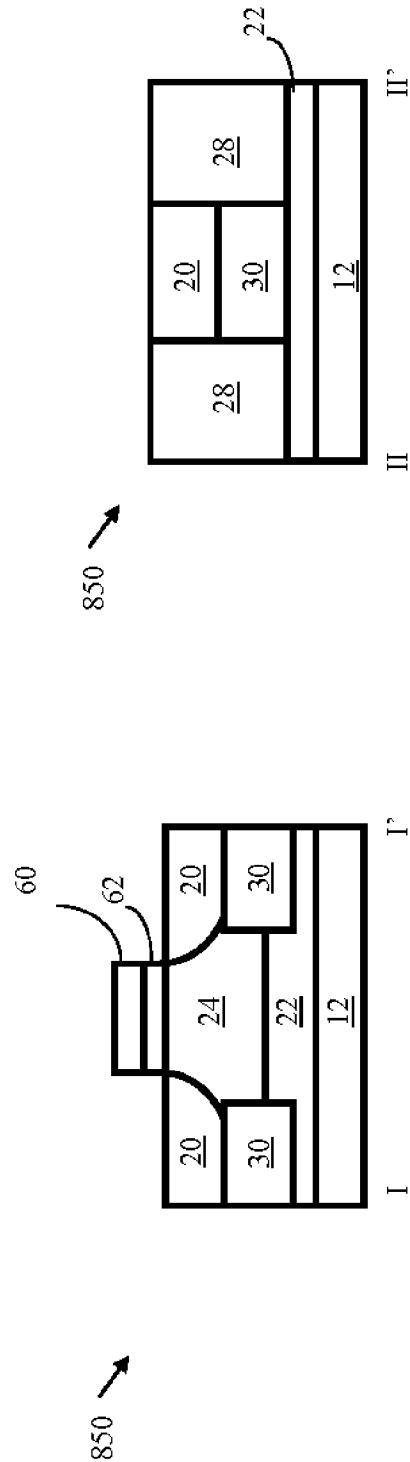


FIG. 132U

FIG. 132T

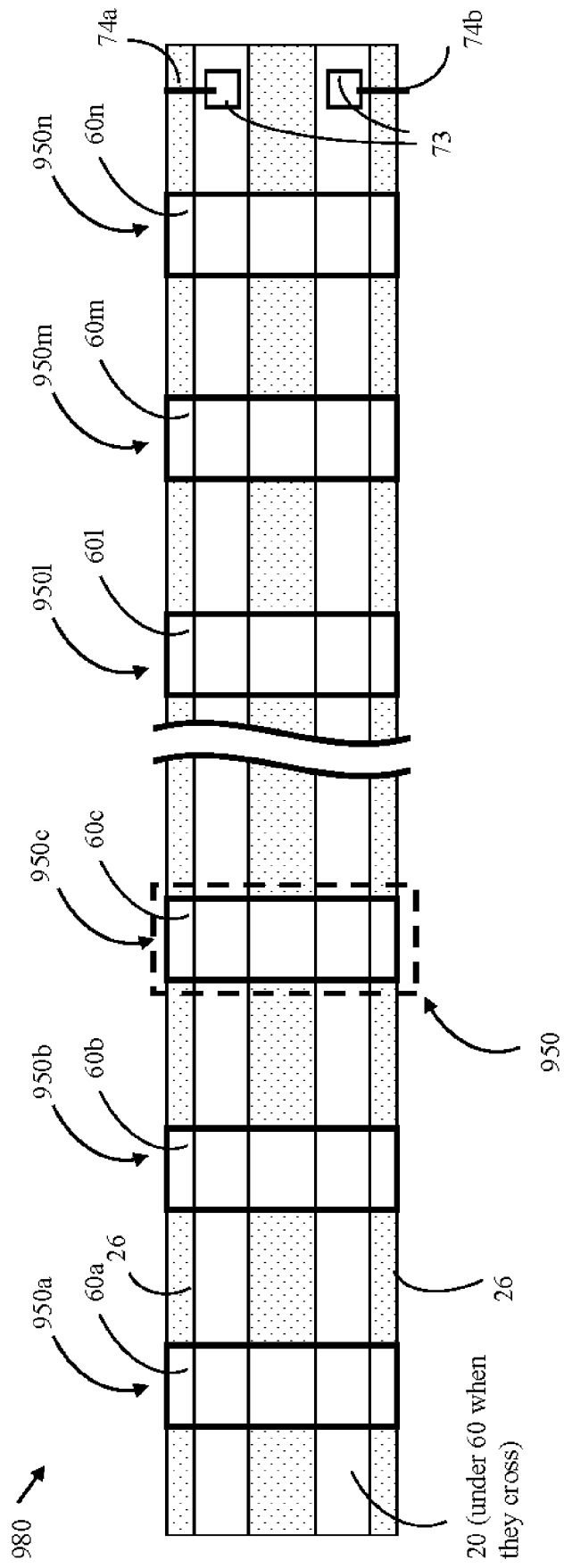
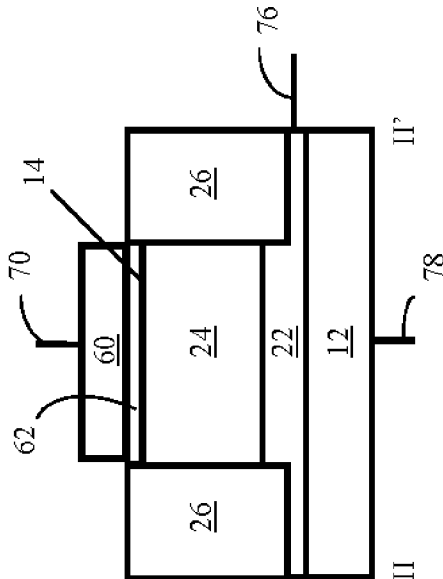
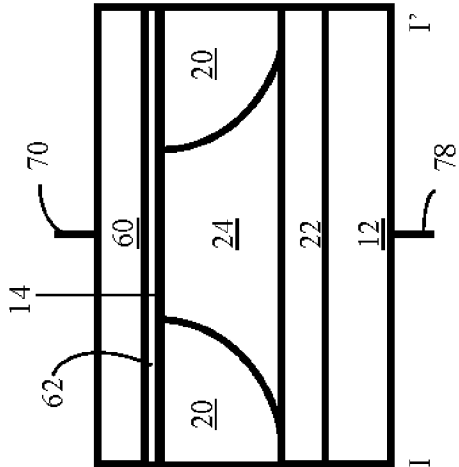
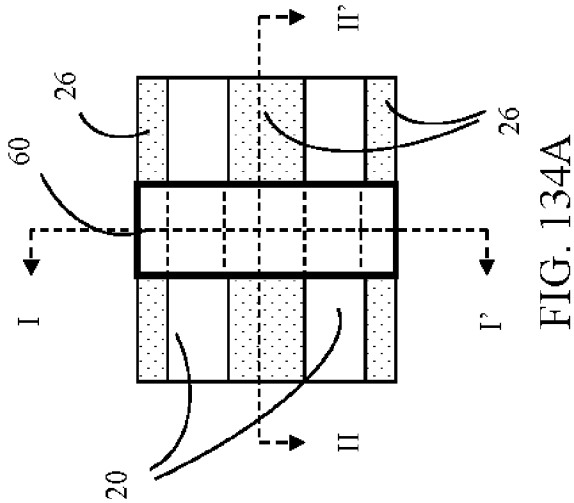


FIG. 133



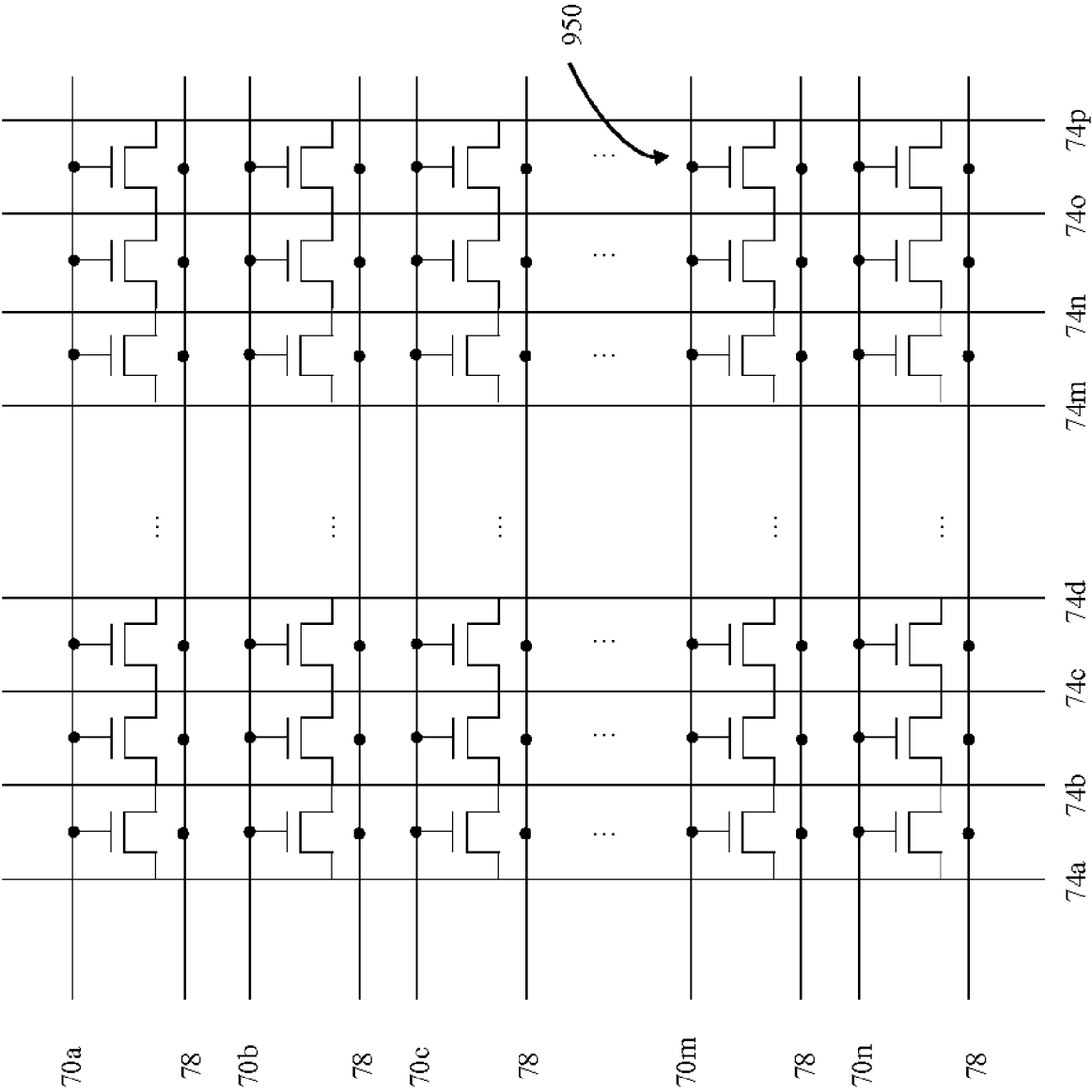


FIG. 135

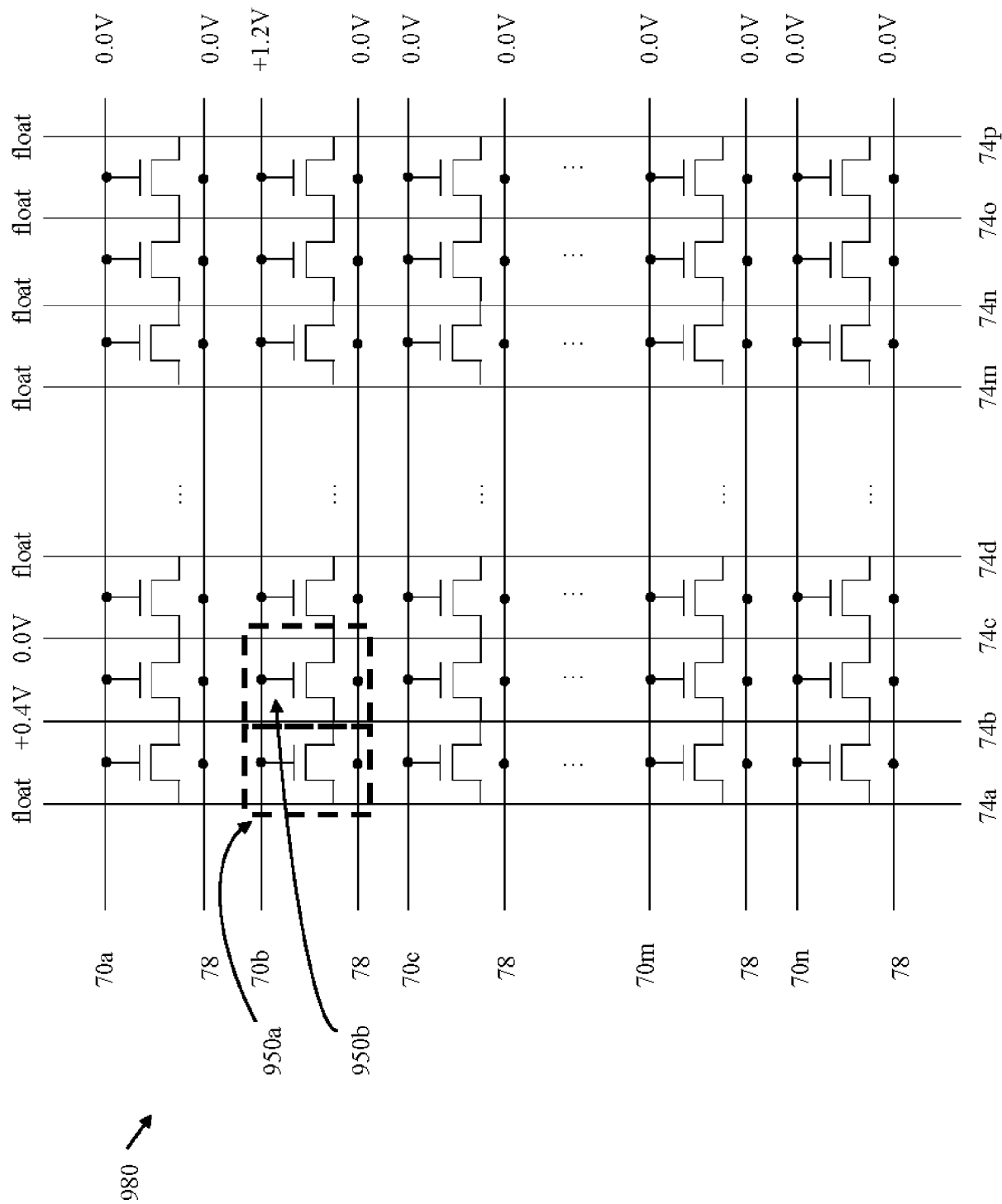


FIG. 136

950b →

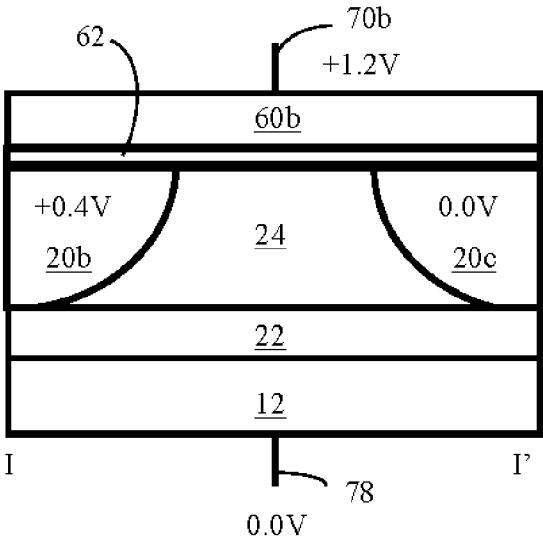


FIG. 137

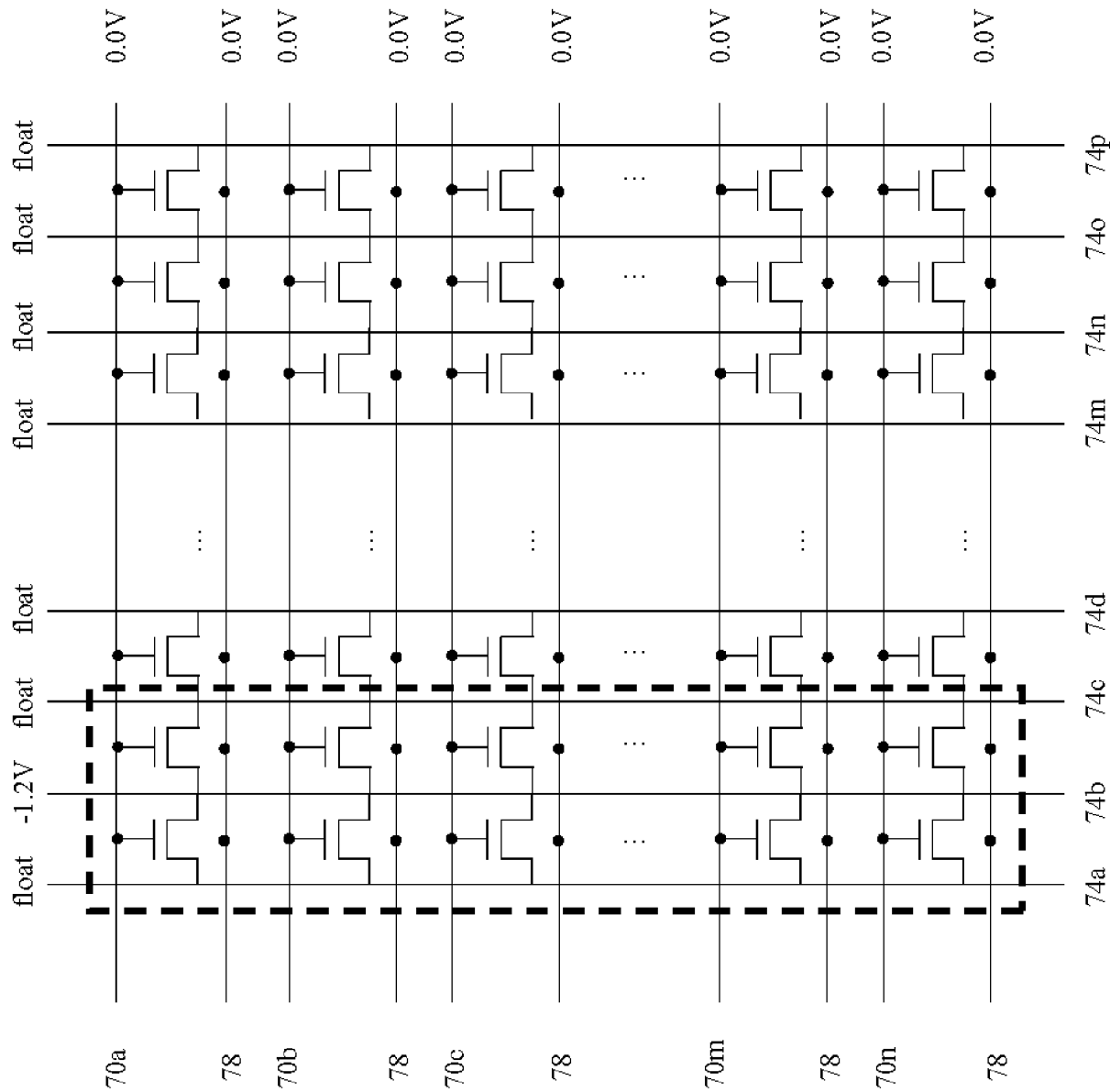


FIG. 138

980 ↗

950b →

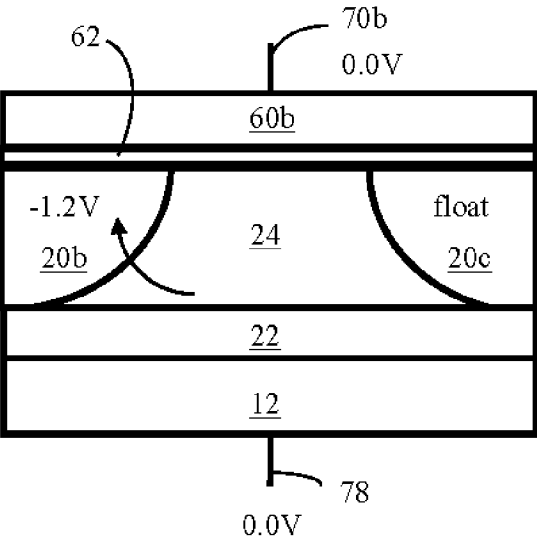


FIG. 139

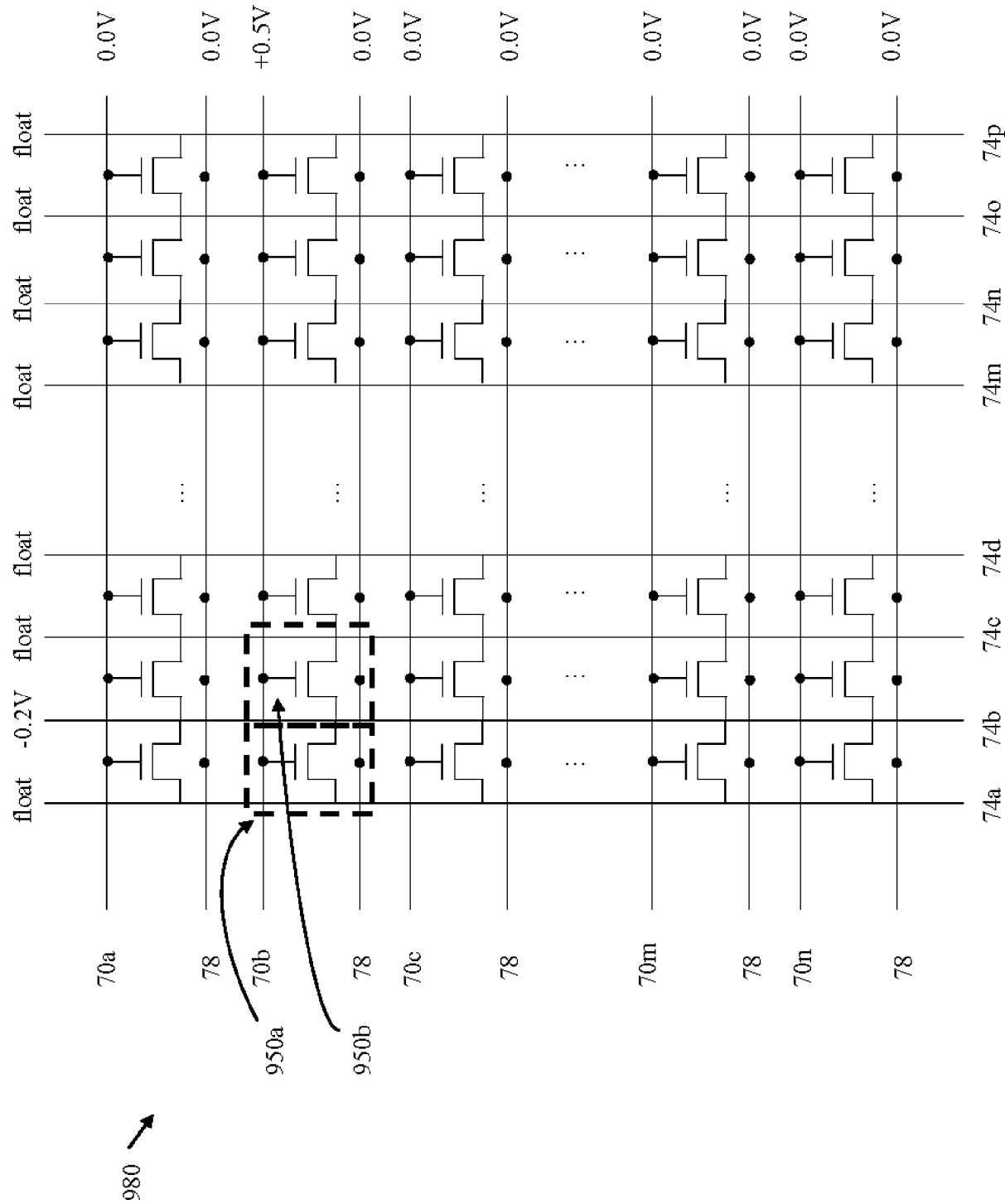


FIG. 140

950b →

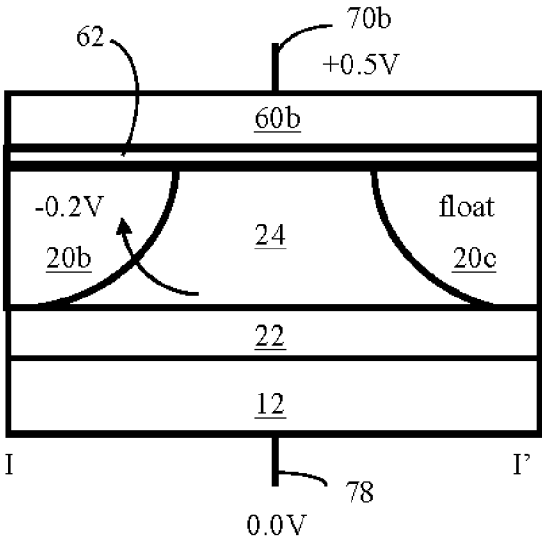
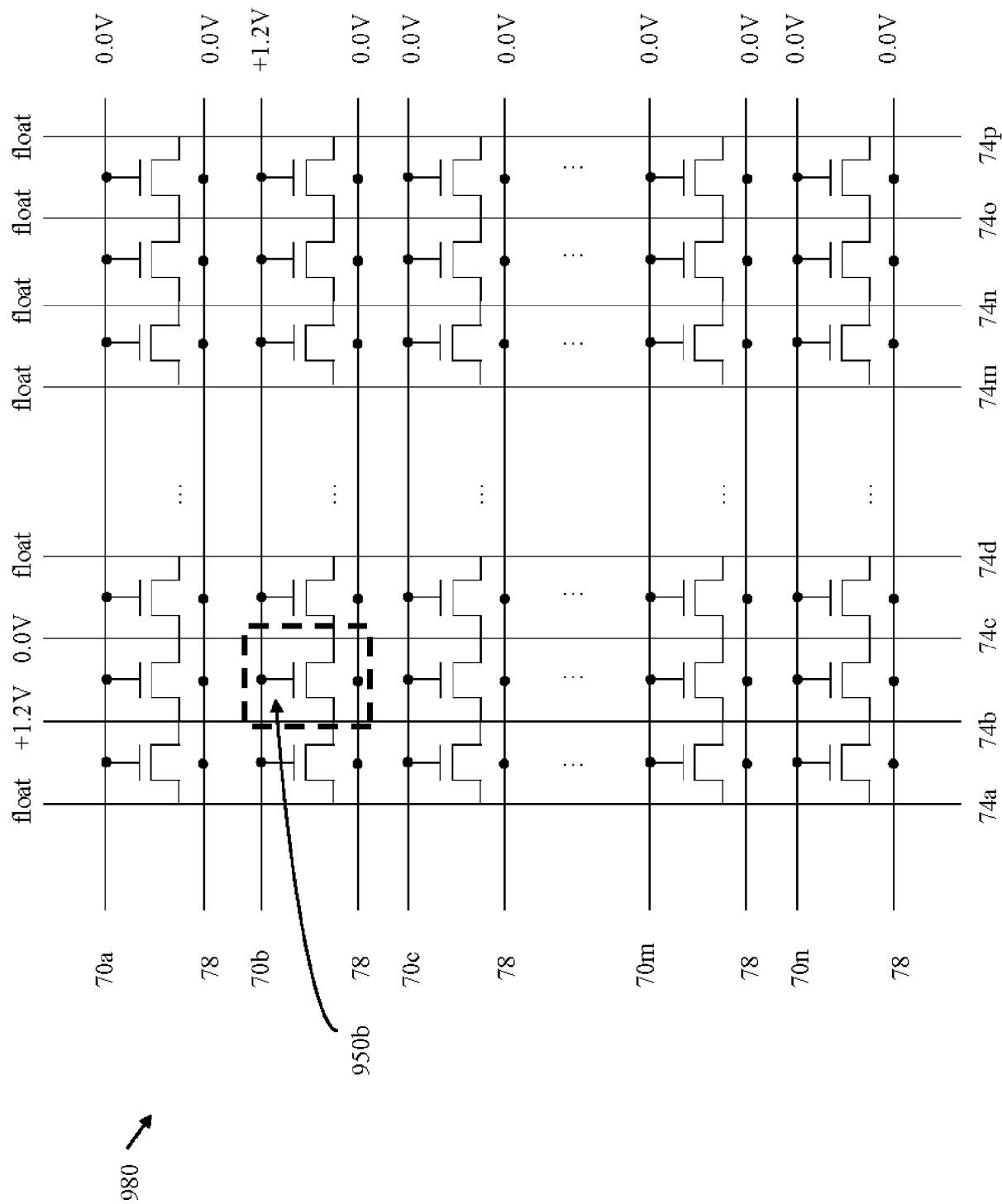


FIG. 141



950b →

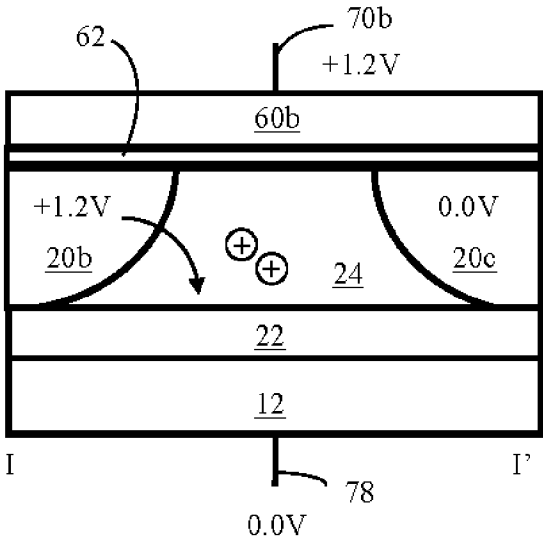


FIG. 143

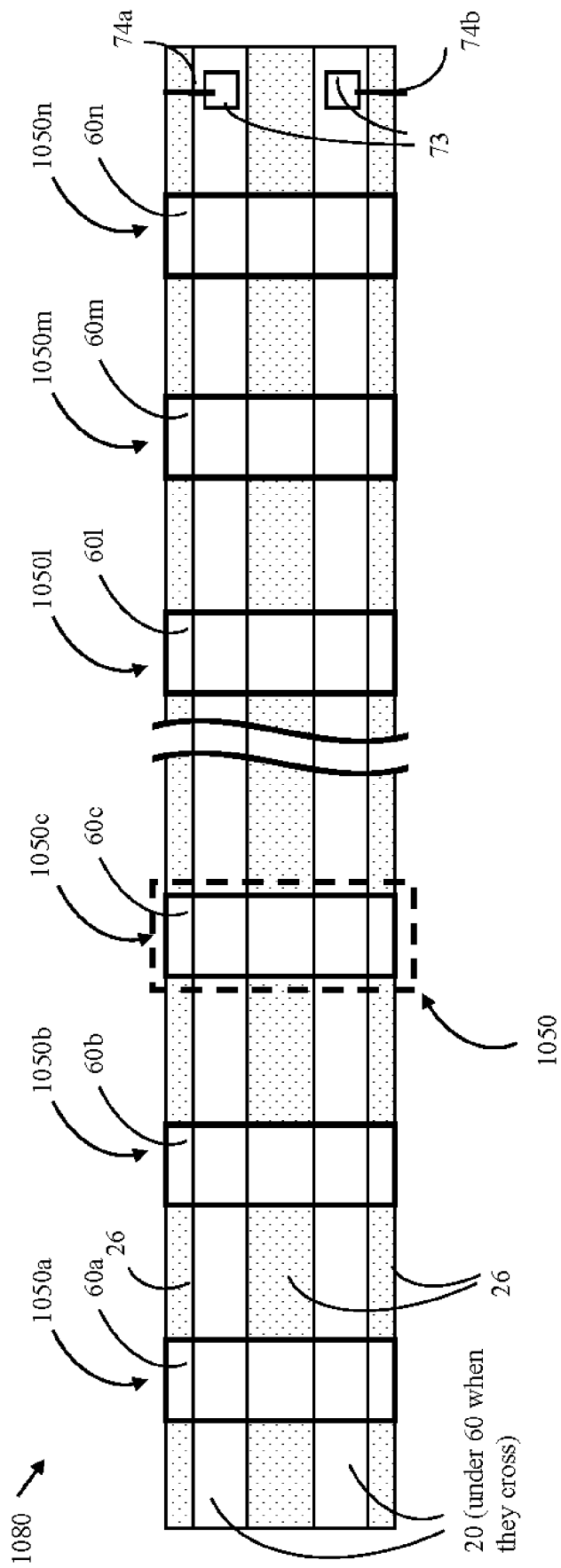


FIG. 144

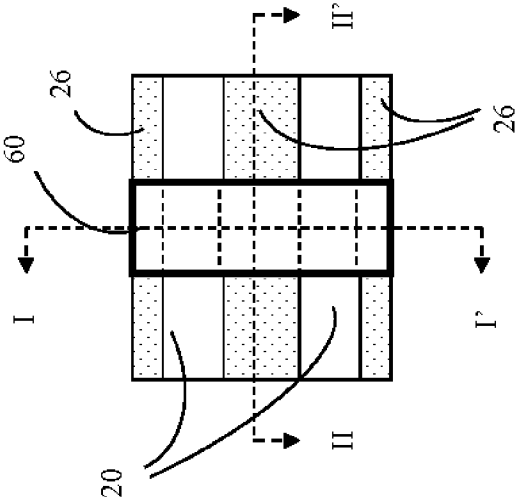


FIG. 145A

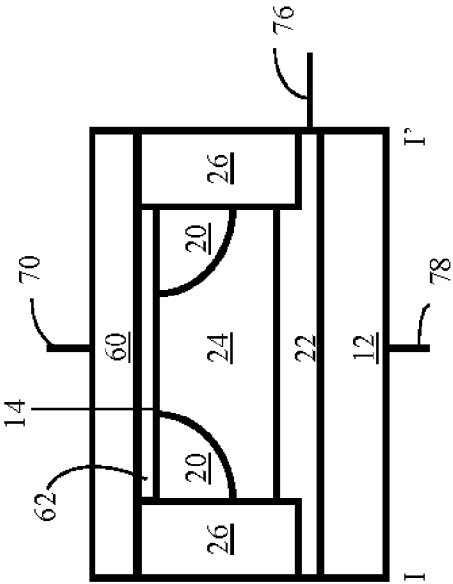


FIG. 145B

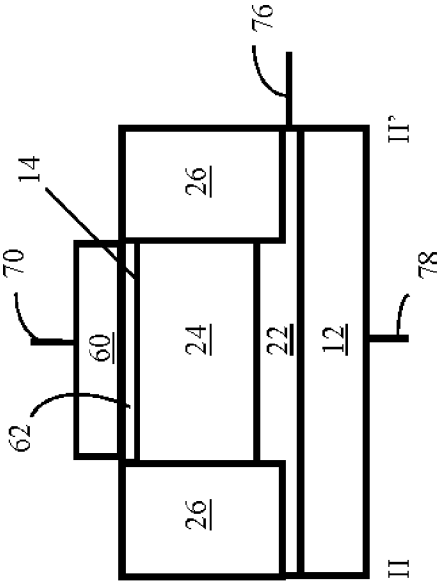


FIG. 145C

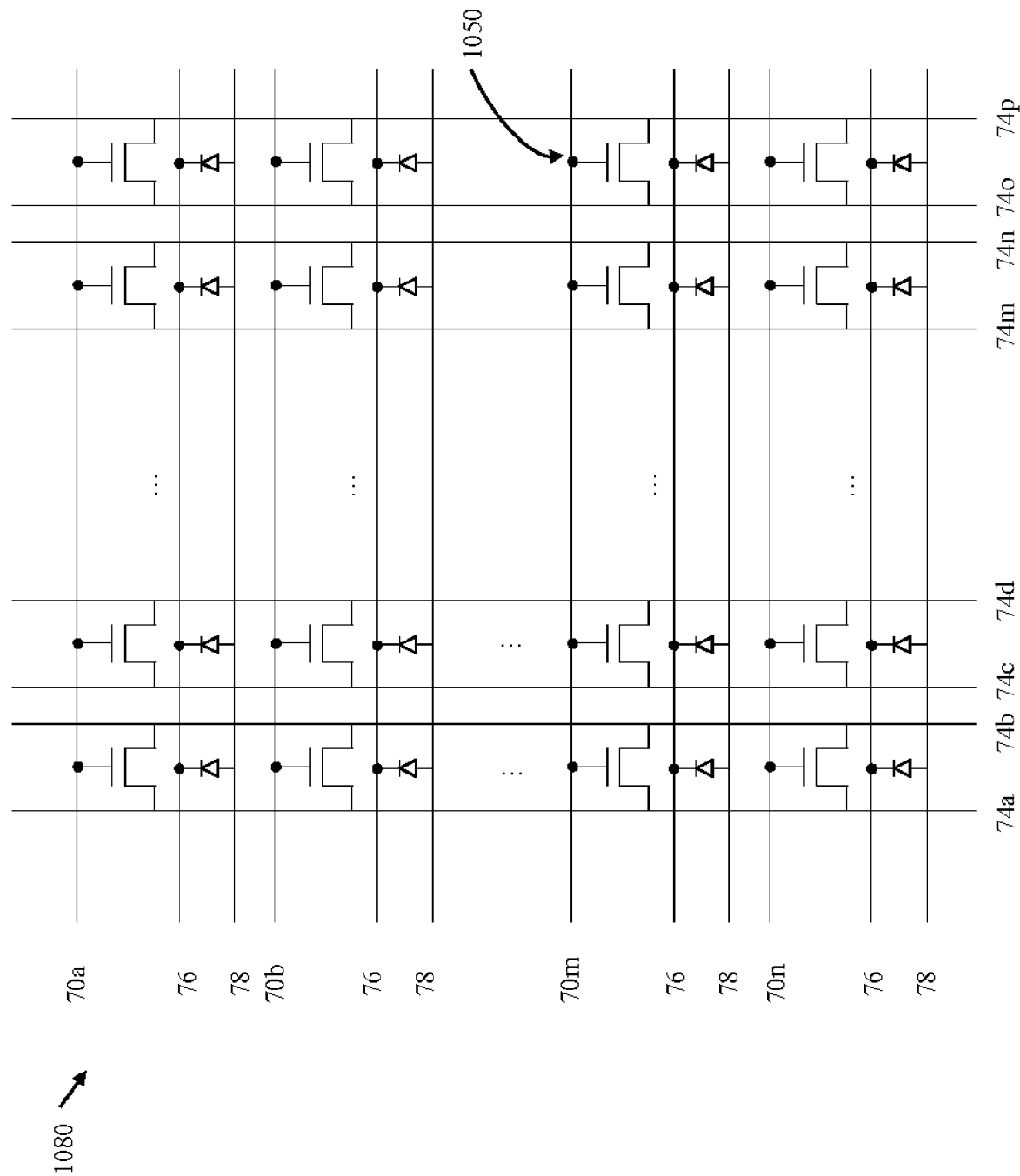


FIG. 146

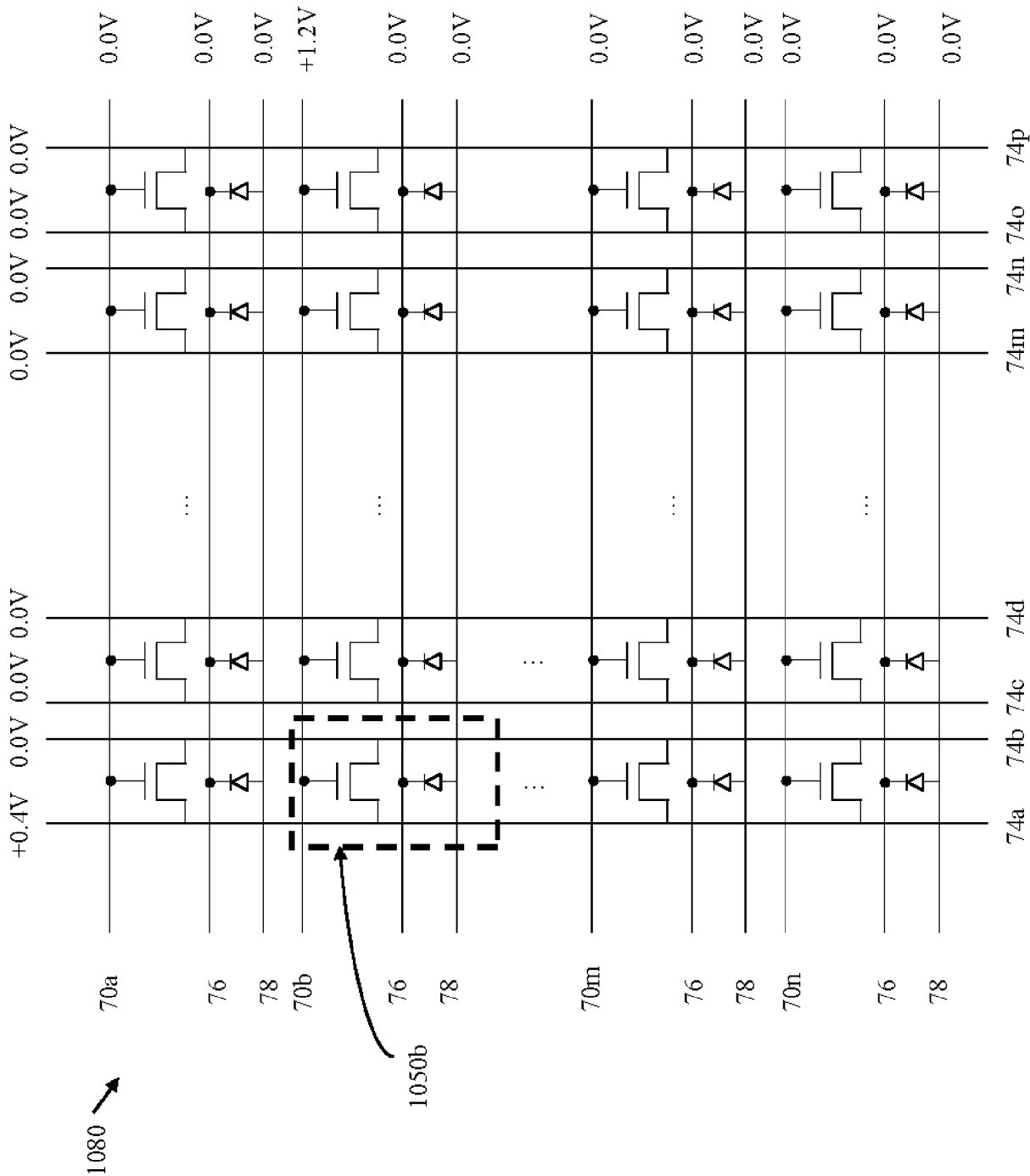


FIG. 147

1050b

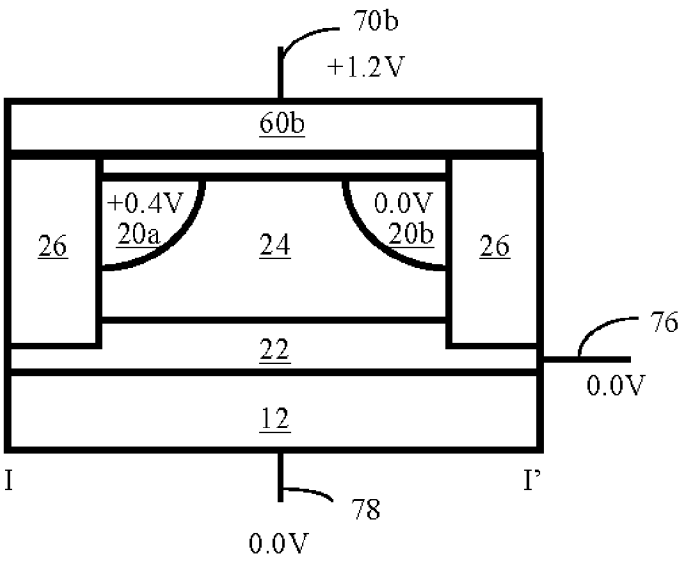


FIG. 148

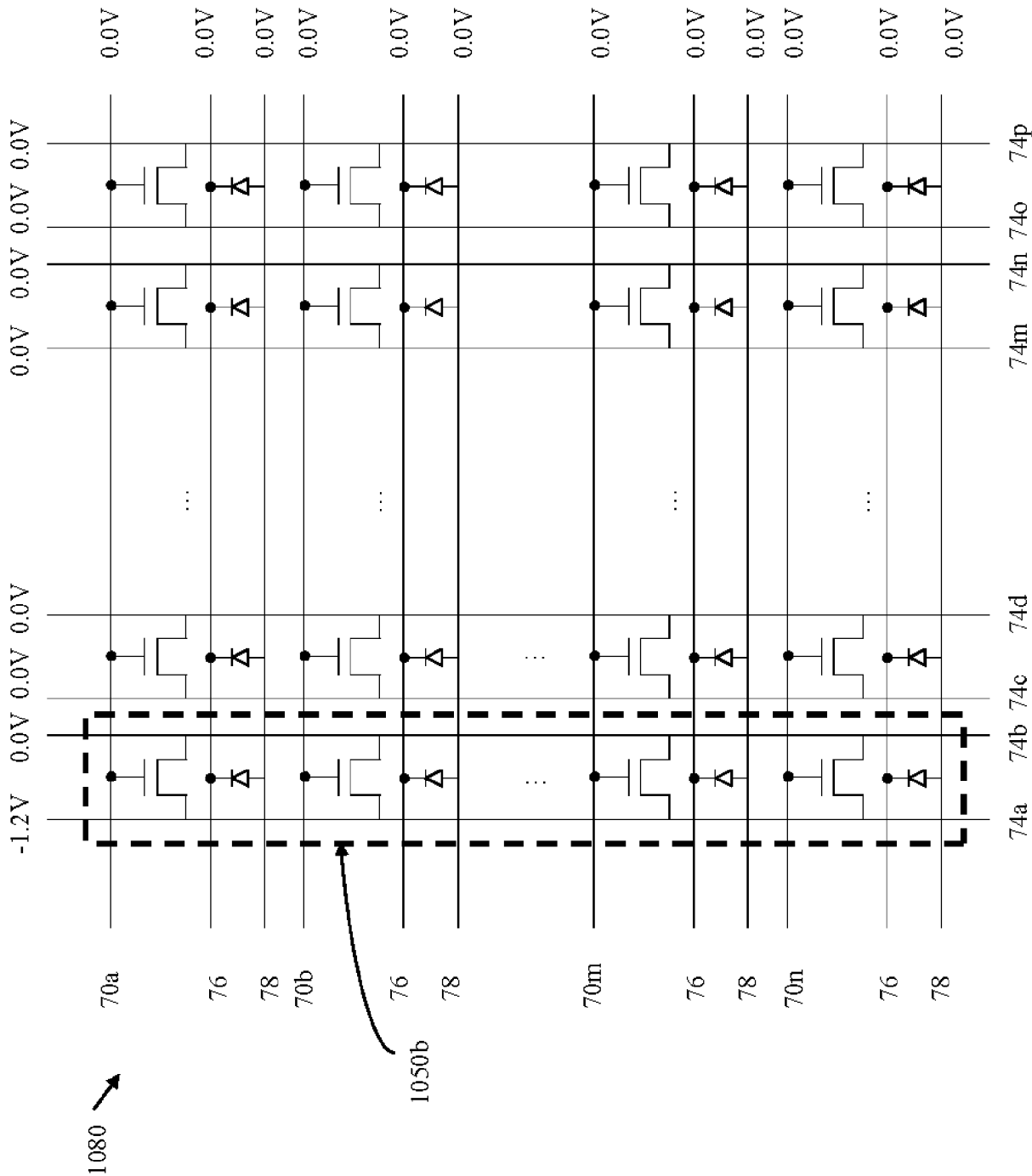


FIG. 149

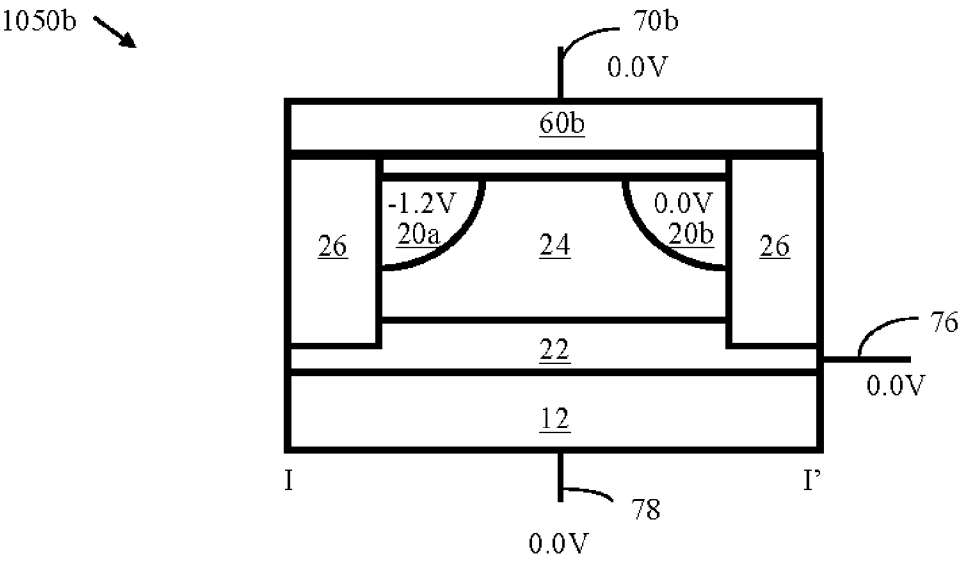


FIG. 150

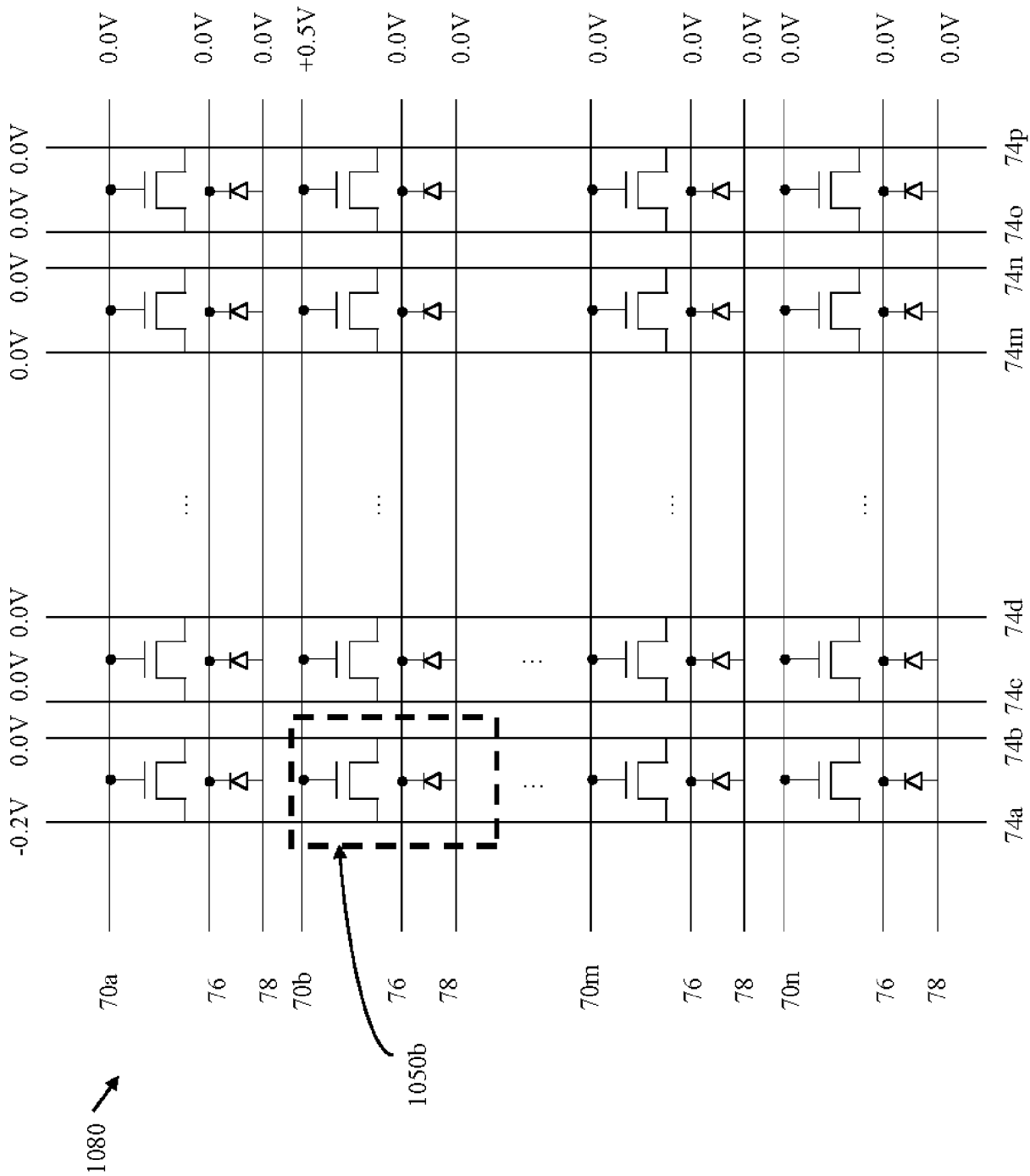


FIG. 151

1050b →

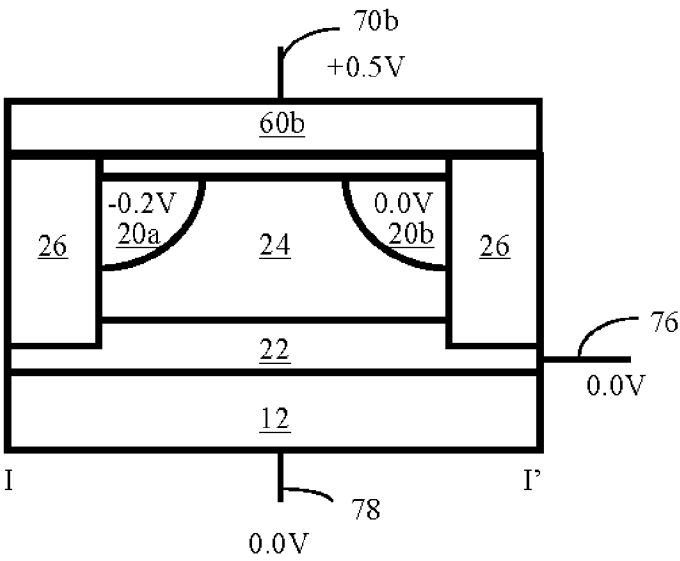


FIG. 152

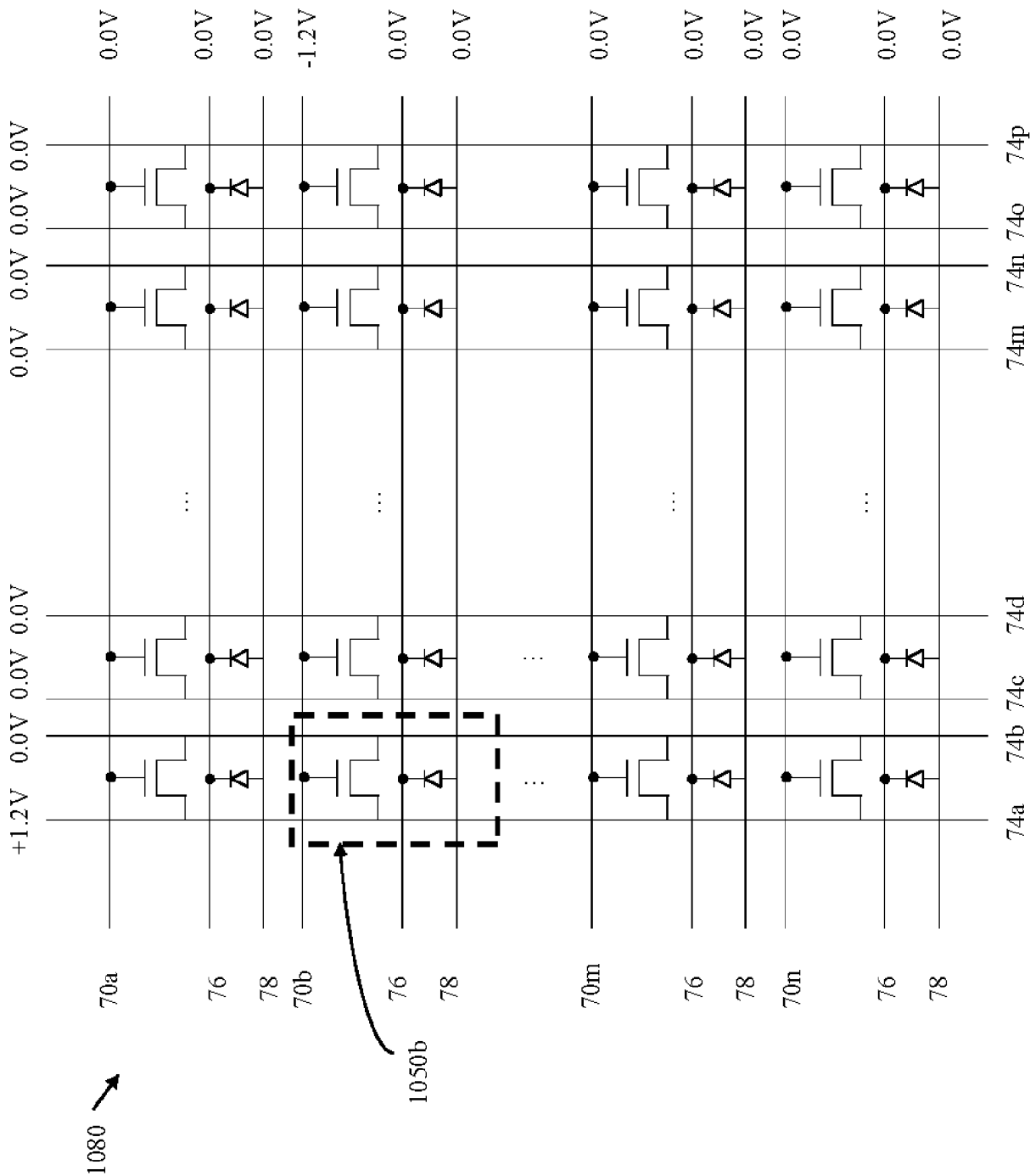


FIG. 153

1050b

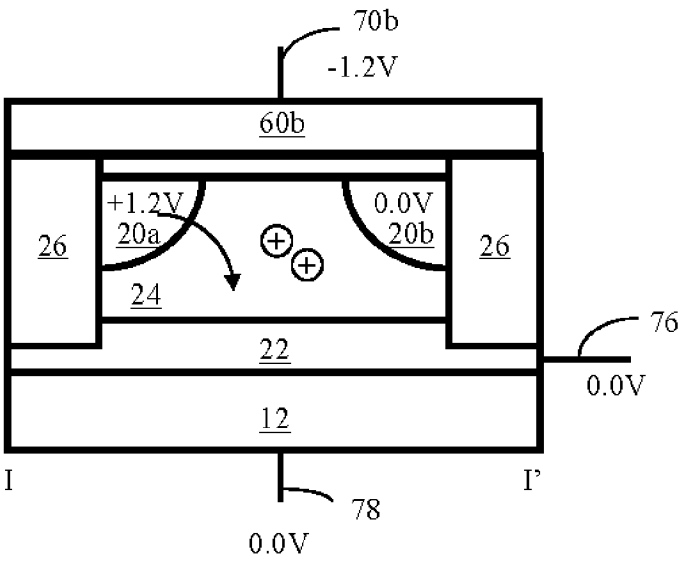


FIG. 154

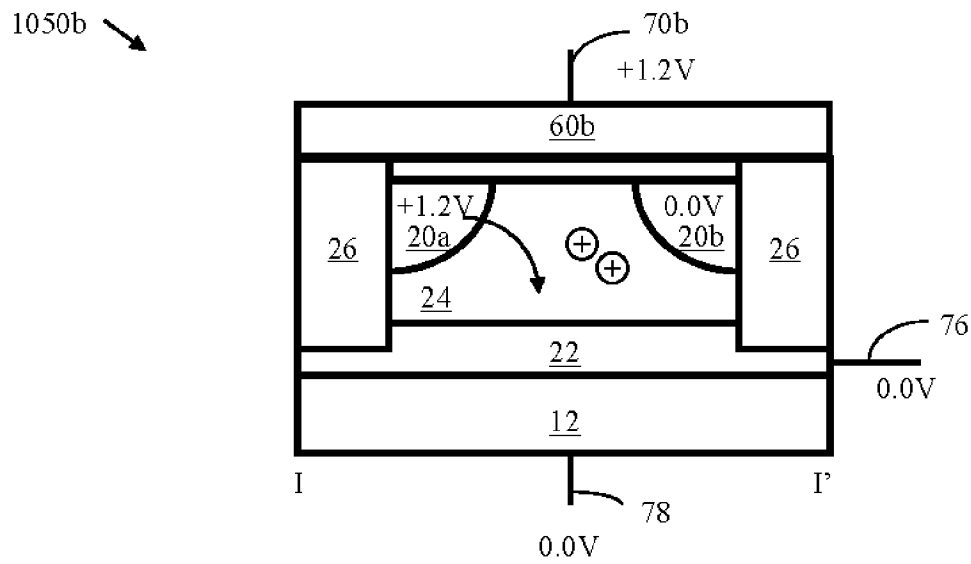


FIG. 156

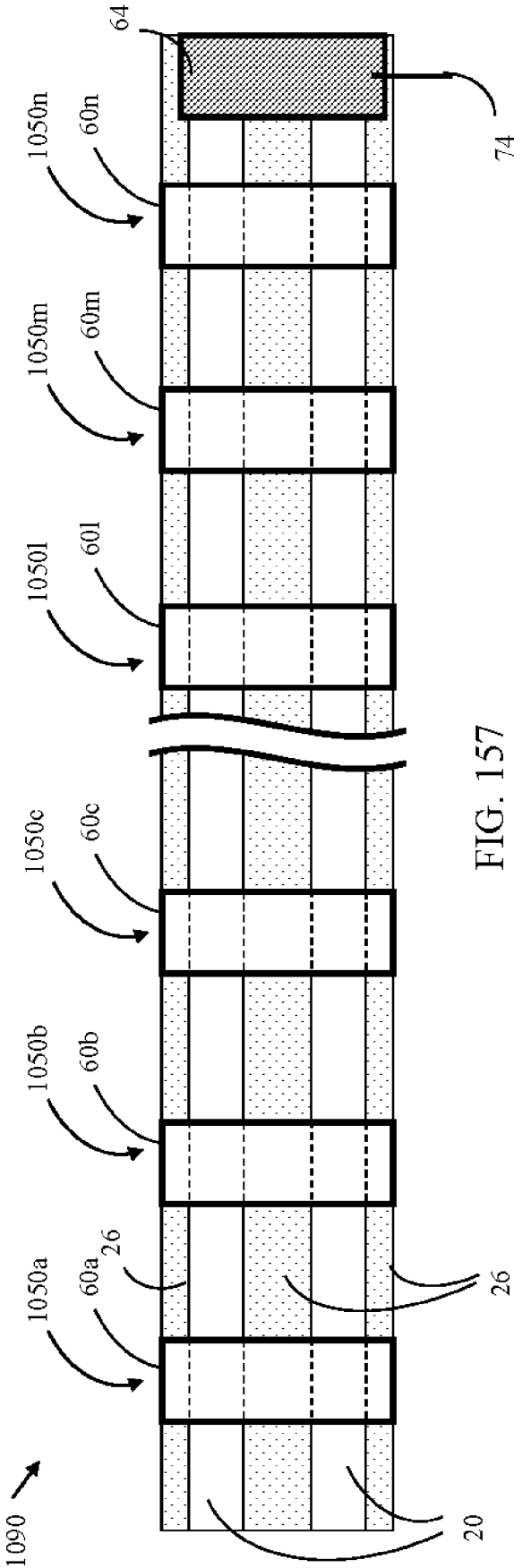


FIG. 157

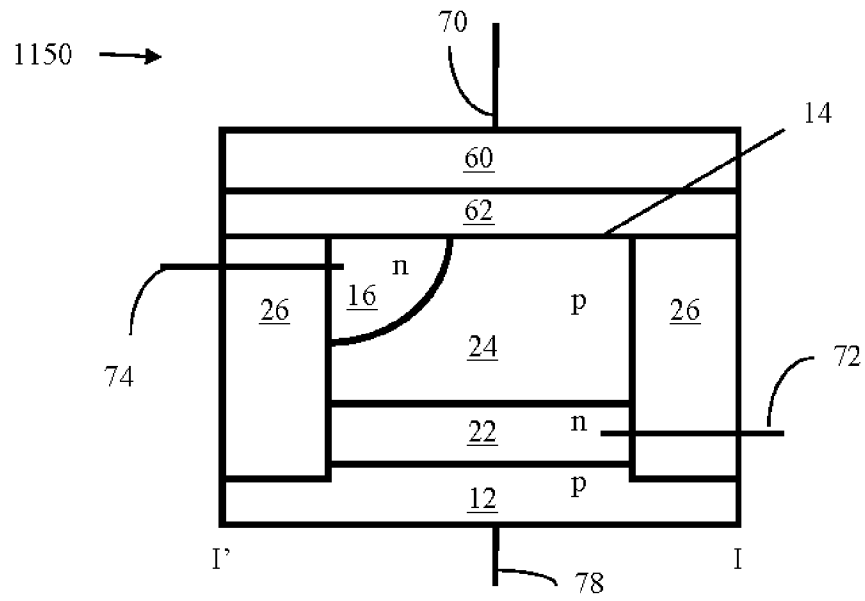


FIG. 158C

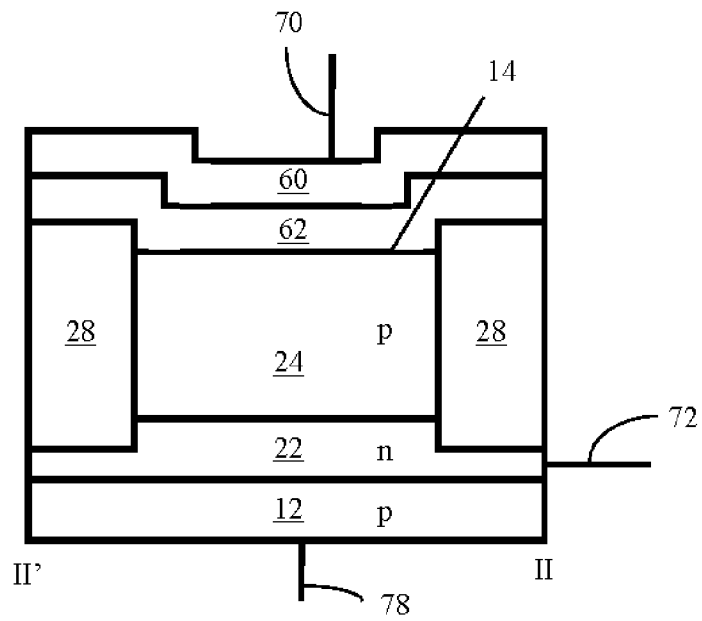


FIG. 158D

1180

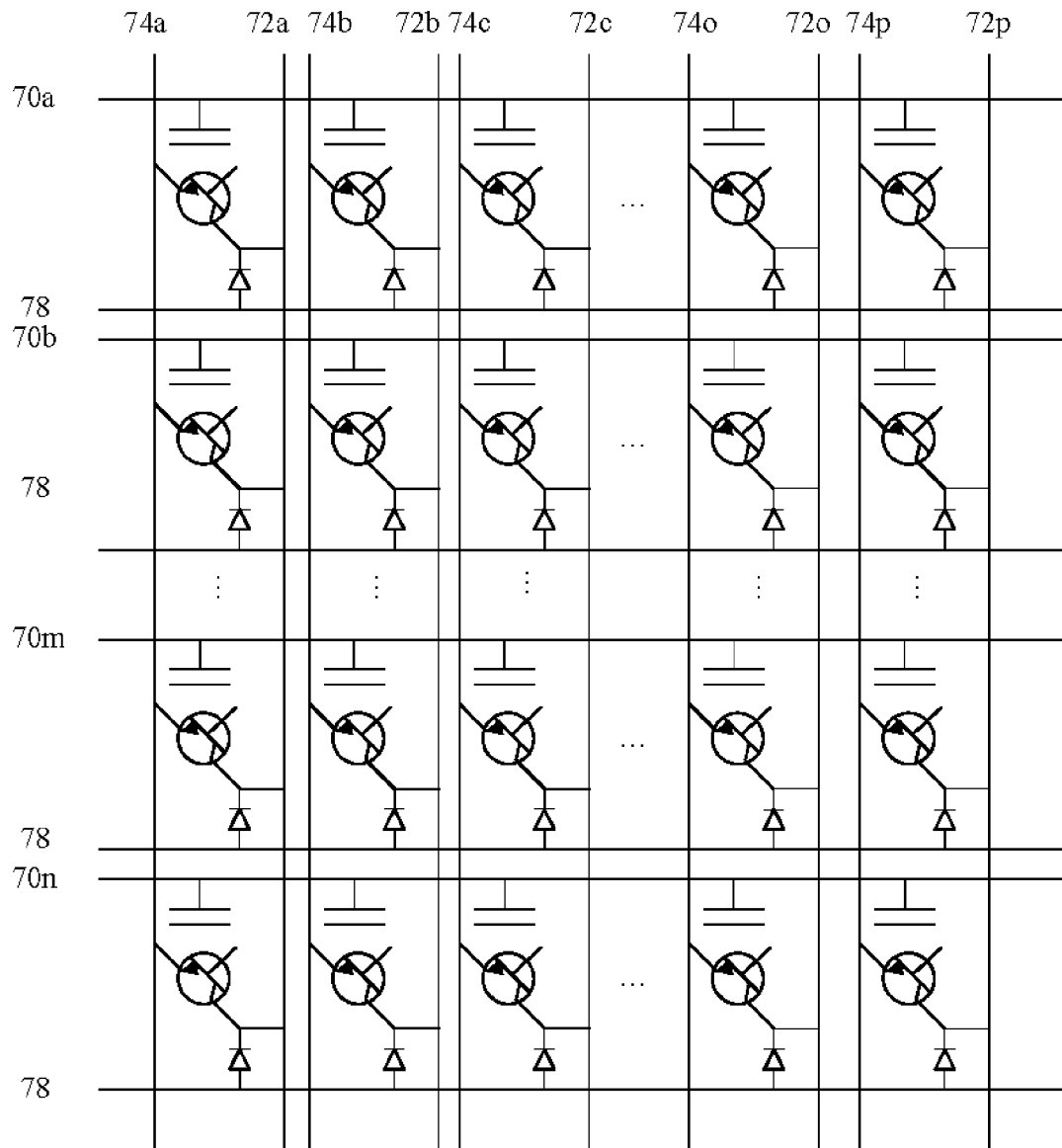


FIG. 159

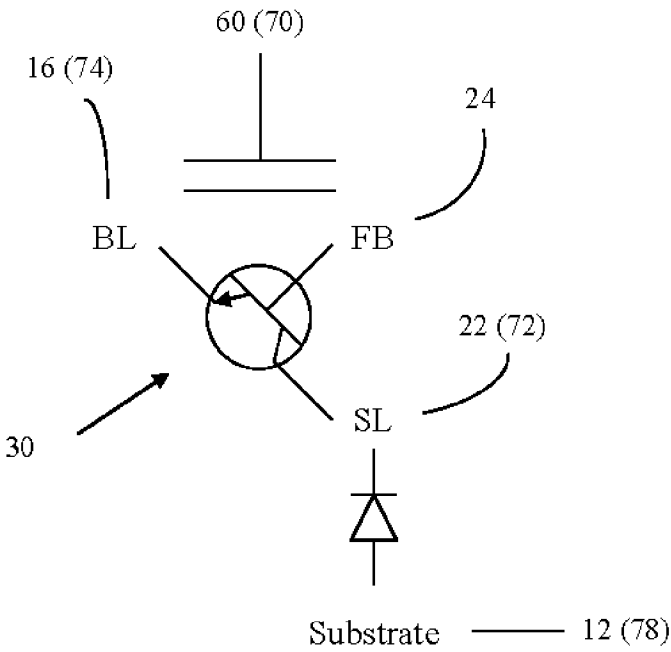


FIG. 160A

Floating Body 24 is positively charged

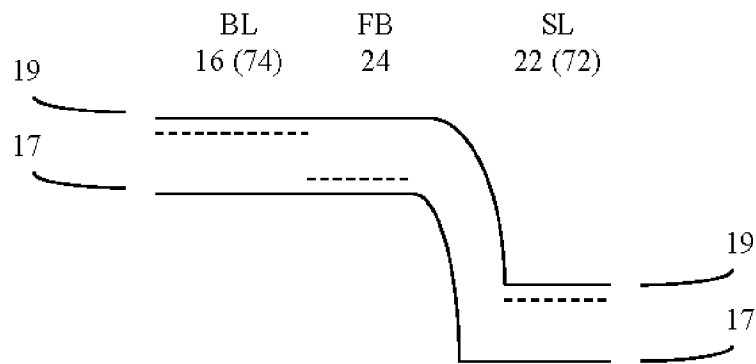


FIG. 160B

FB is neutrally charged: $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

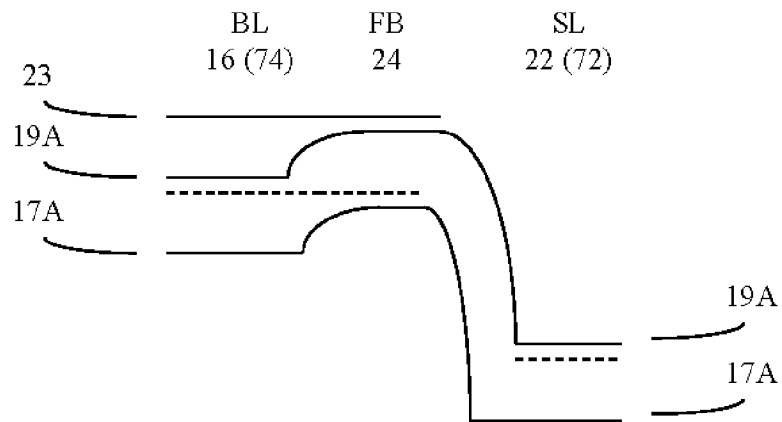


FIG. 160C

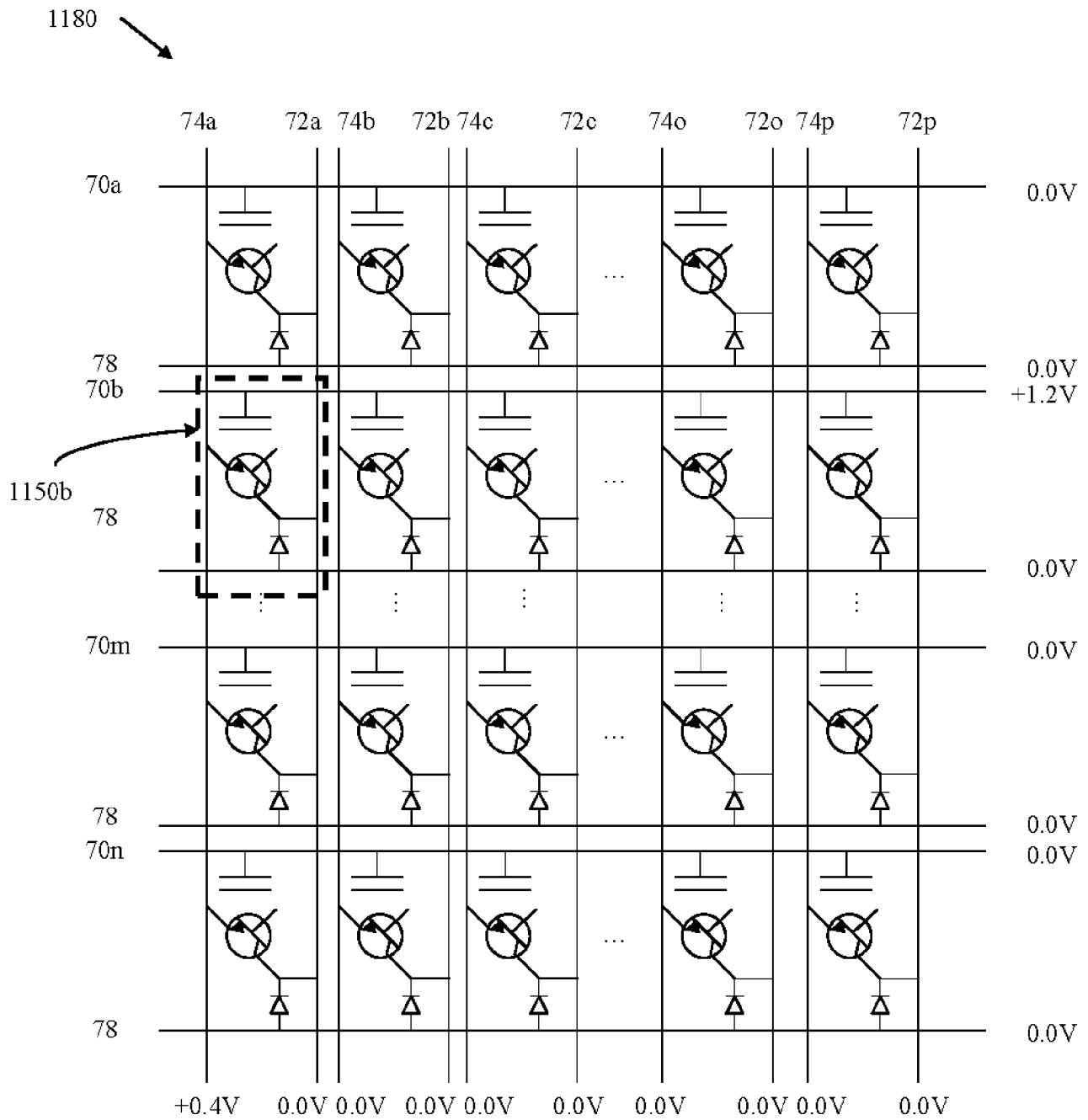


FIG. 161

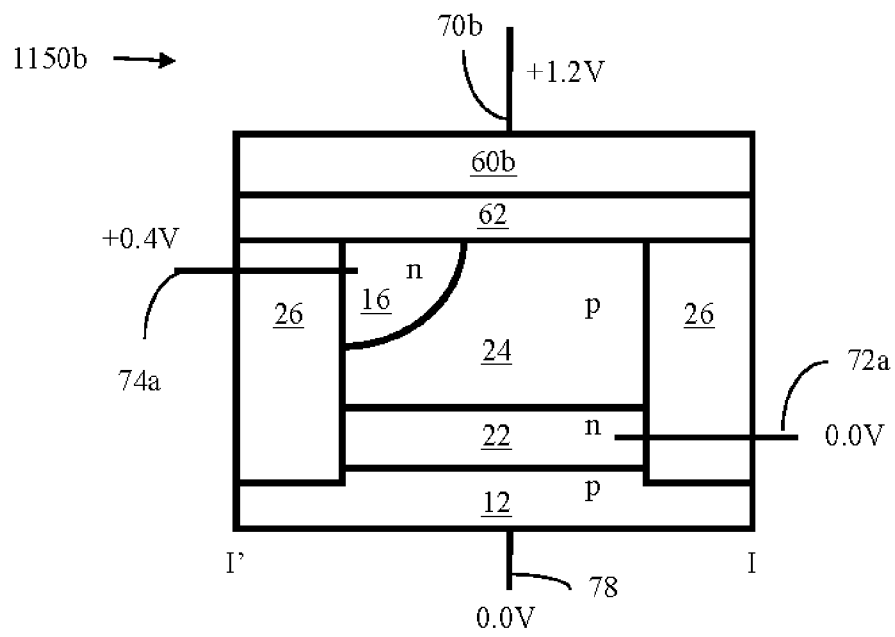


FIG. 162

1180

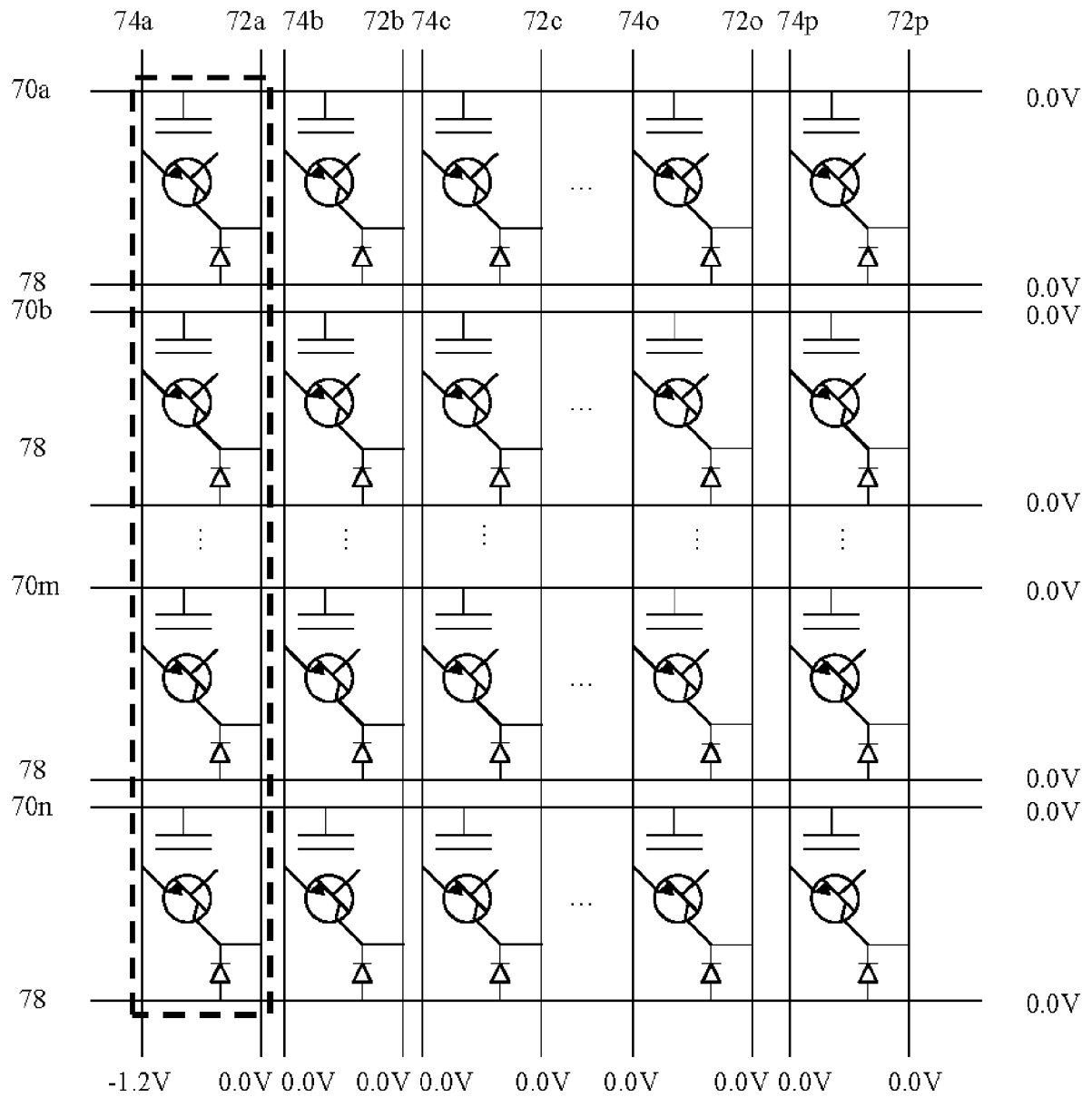


FIG. 163

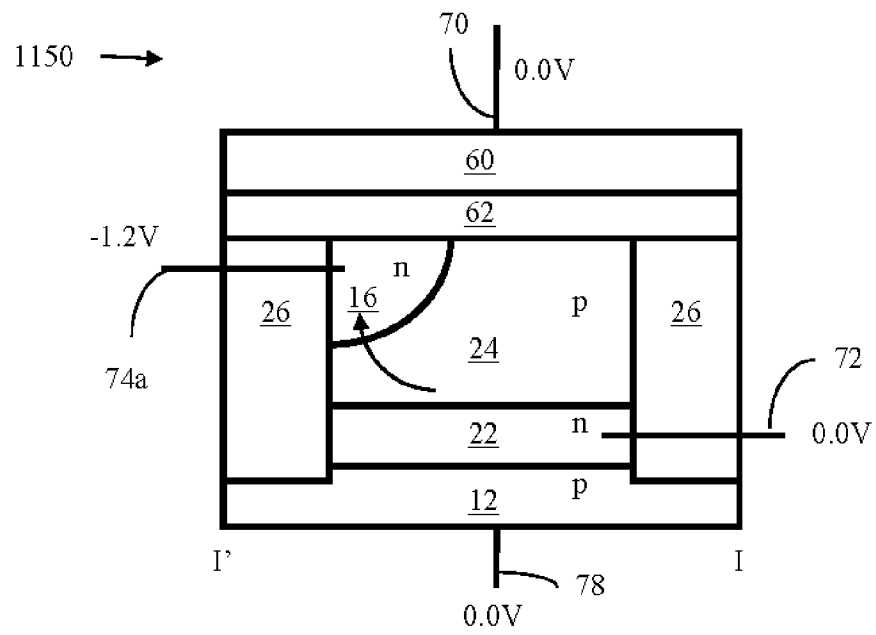


FIG. 164

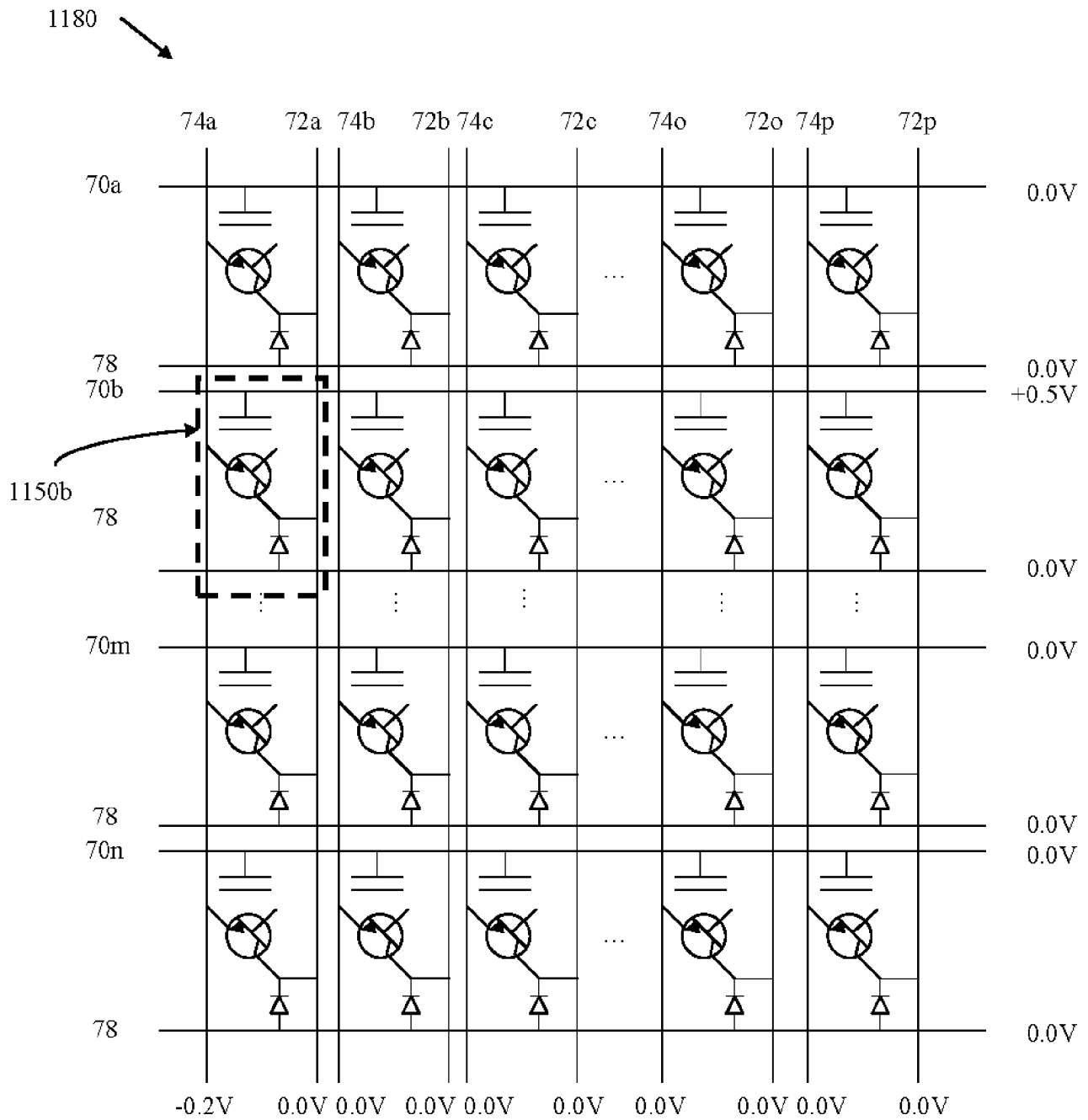


FIG. 165

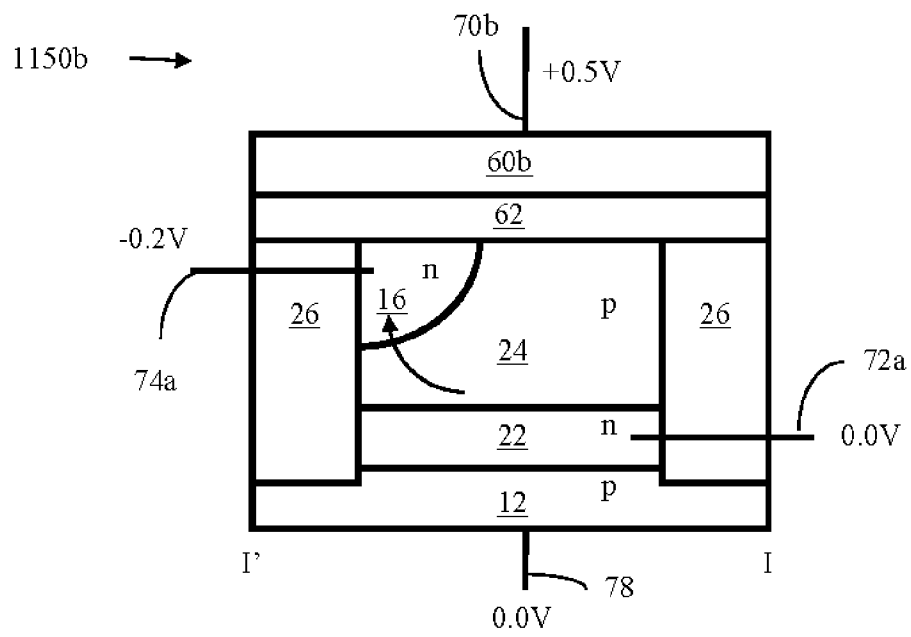


FIG. 166

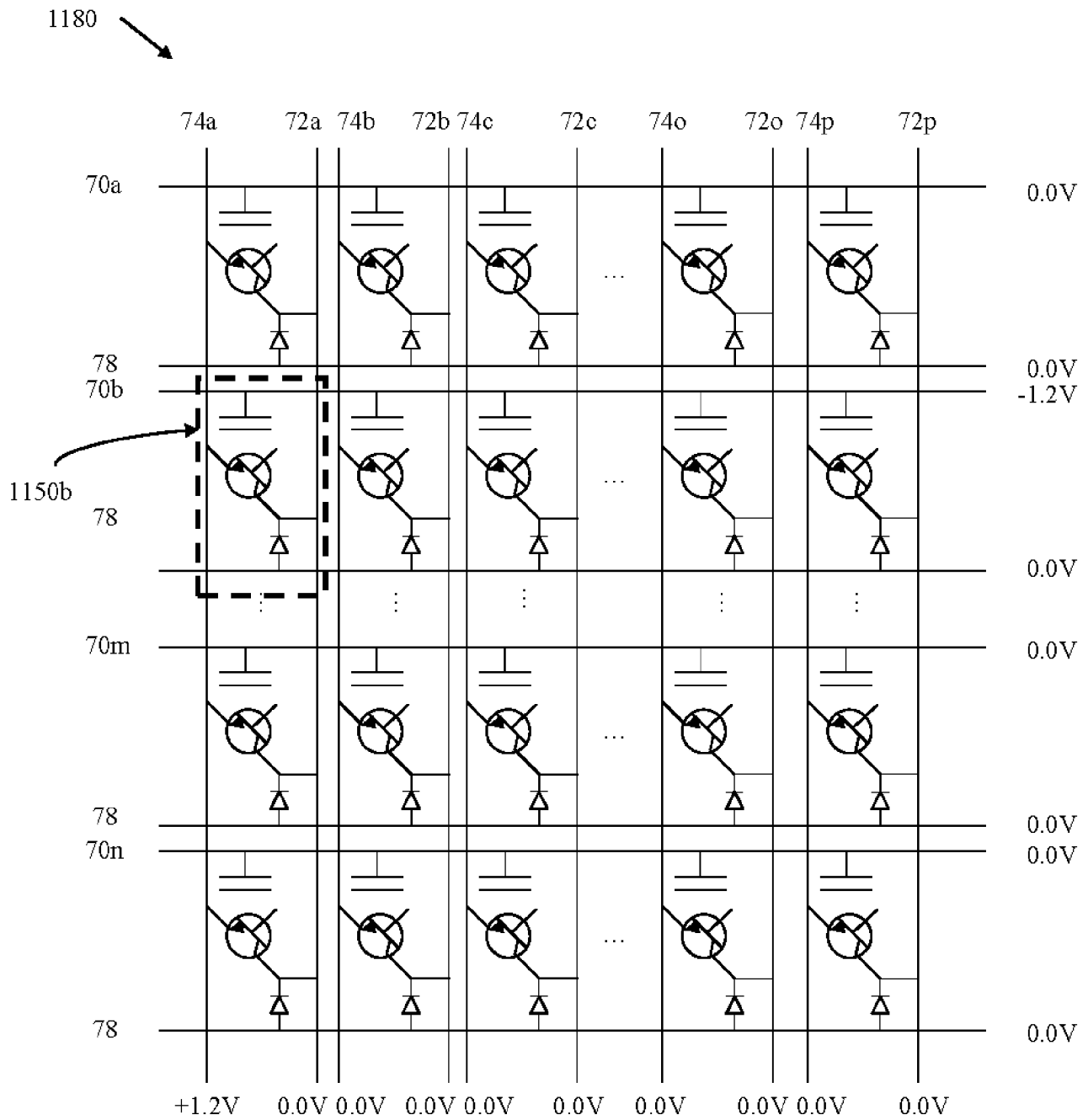


FIG. 167

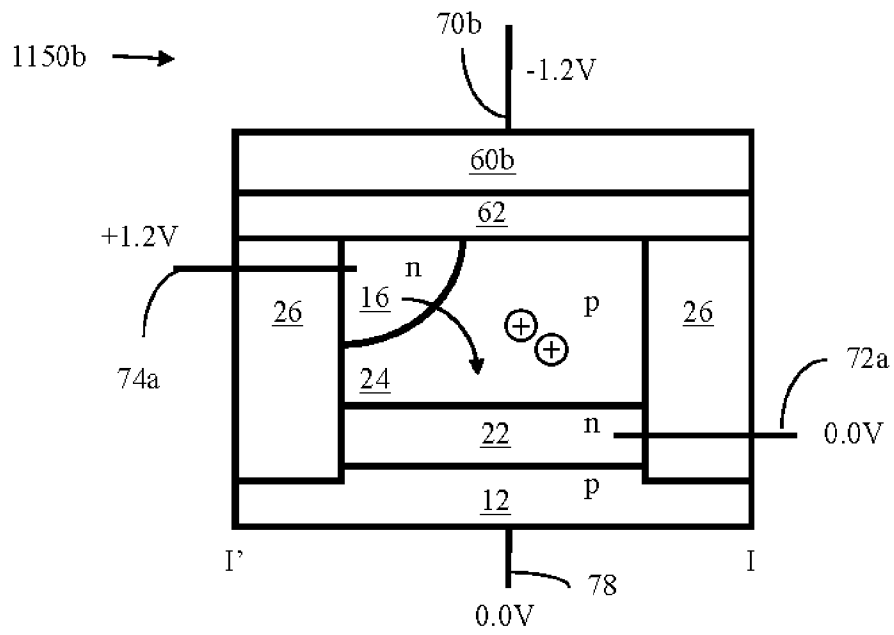


FIG. 168

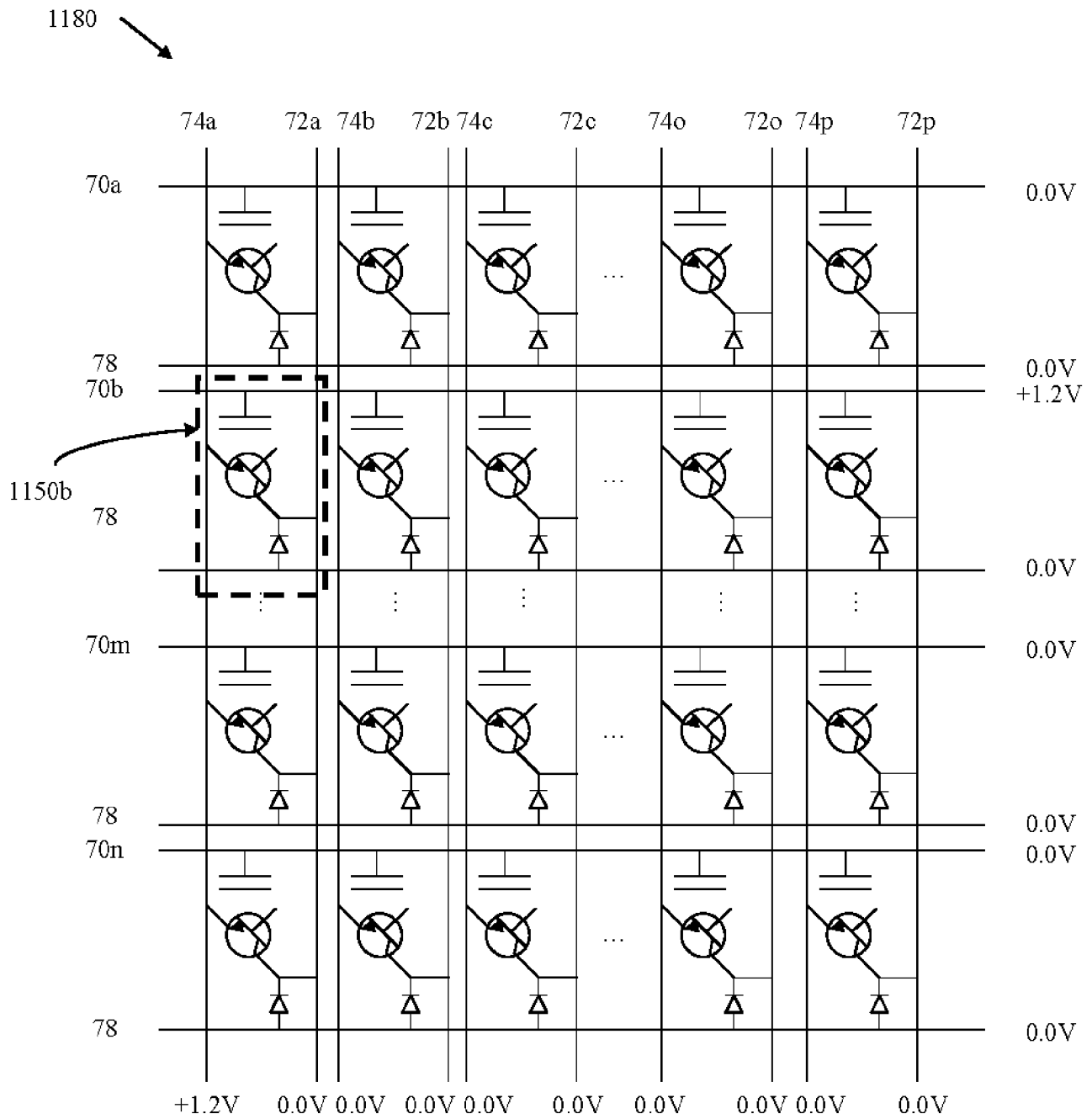


FIG. 169

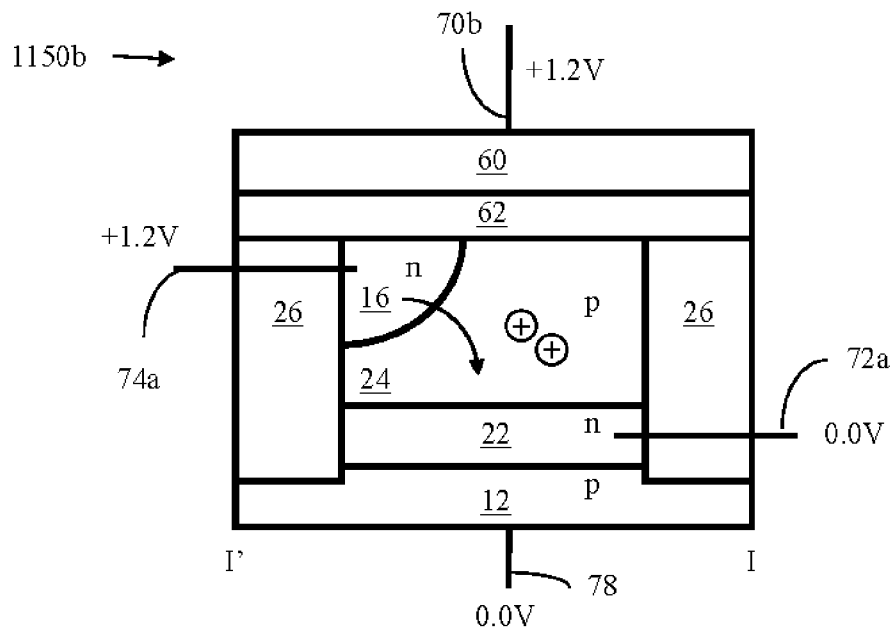


FIG. 170

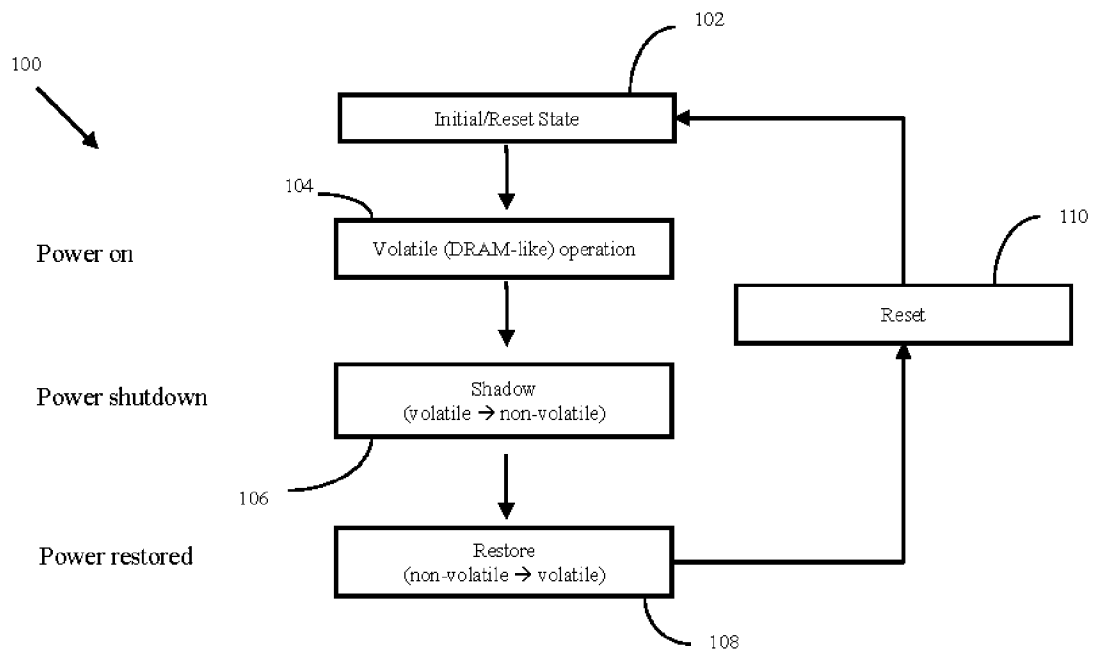


FIG. 171

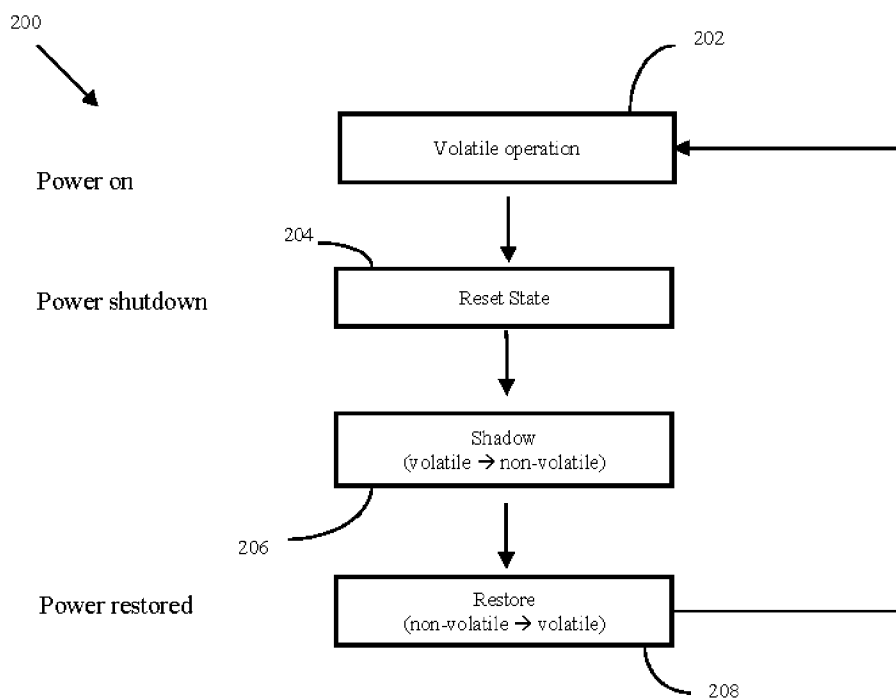


FIG. 172

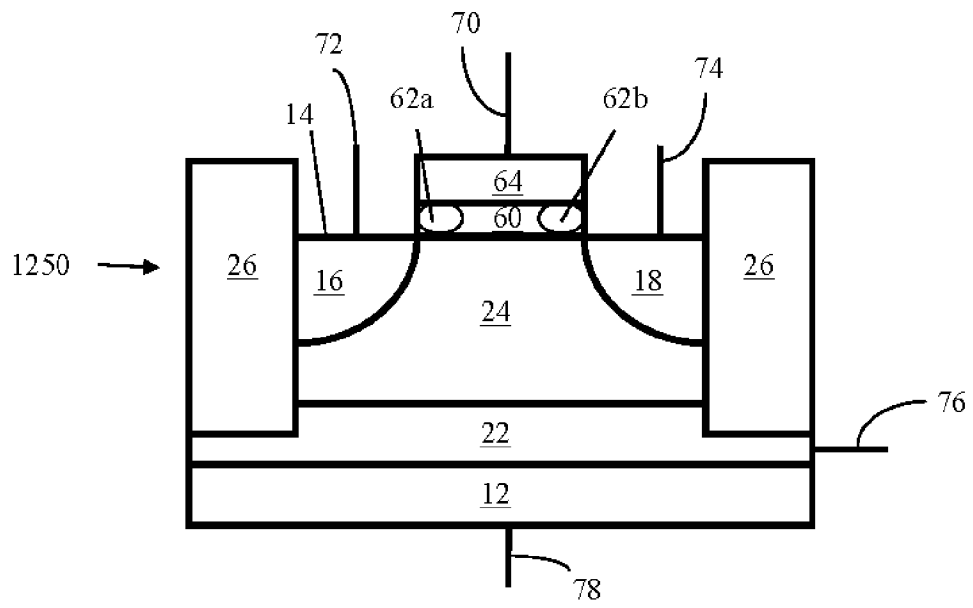


FIG. 173A

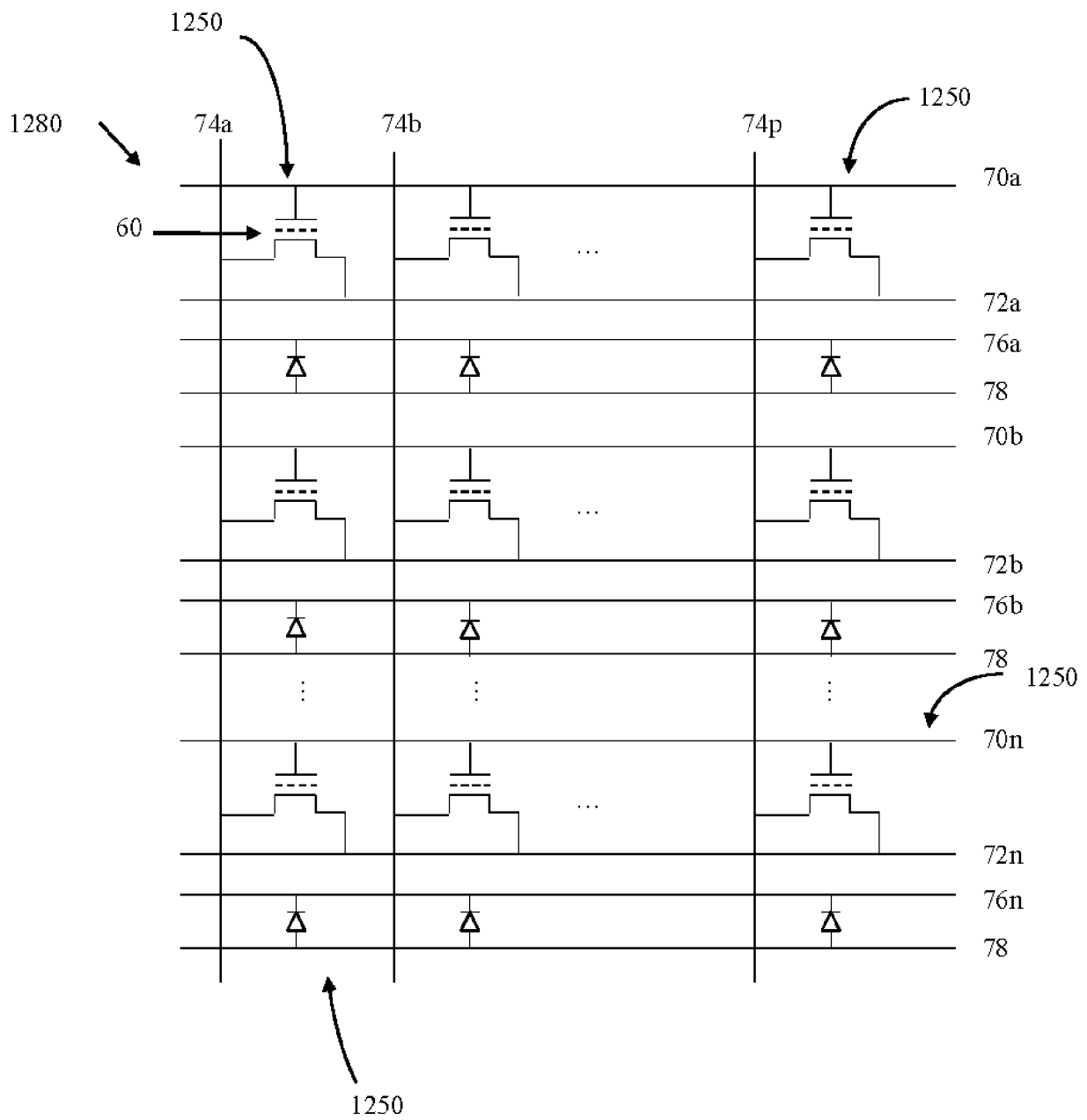


FIG. 173B

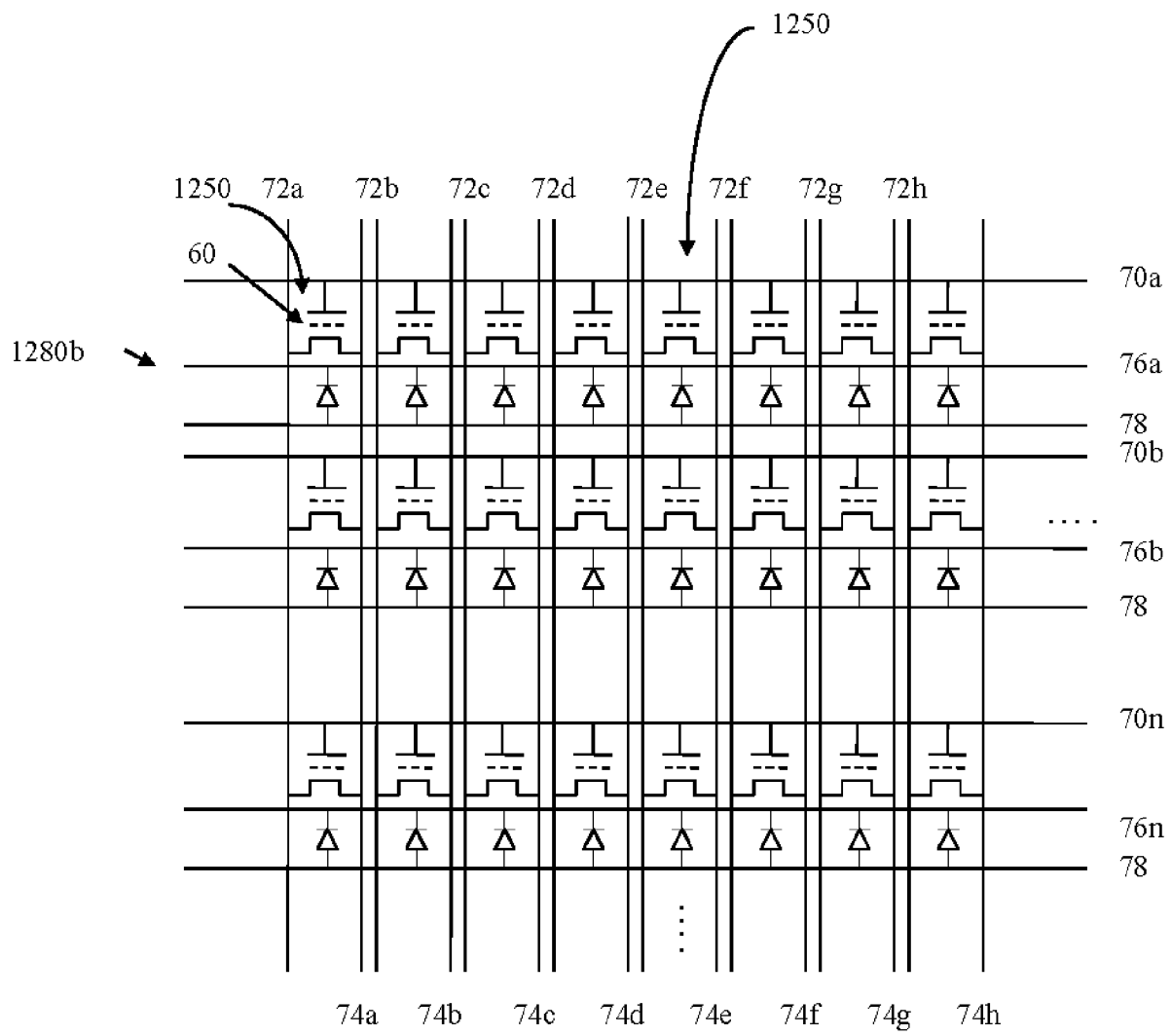


FIG. 173C

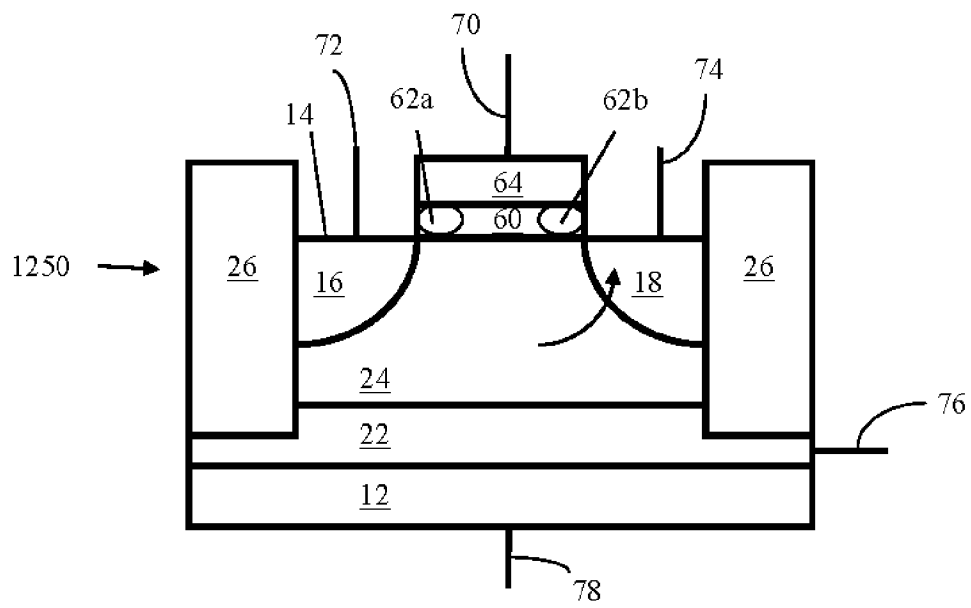


FIG. 175

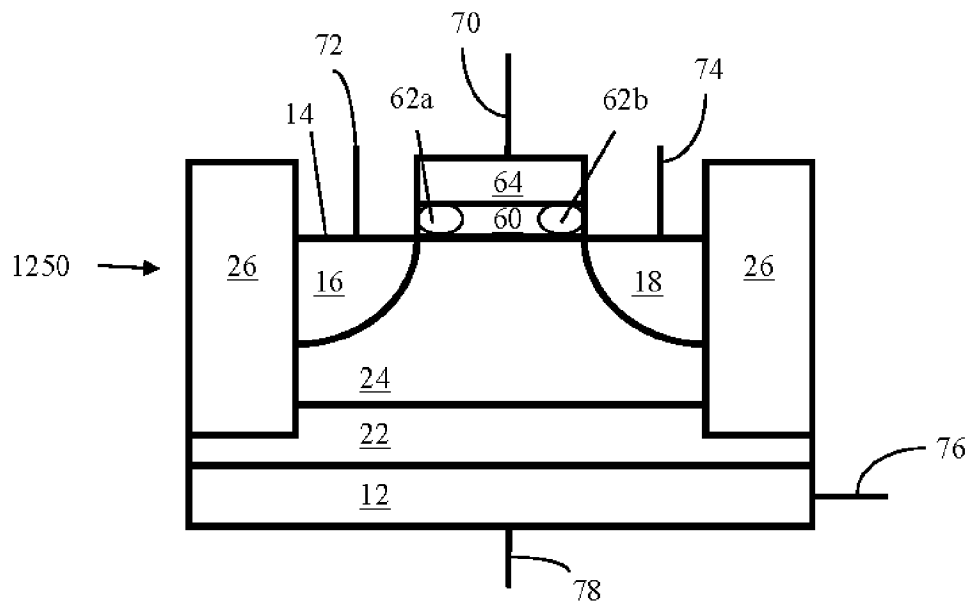


FIG. 176

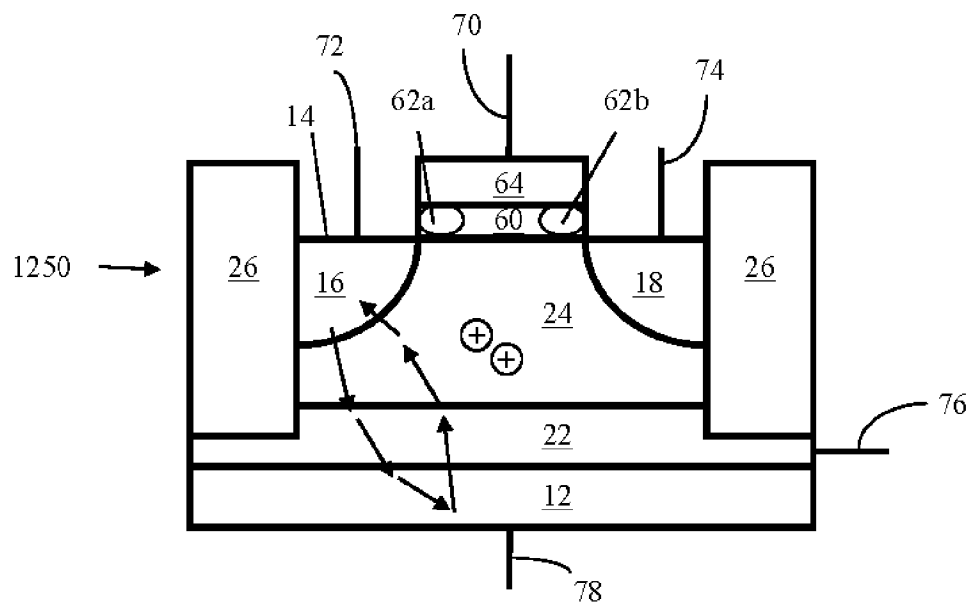


FIG. 177

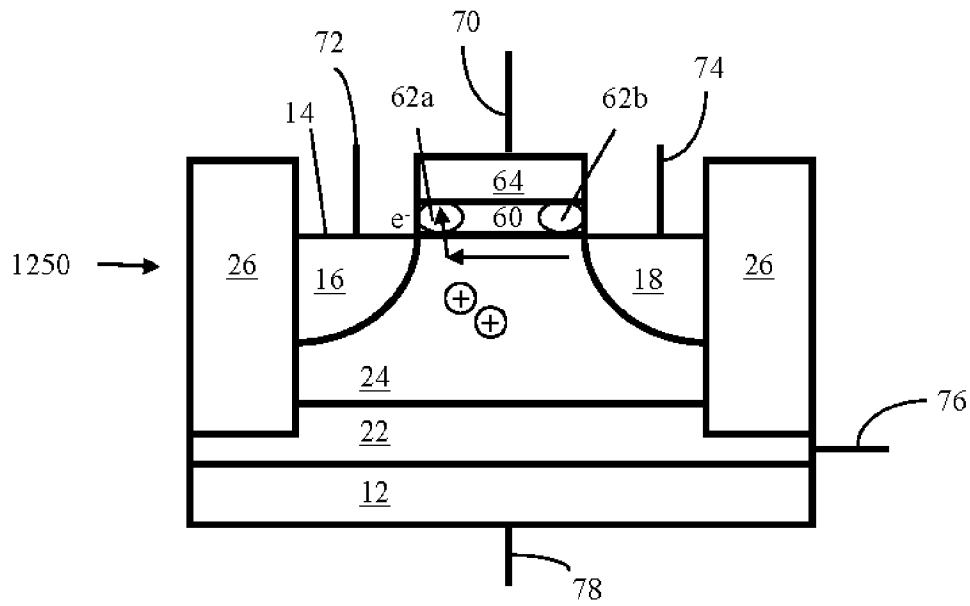


FIG. 178A

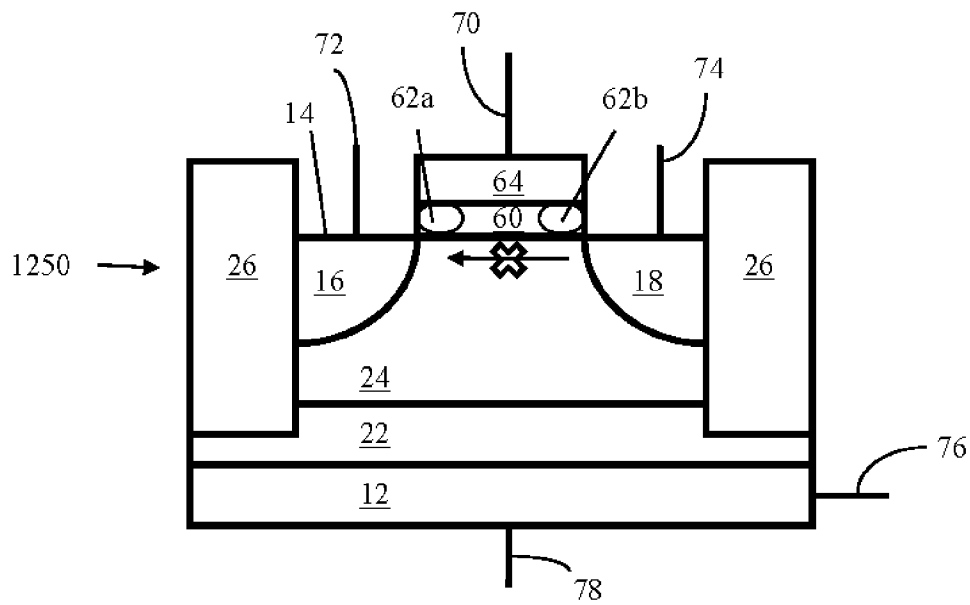


FIG. 178B

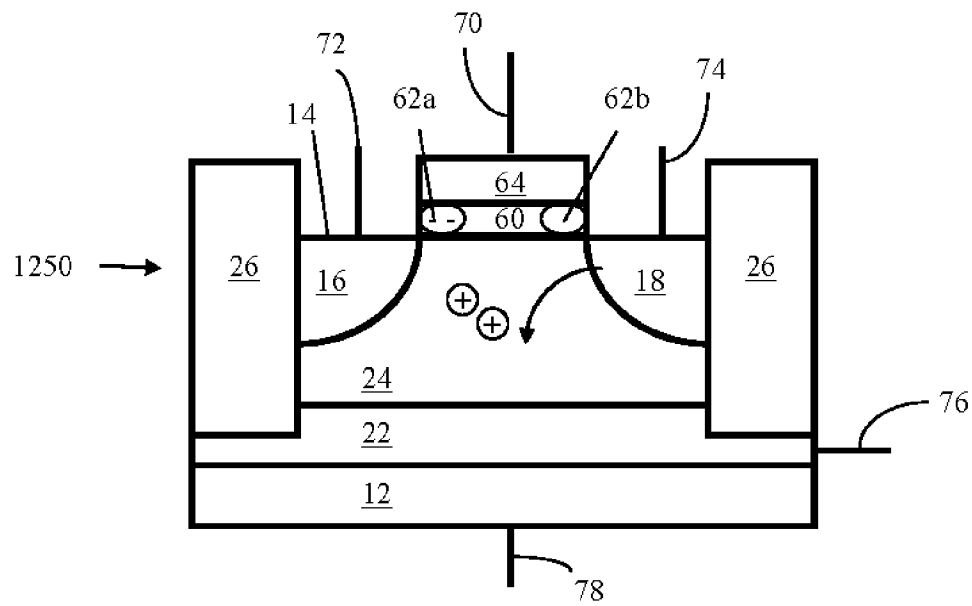


FIG. 179A

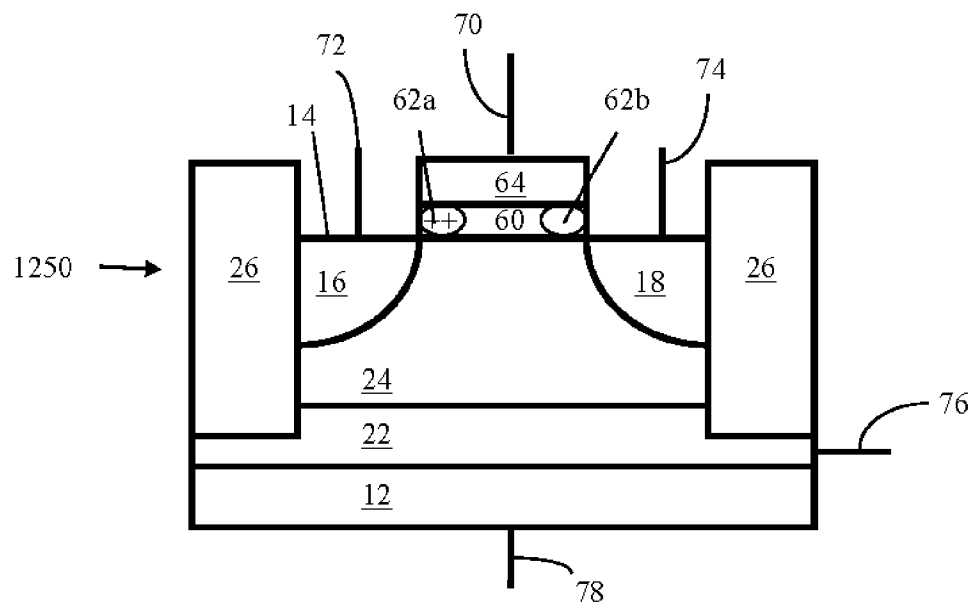


FIG. 179B

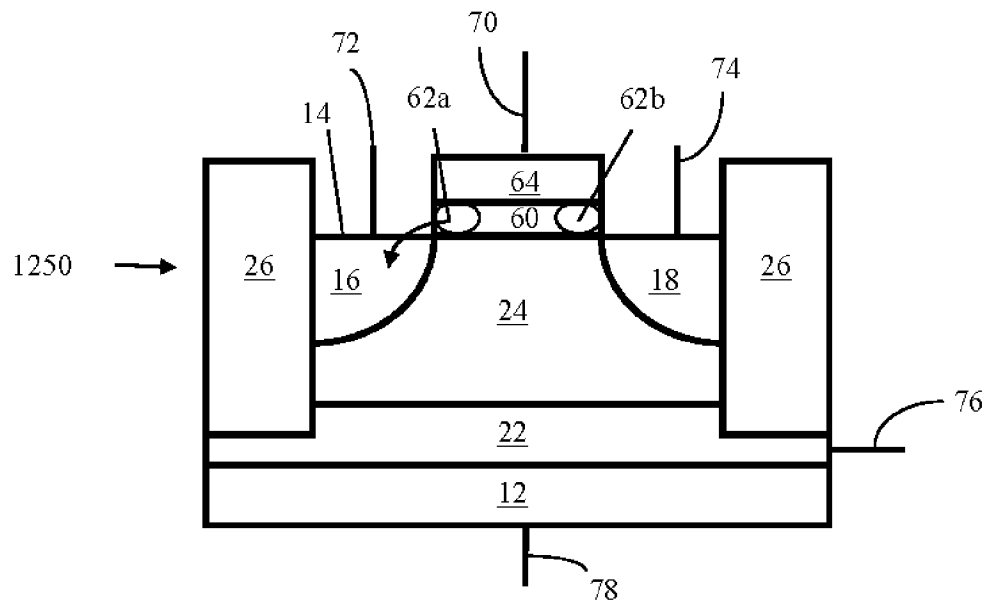


FIG. 180

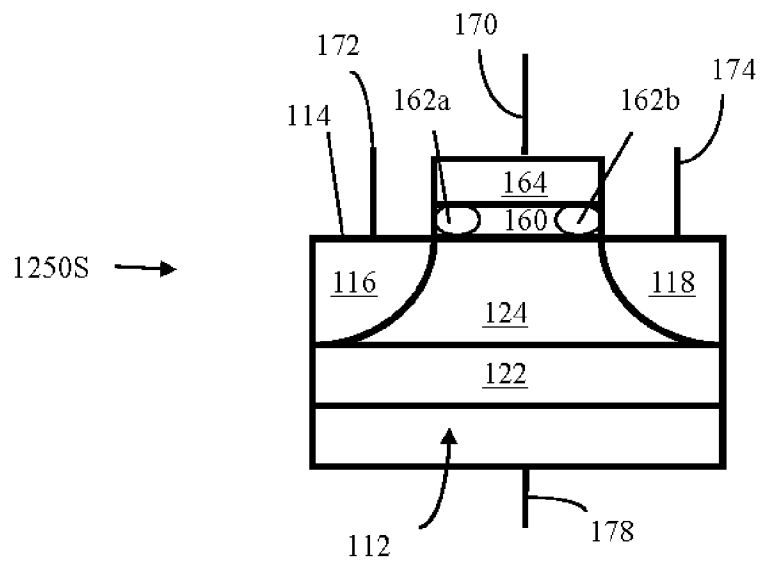


FIG. 181A

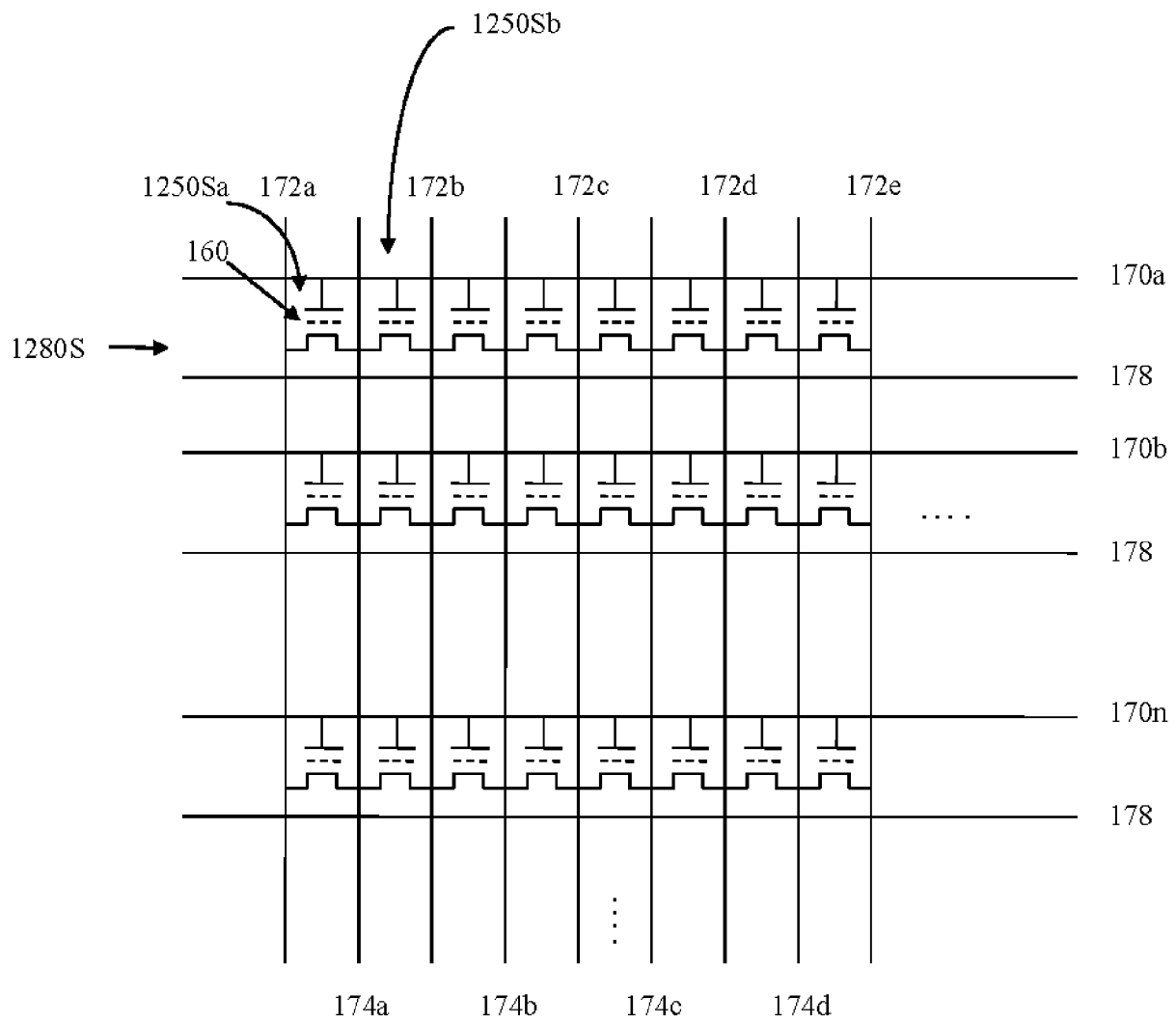


FIG. 181B

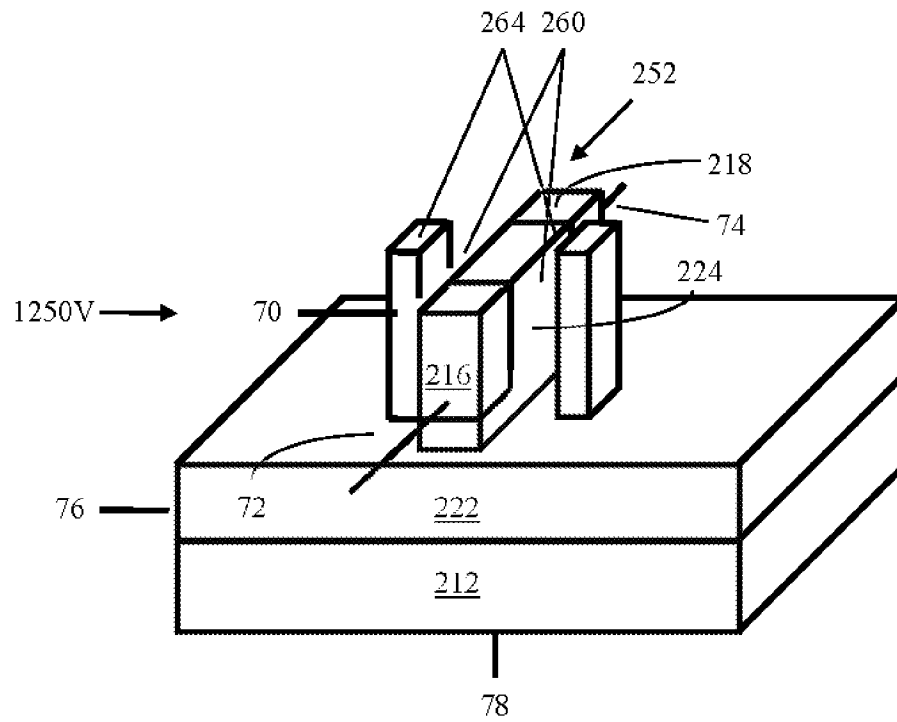


FIG. 182

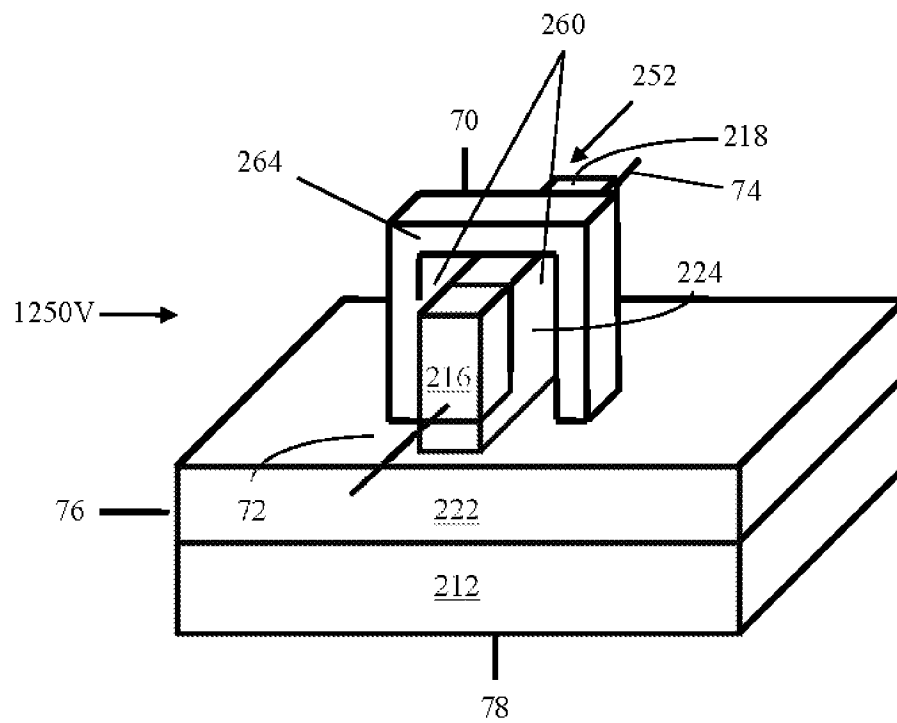


FIG. 183

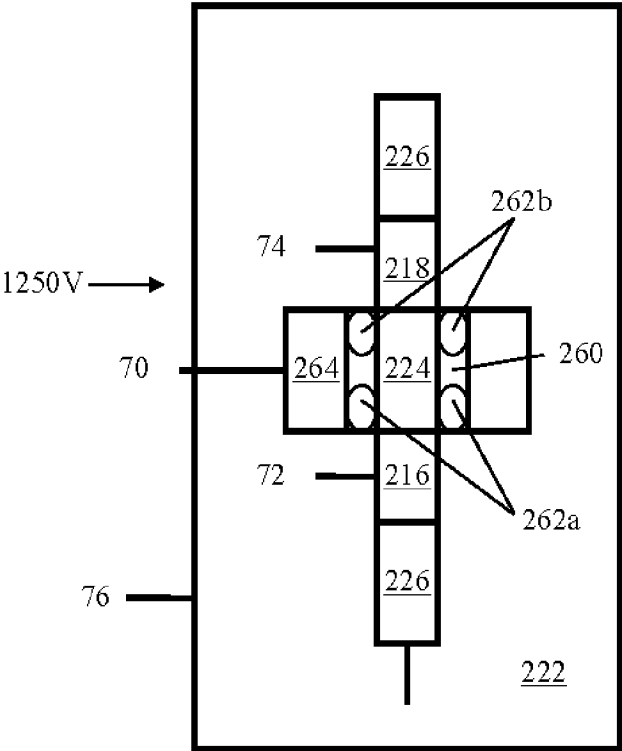
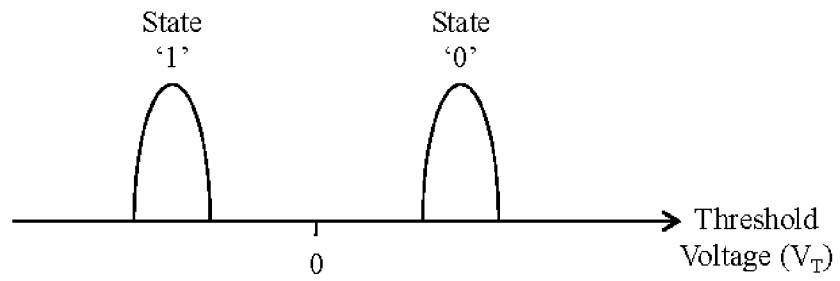
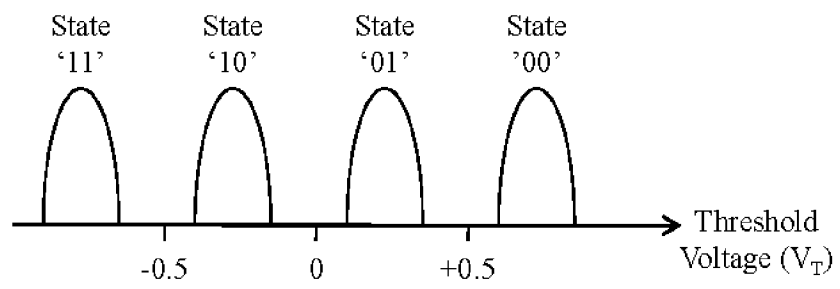


FIG. 184



Binary Cell

FIG. 185A



Multi-Level Cell

FIG. 185B

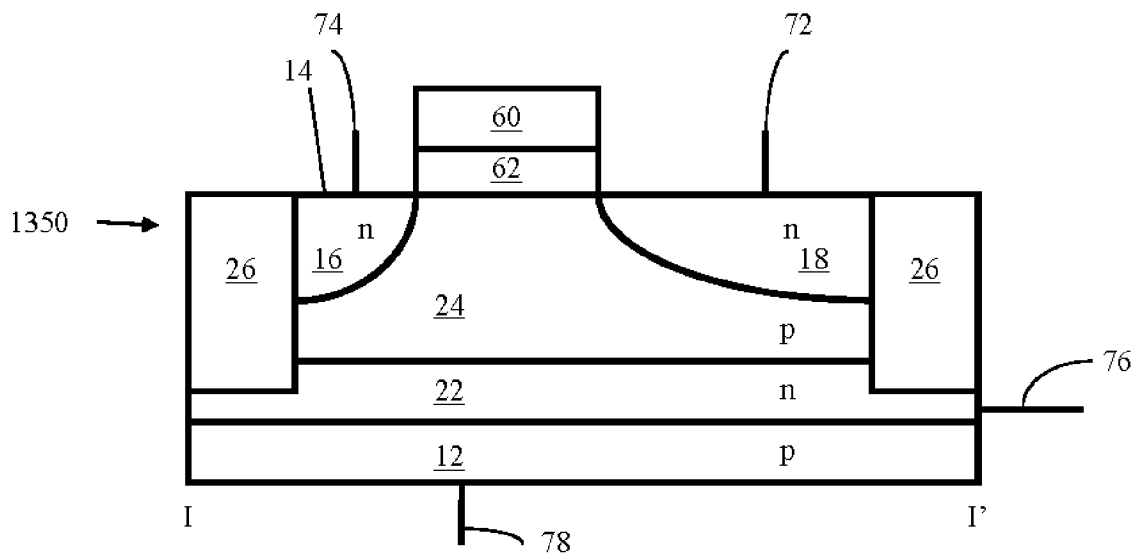


FIG. 186A

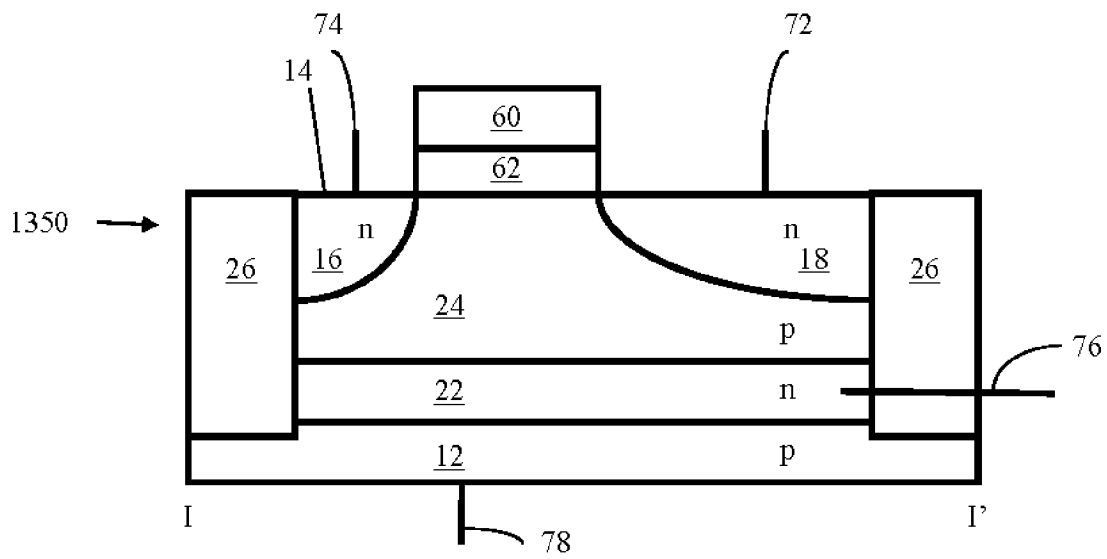


FIG. 186B

[illegible]

FIG. 186D

Exemplary Memory Array 1380 with
Representative Memory Cells 1350a, 1350b, 1350c
and 1350d

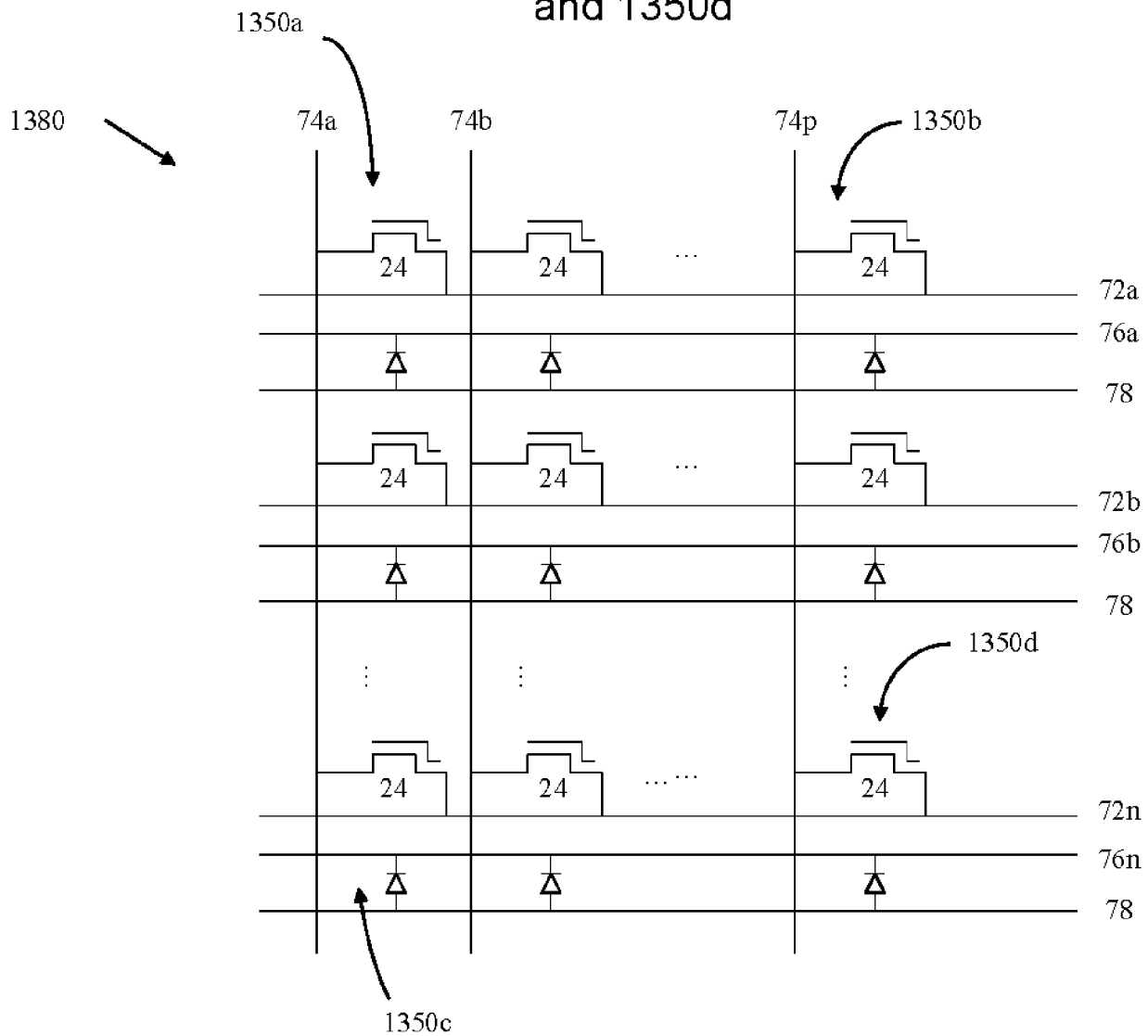


FIG. 186E

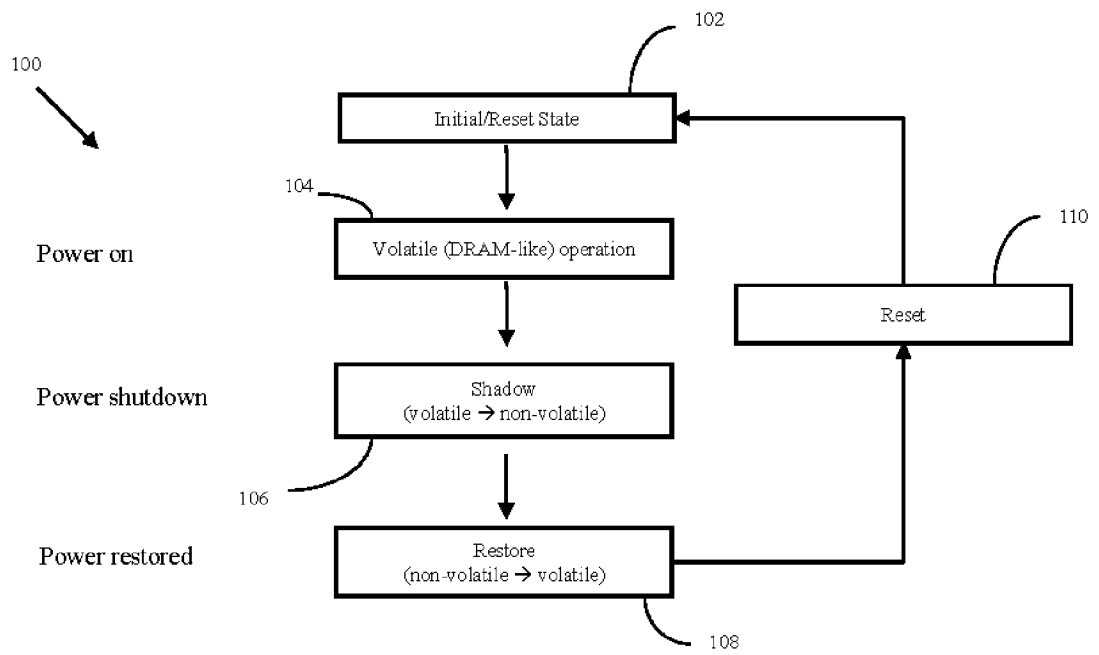


FIG. 187

Array Hold Operation
(All Memory Cells 1350)

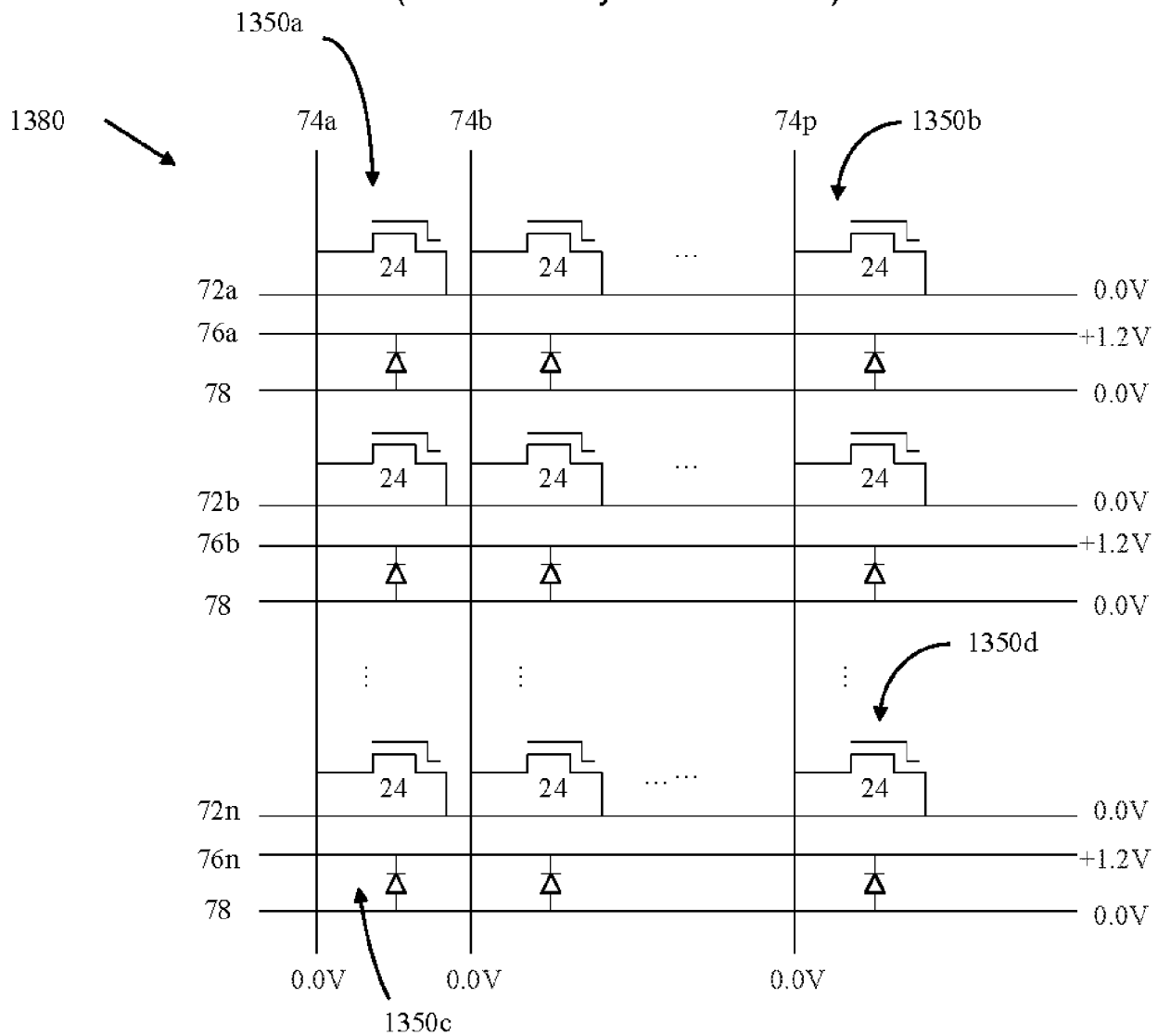


FIG. 188

Floating Body 24 is positively charged and $V(\text{BL } 16) = 0.0\text{V}$

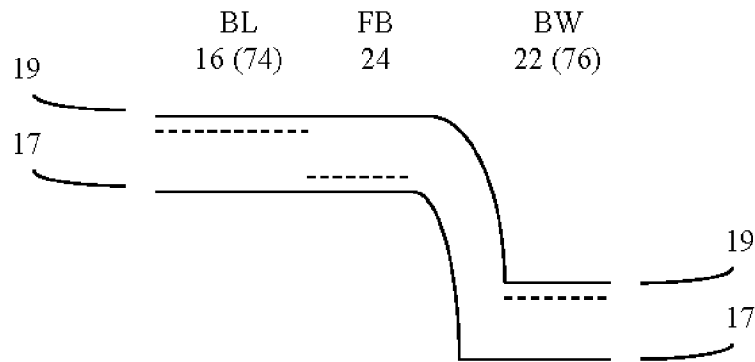


FIG. 189A

FB is neutrally charged; and $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

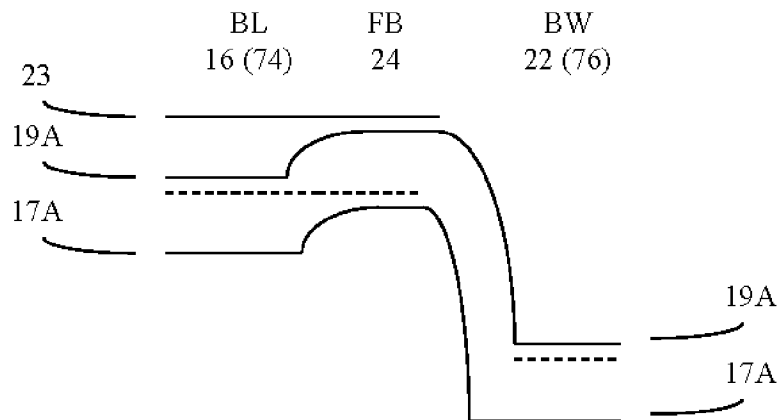


FIG. 189B

Read Operation, Active Bit Line High
(Memory Cell 1350a)

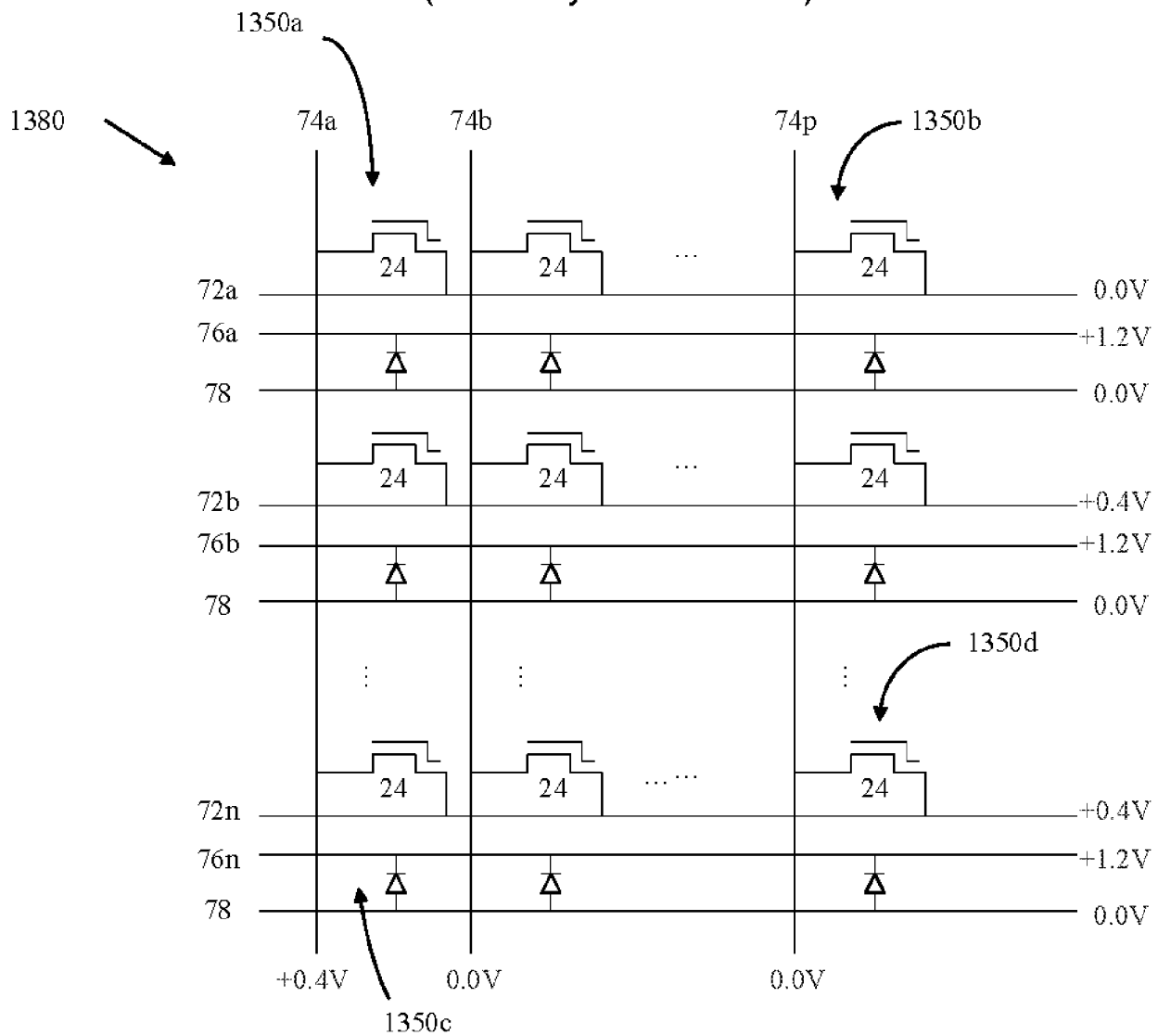


FIG. 190A

Read Operation, Active Source Line High
(Memory Cell 1350a)

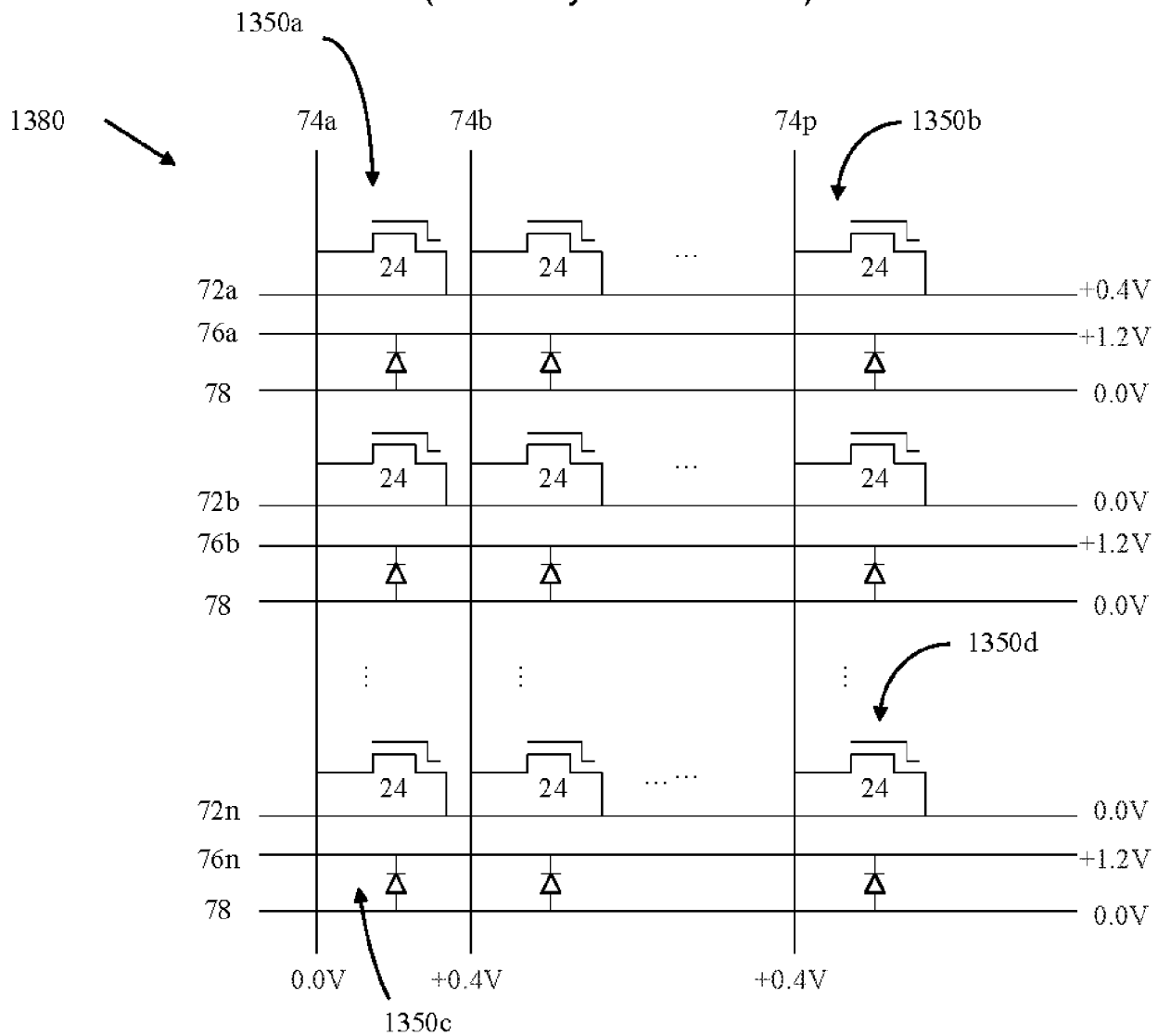


FIG. 190B

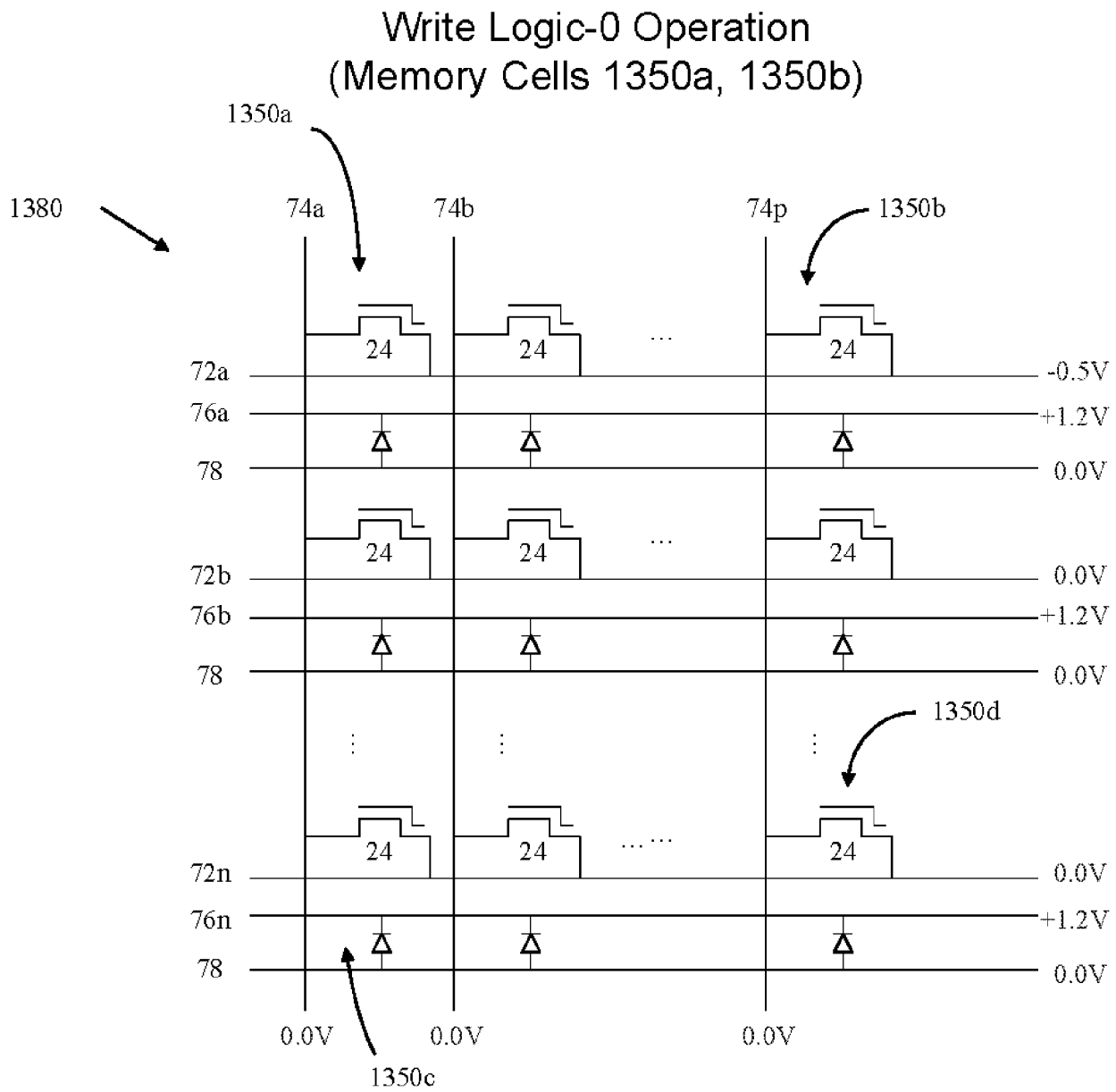


FIG. 191A

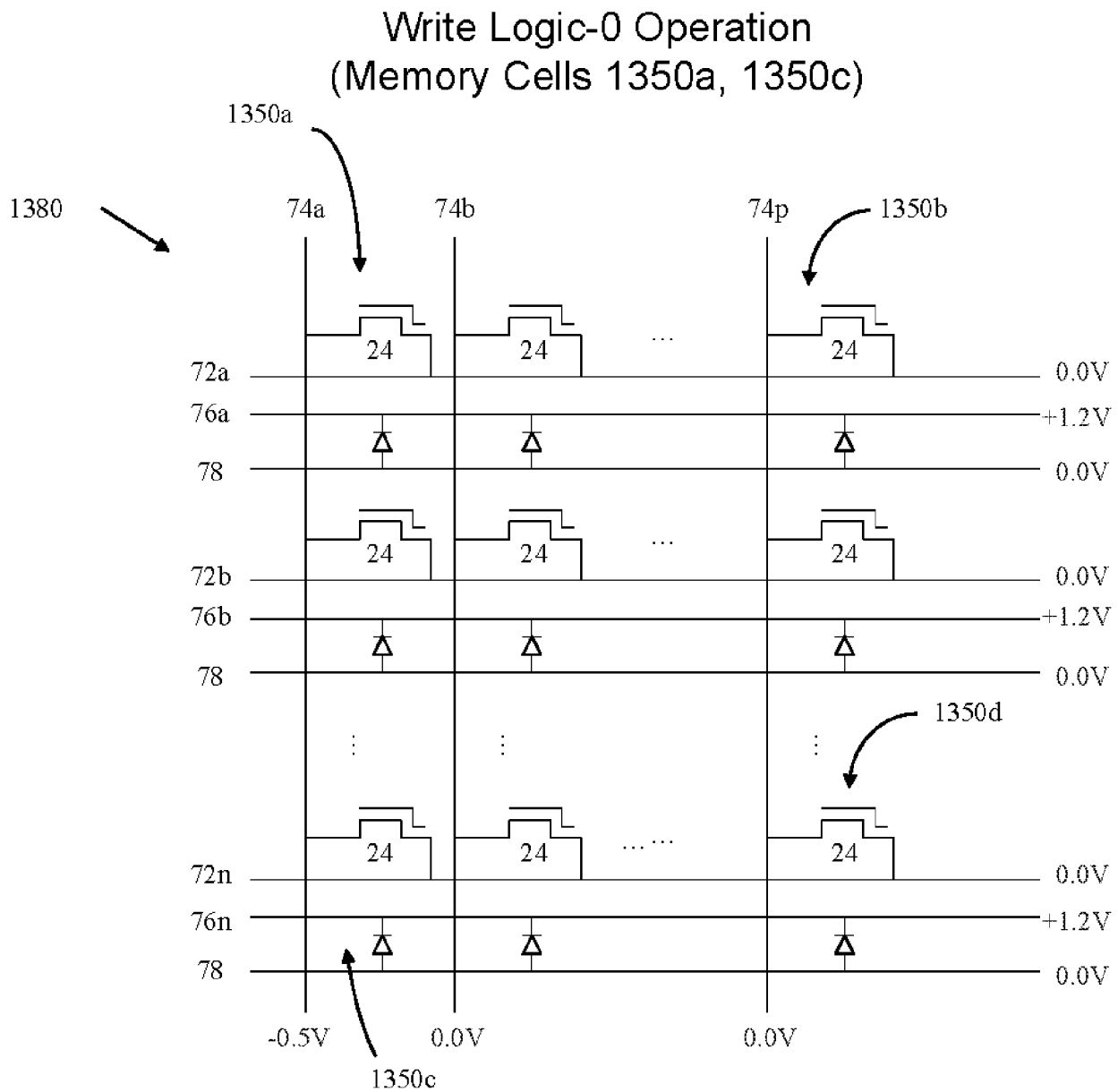


FIG. 191B

Write Logic-1 Operation, Active Bit Line High (Memory Cell 1350a)

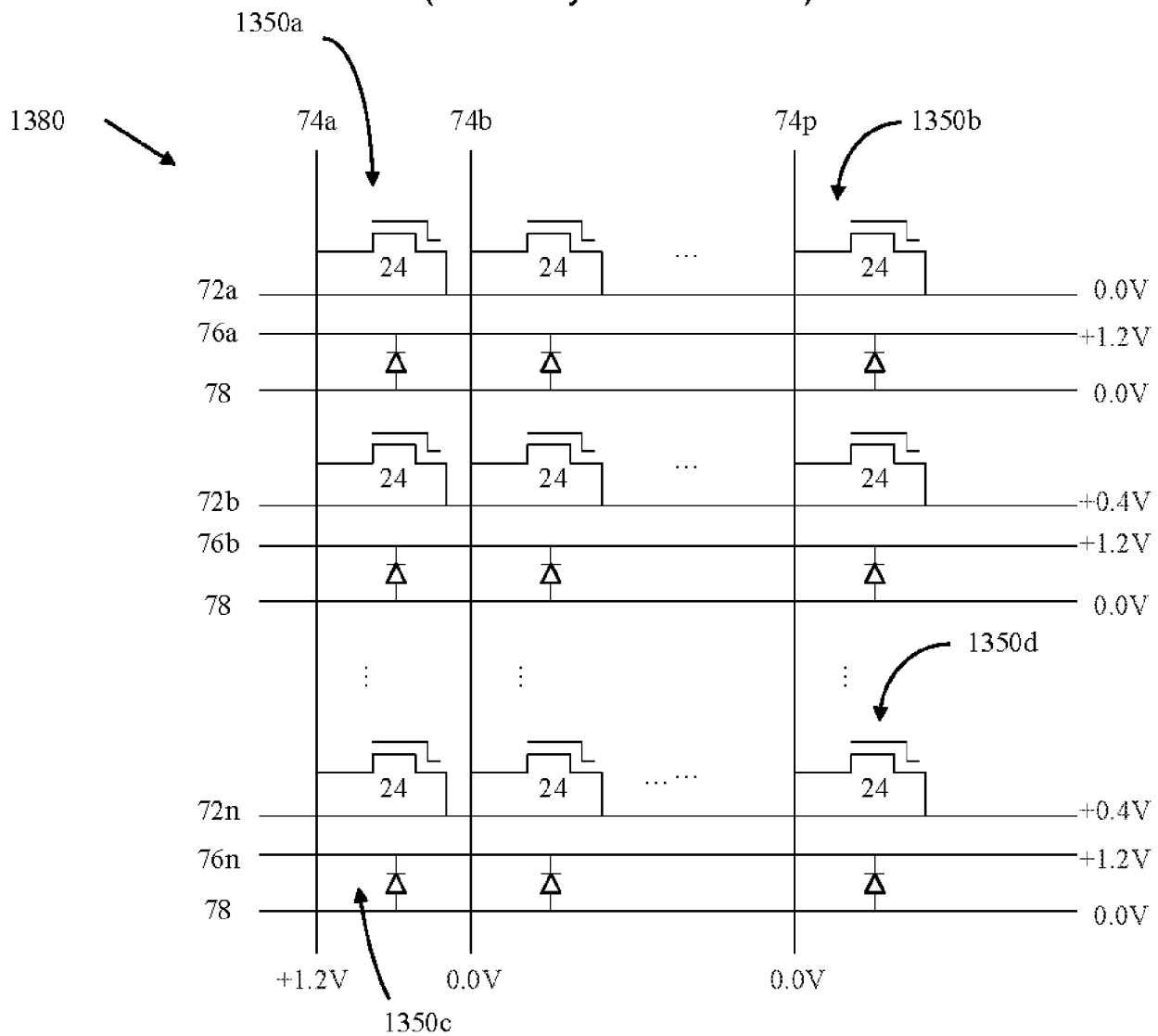


FIG. 192A

Write Logic-1 Operation, Active Source Line High
(Memory Cell 1350a)

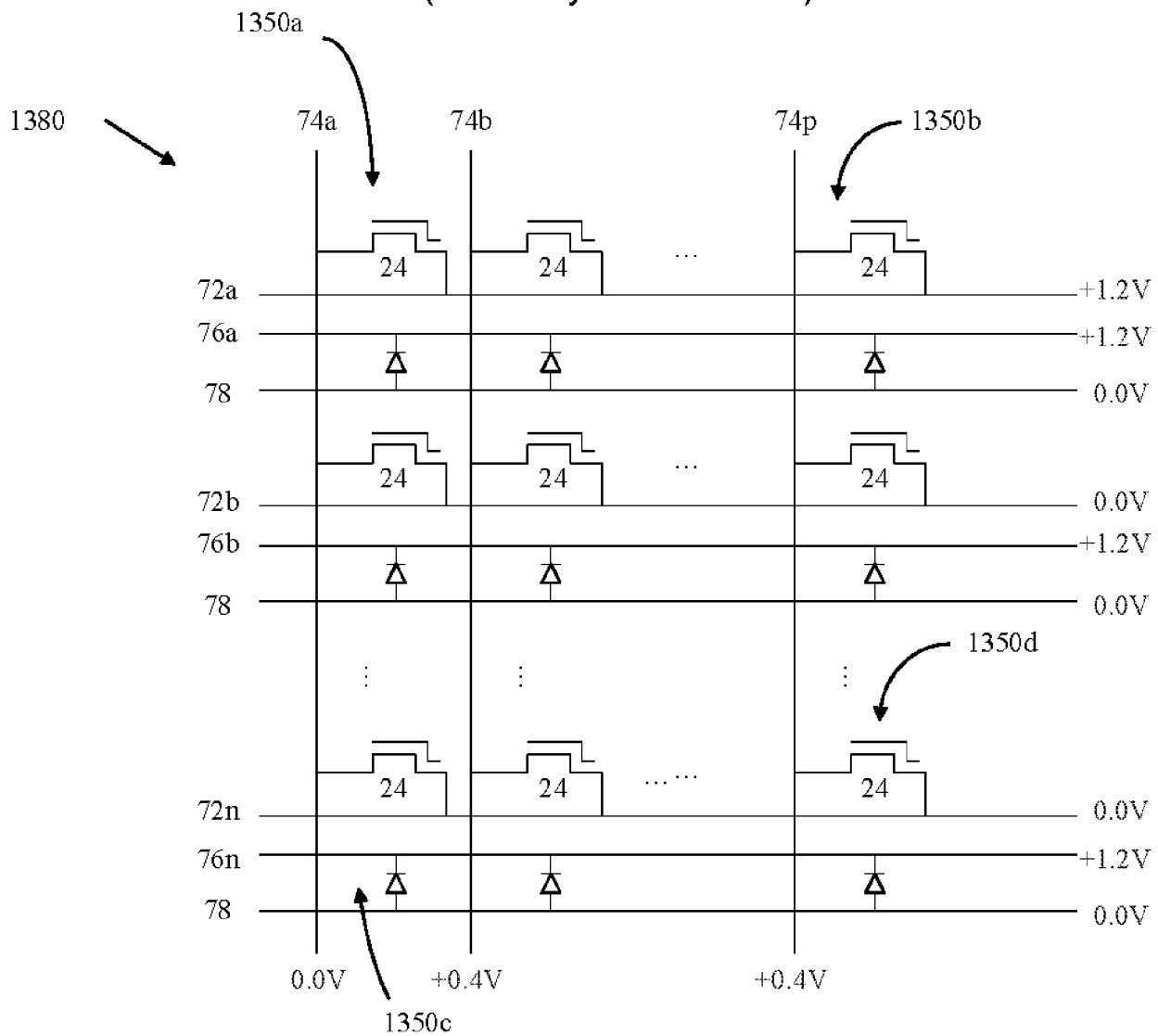


FIG. 192B

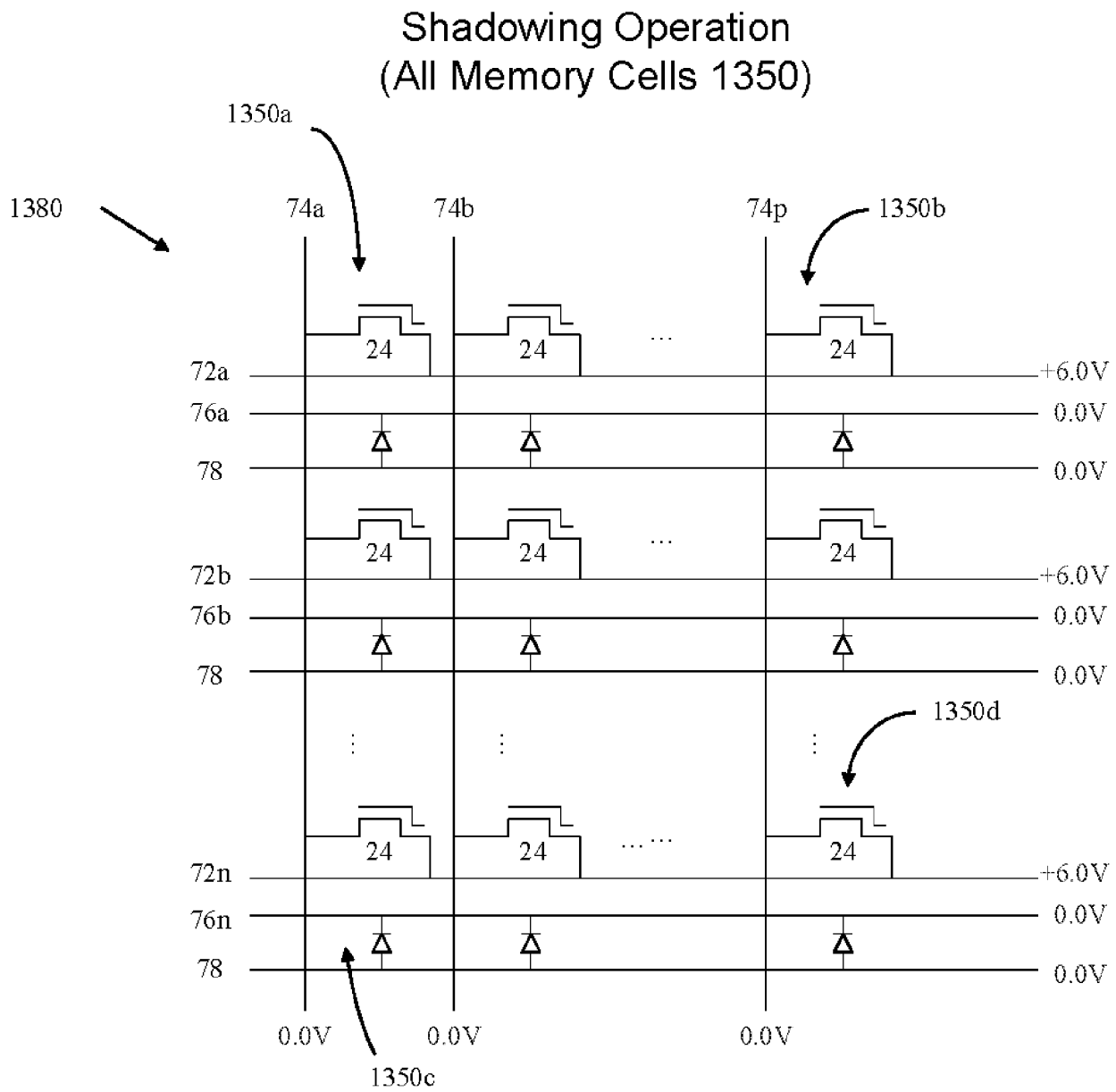


FIG. 193A

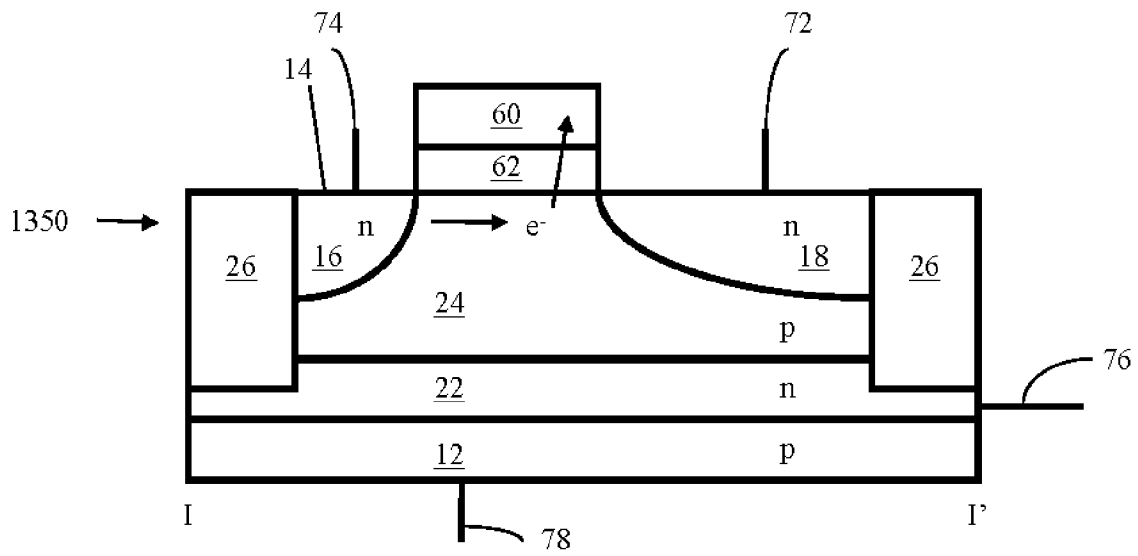


FIG. 193B

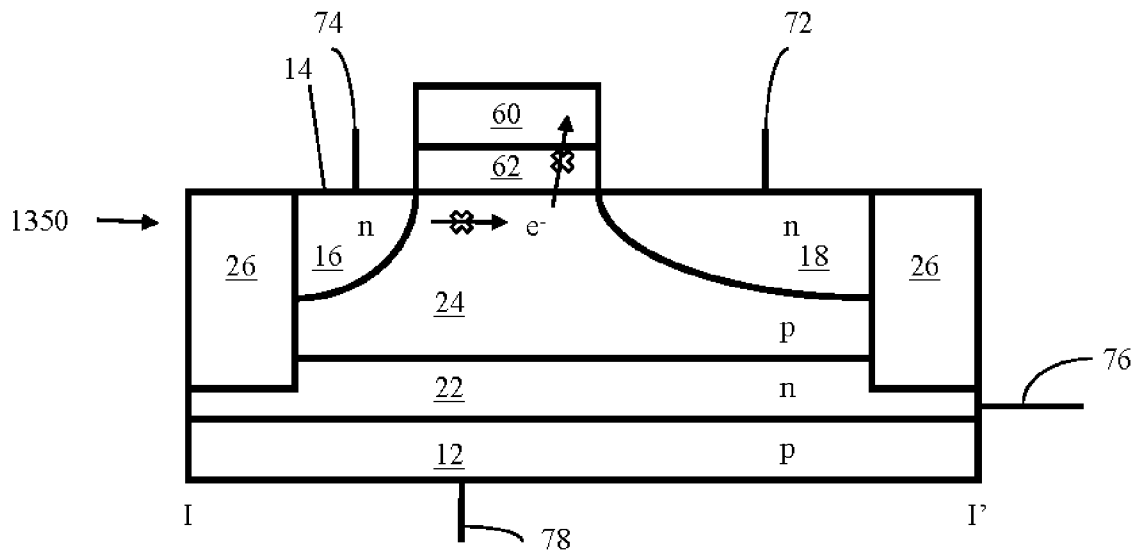


FIG. 193C

Restore Operation (All Memory Cells 1350)

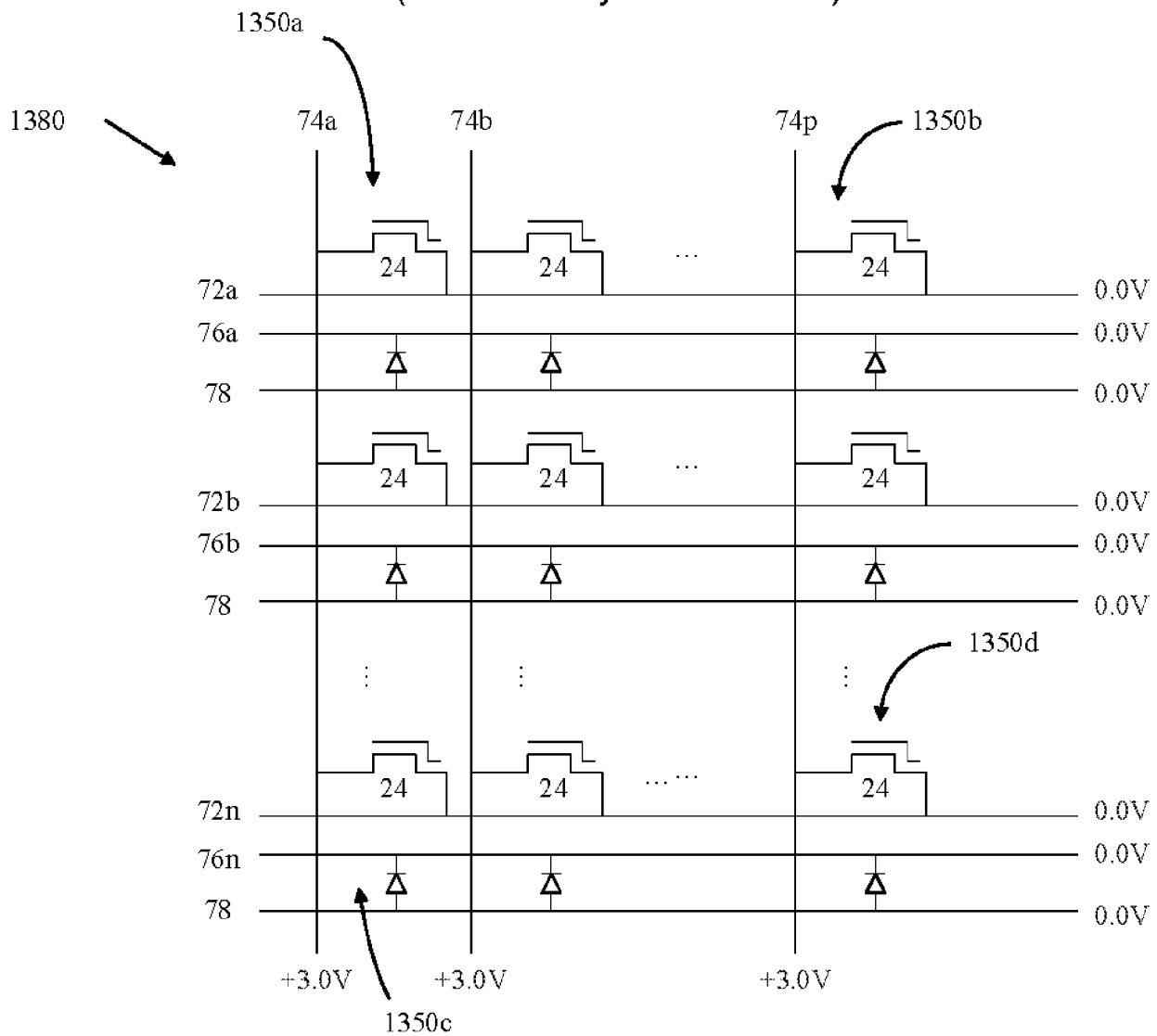


FIG. 194A

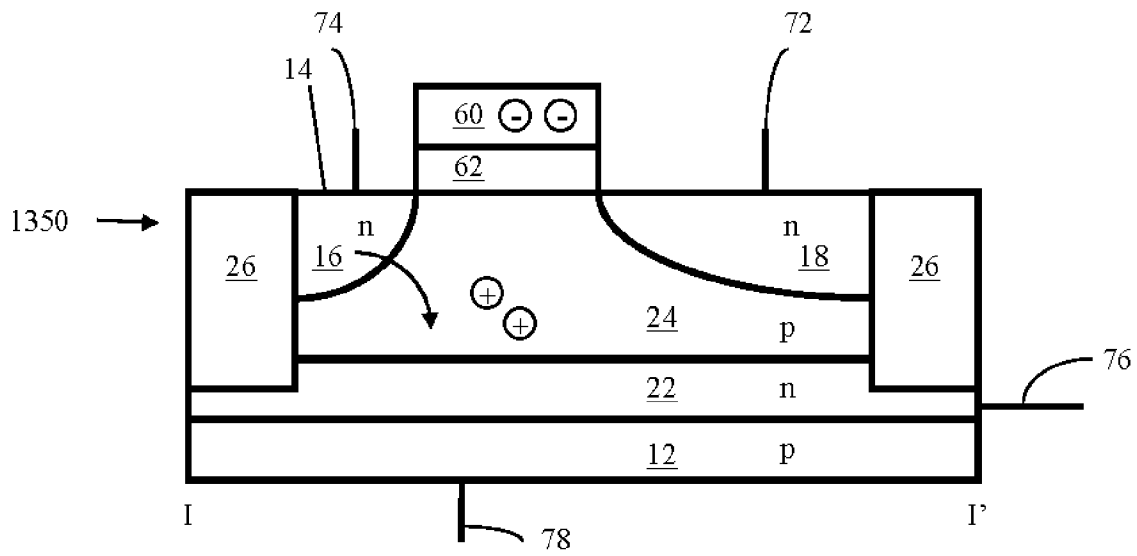


FIG. 194B

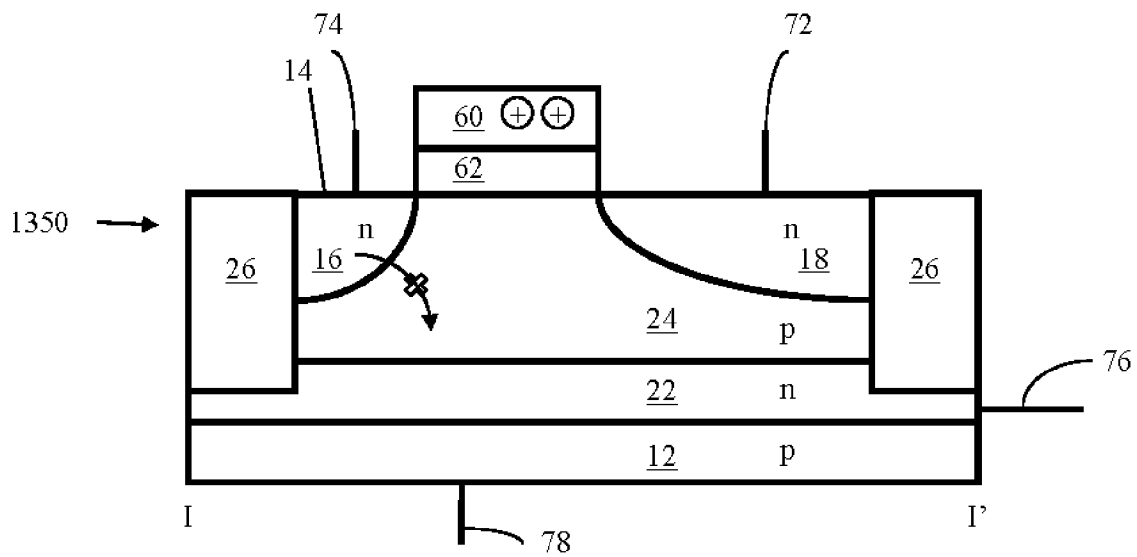


FIG. 194C

Reset Operation (All Memory Cells 1350)

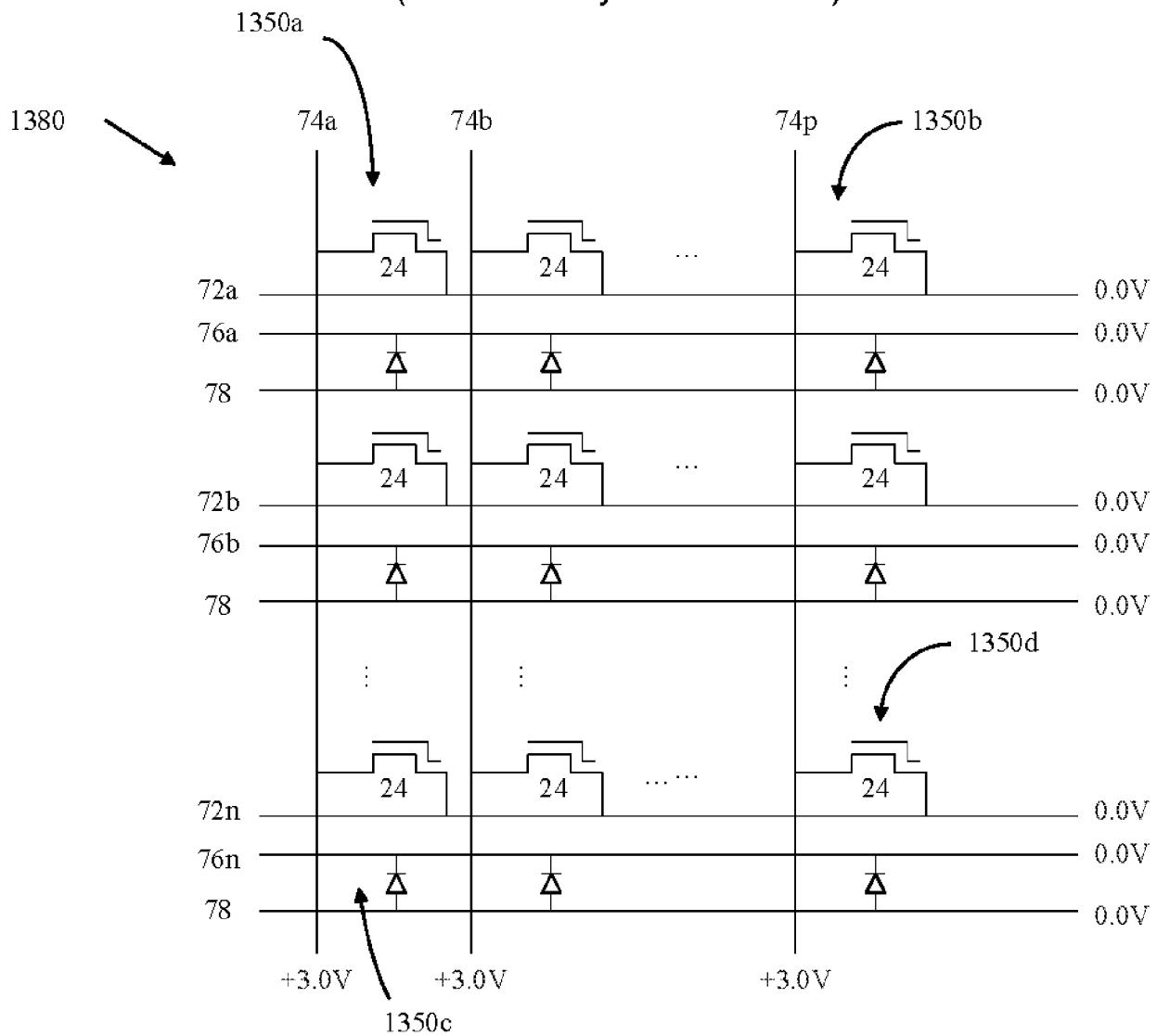


FIG. 195

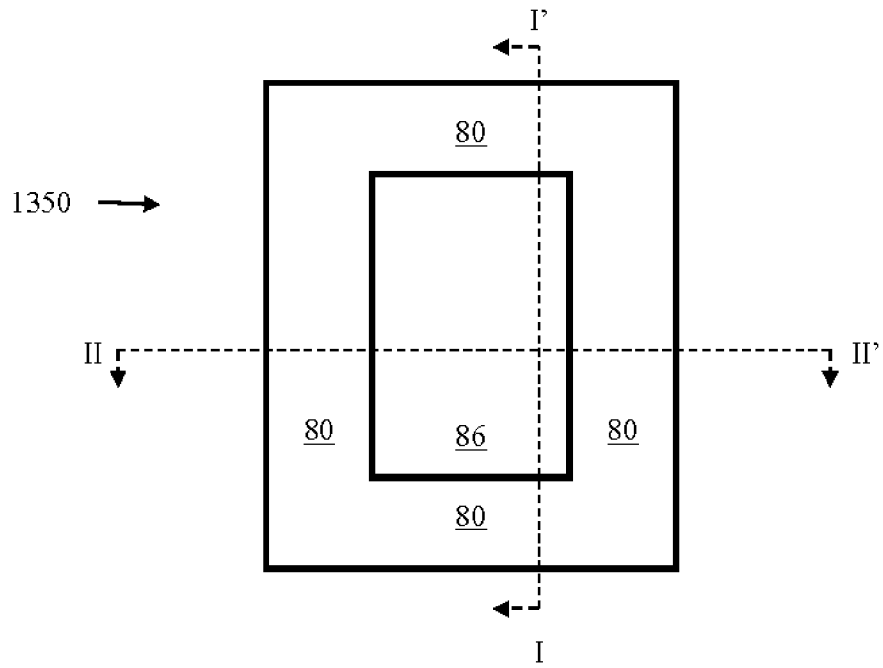


FIG. 196A

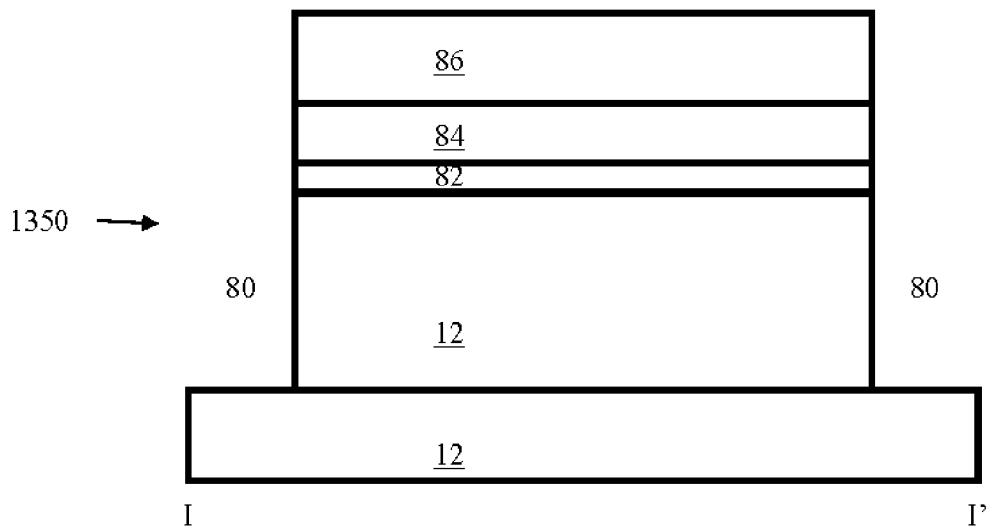


FIG. 196B

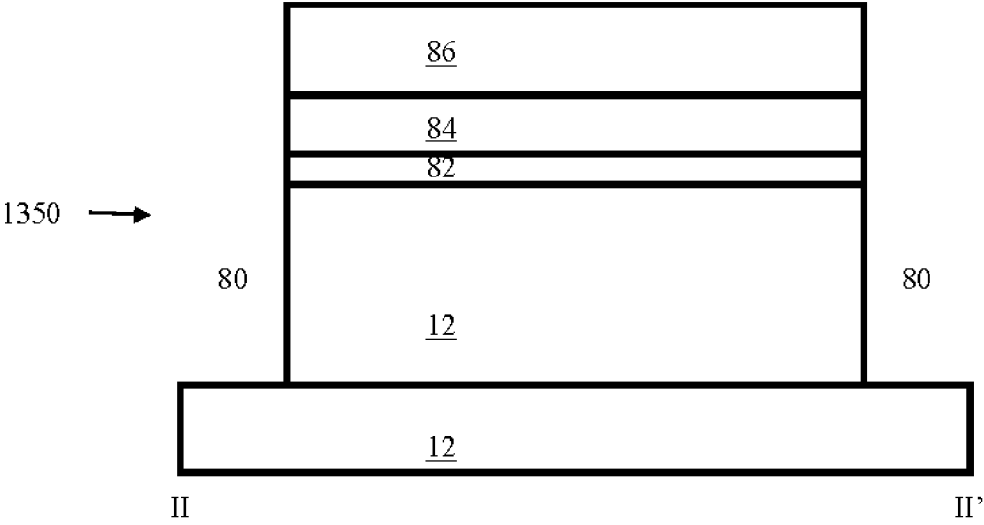


FIG. 196C

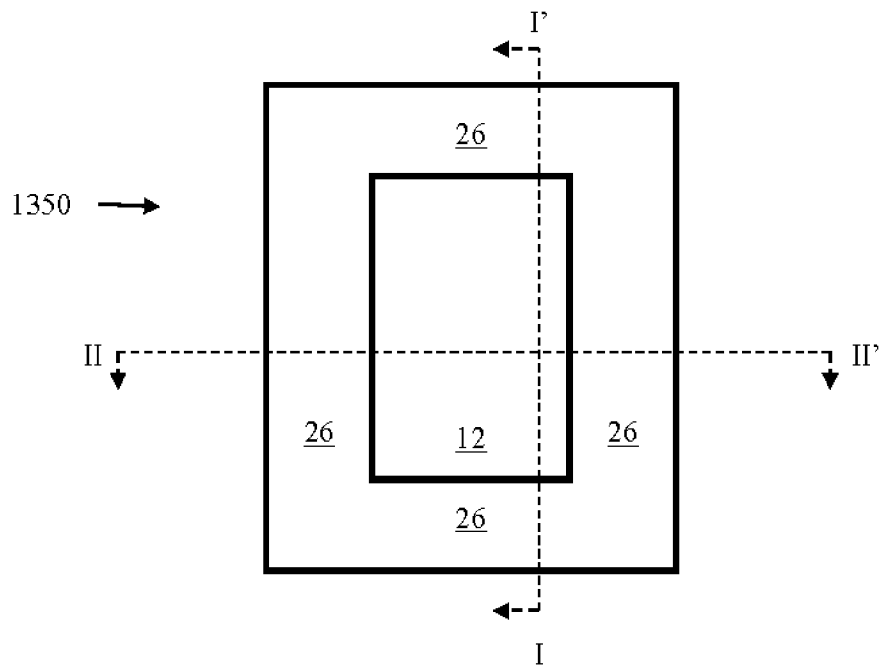


FIG. 196D

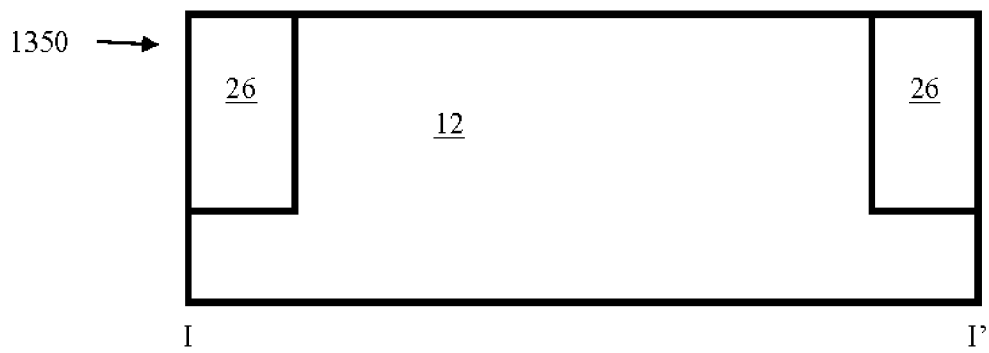


FIG. 196E

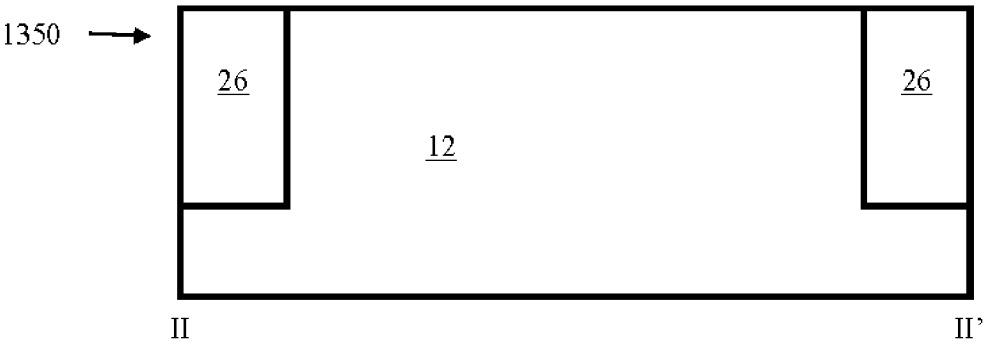


FIG. 196F

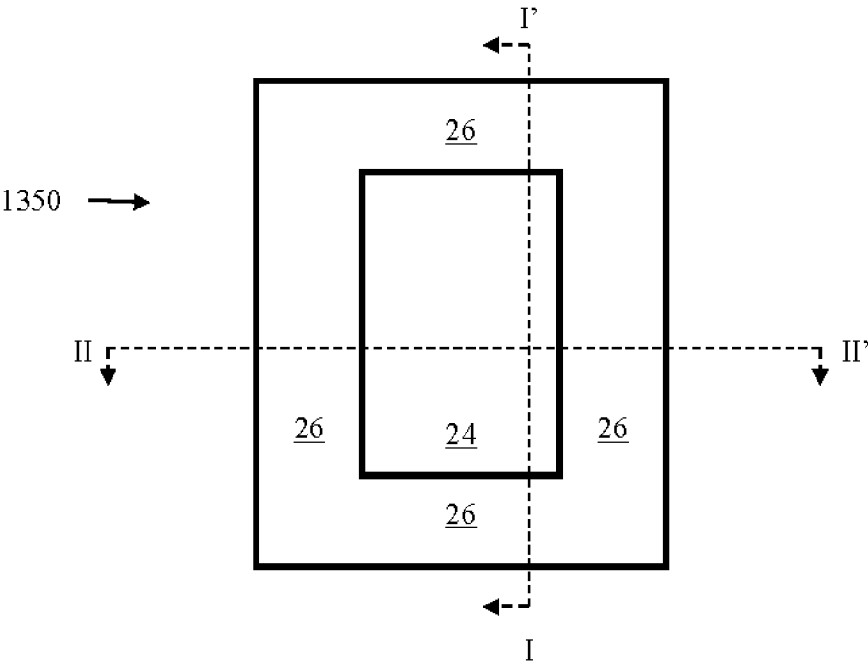


FIG. 196G

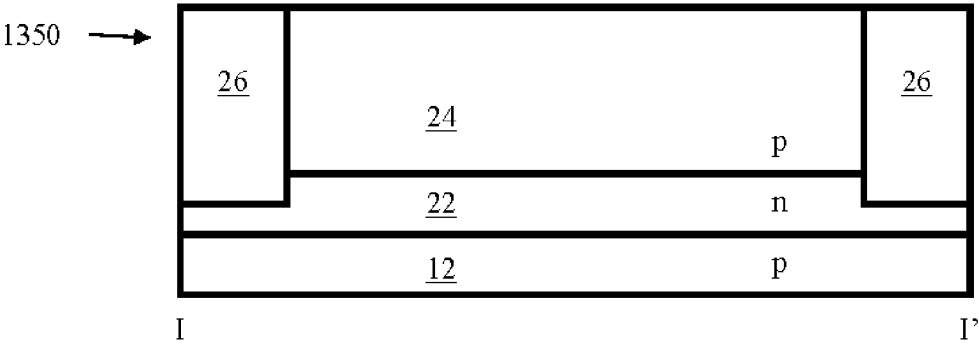


FIG. 196H

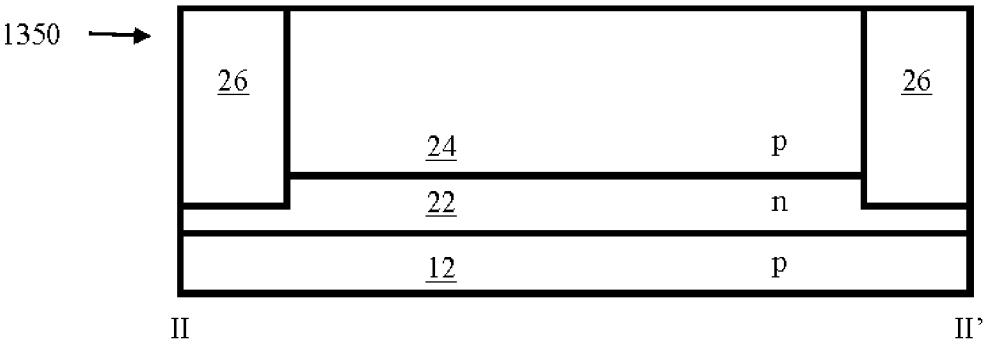


FIG. 196I

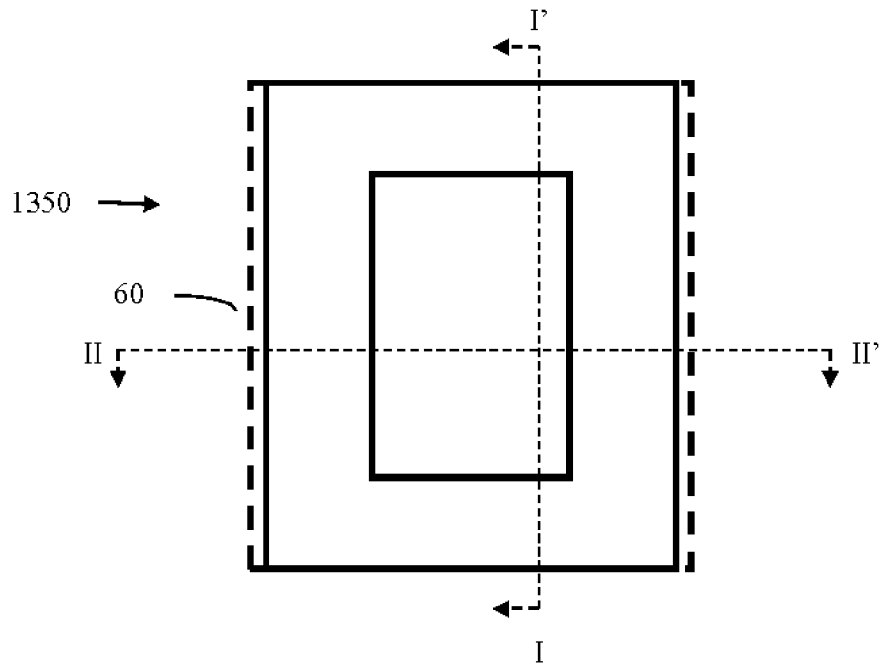


FIG. 196J

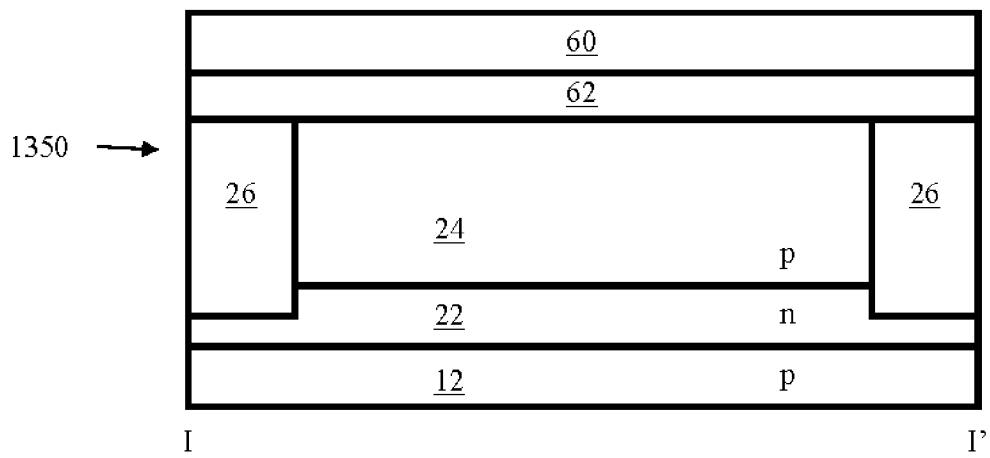


FIG. 196K

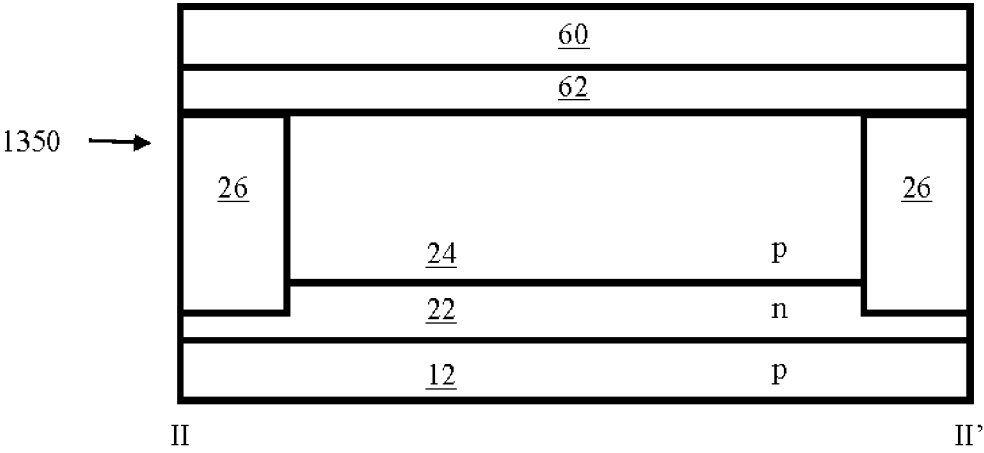


FIG. 196L

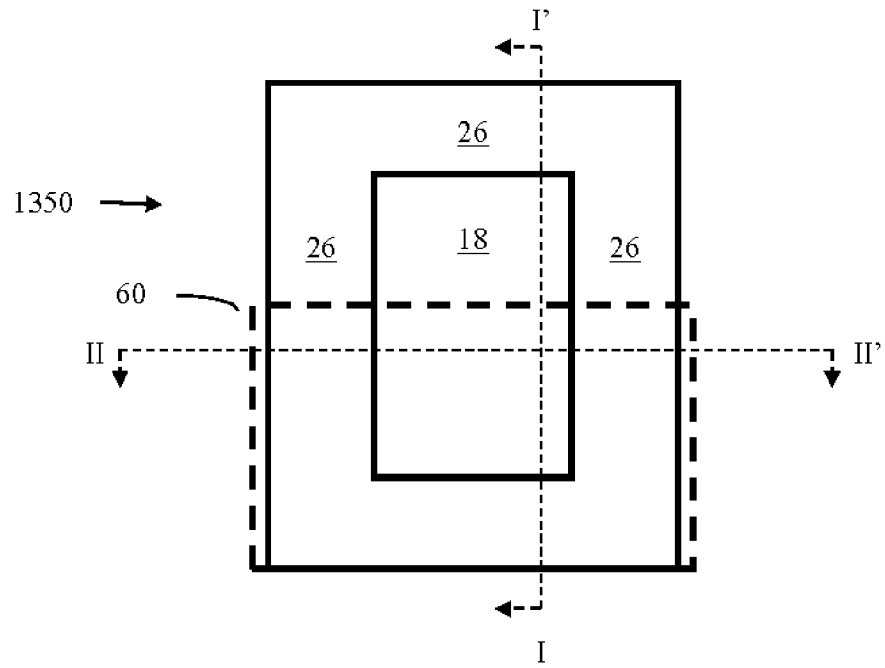


FIG. 196M

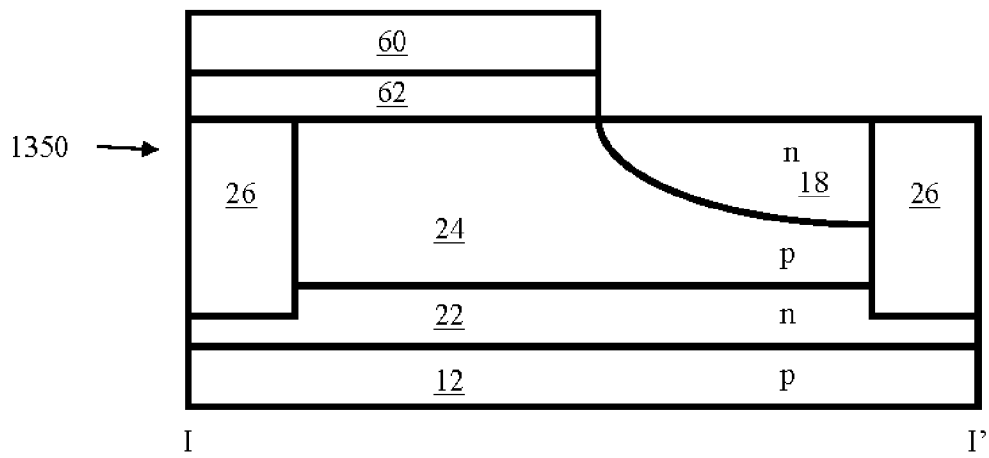


FIG. 196N

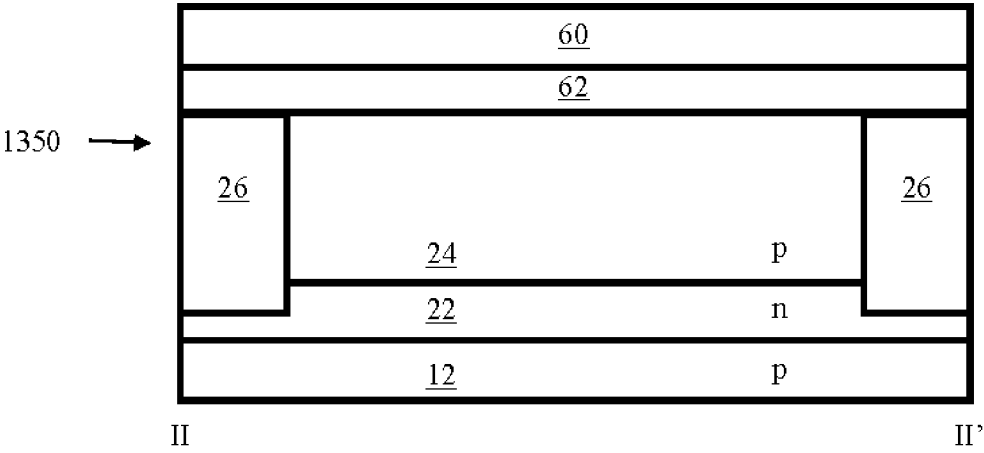


FIG. 196O

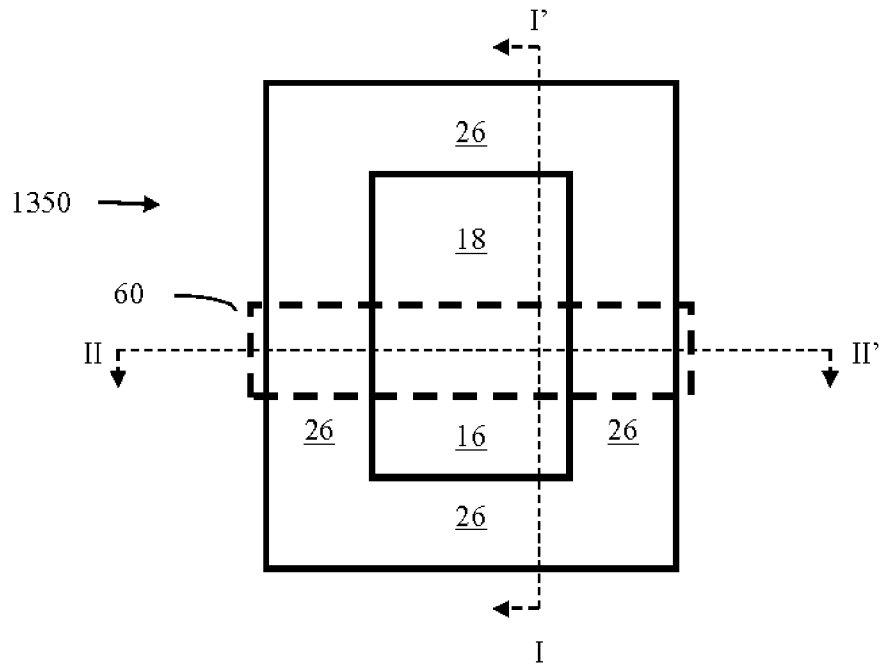


FIG. 196P

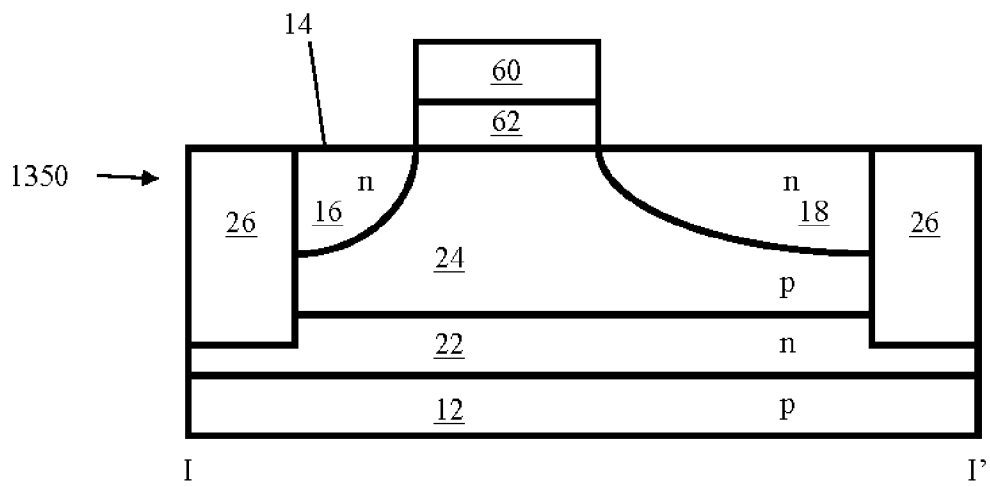


FIG. 196Q

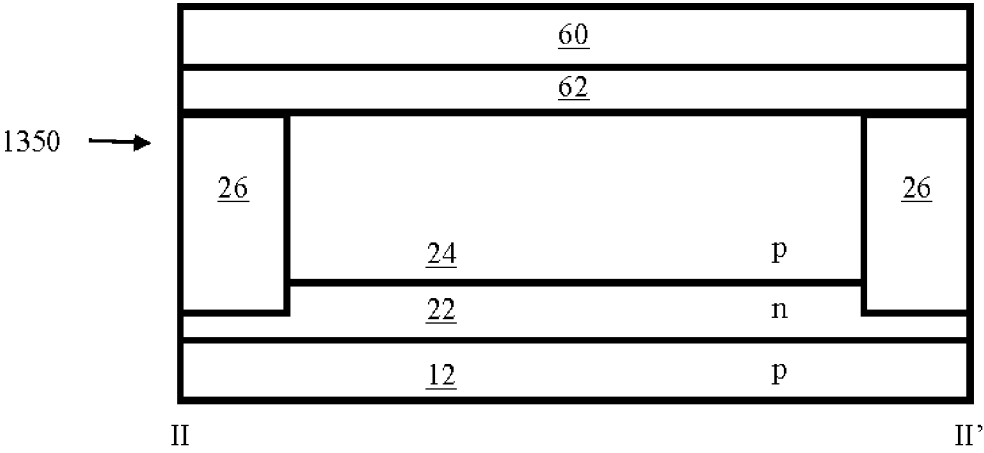


FIG. 196R

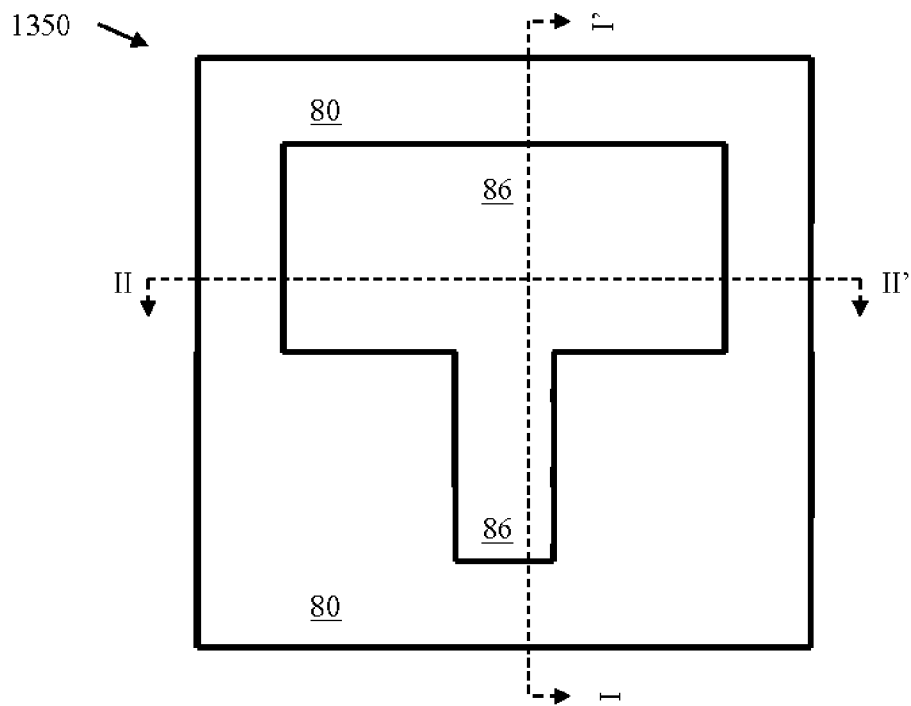


FIG. 197A

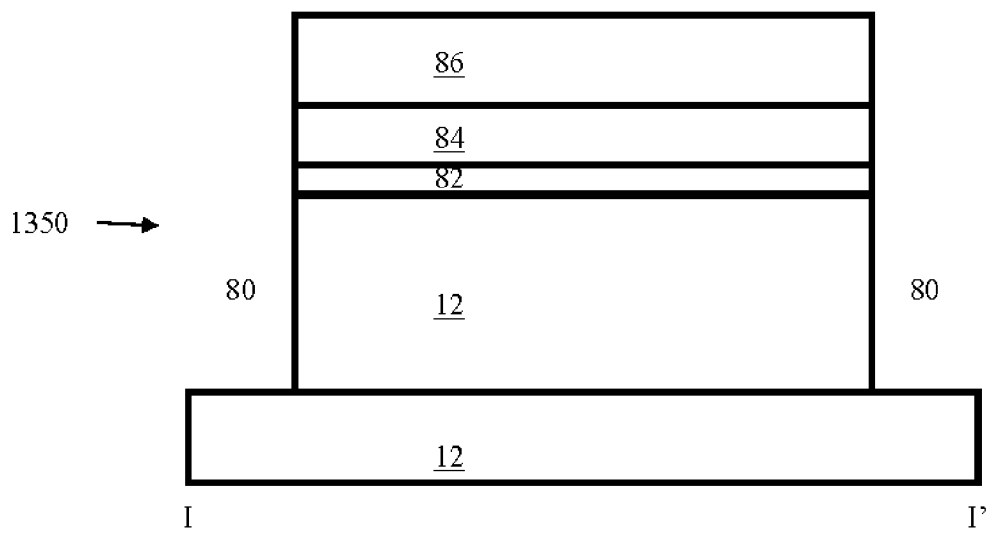


FIG. 197B

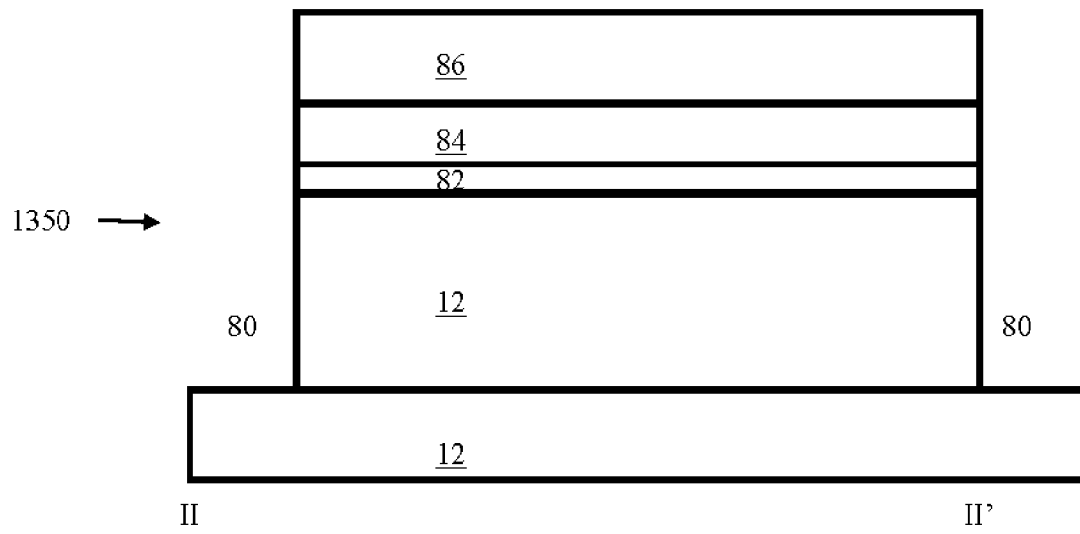


FIG. 197C

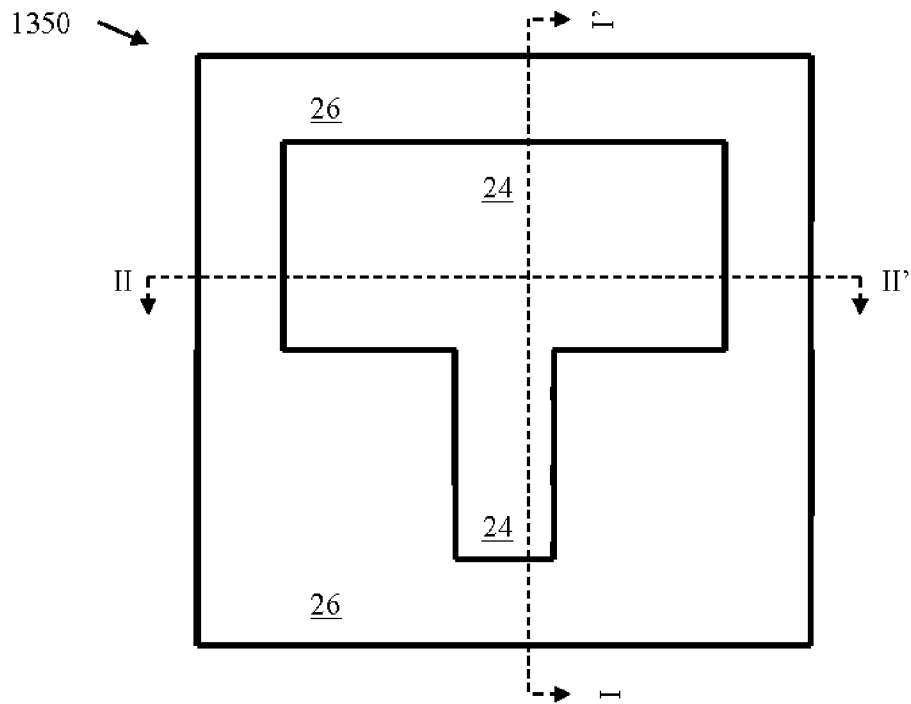


FIG. 197D

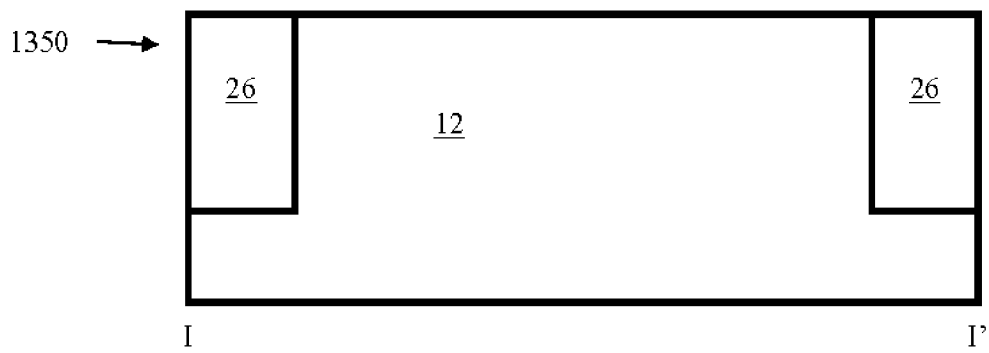


FIG. 197E

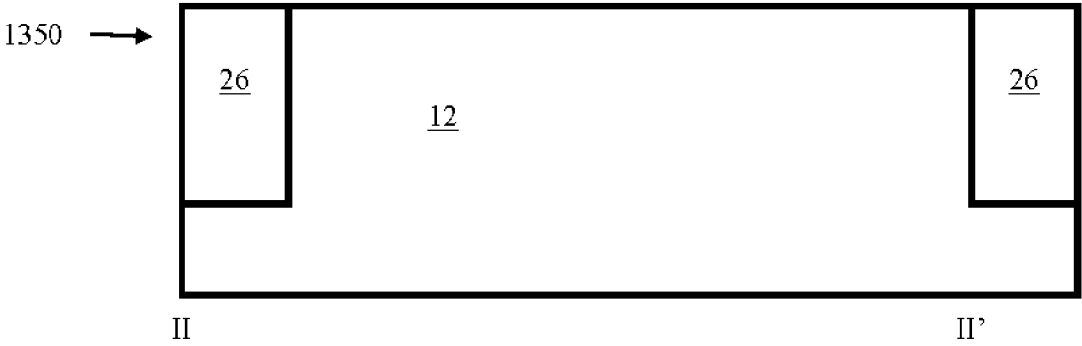


FIG. 197F

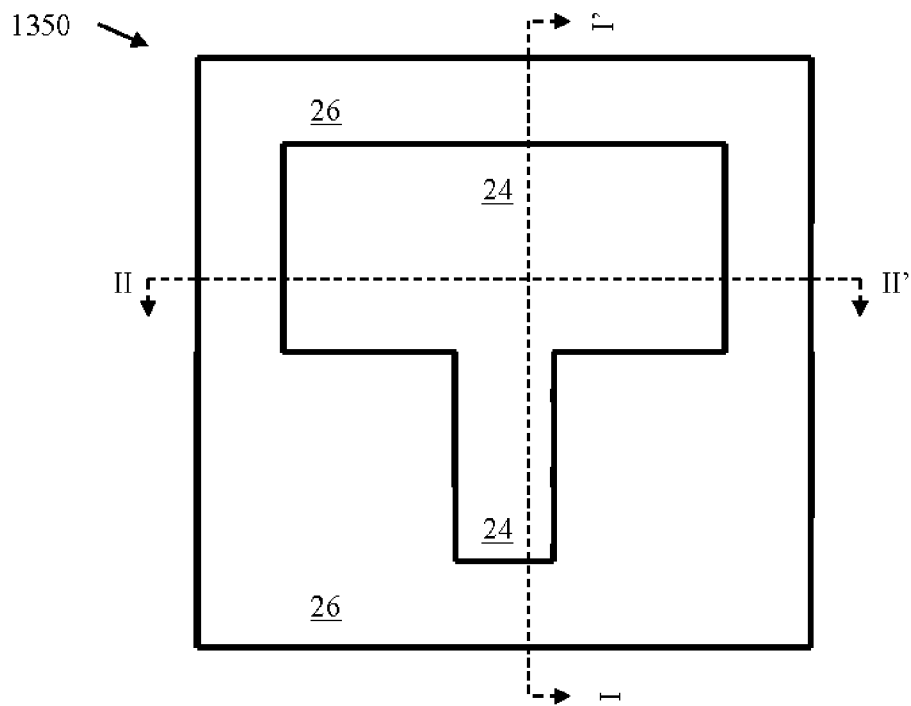


FIG. 197G

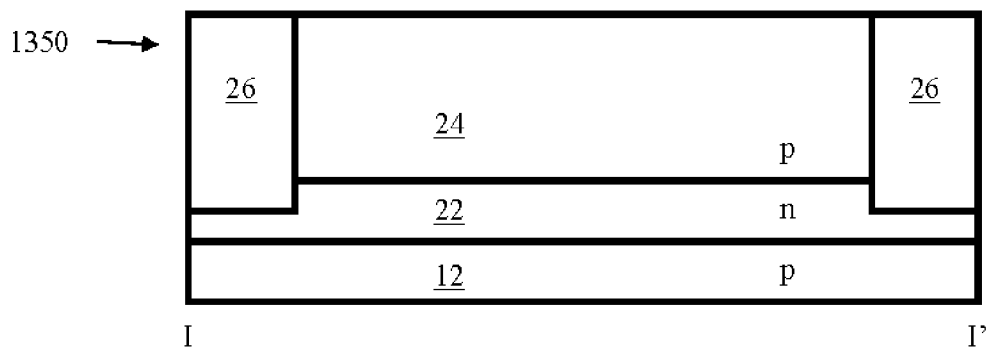


FIG. 197H

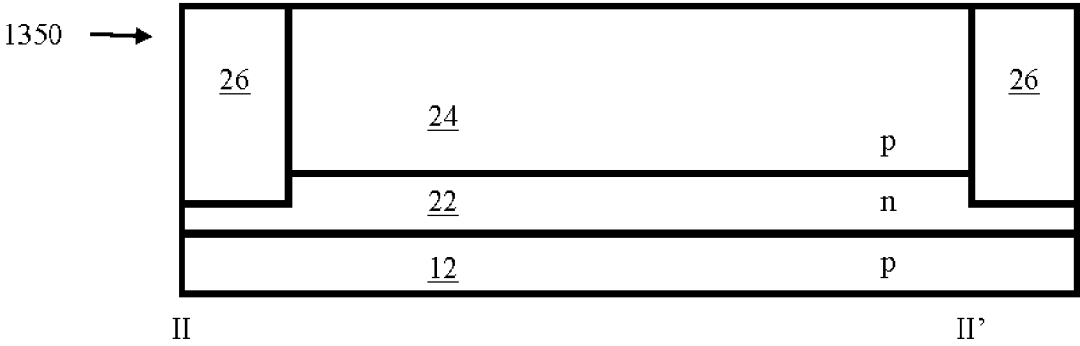


FIG. 197I

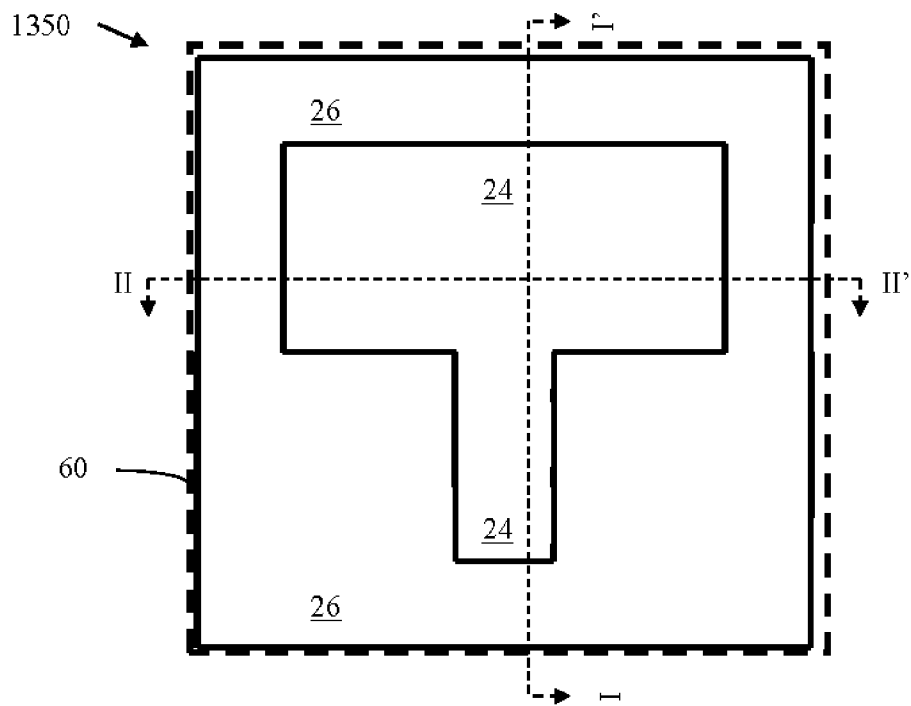


FIG. 197J

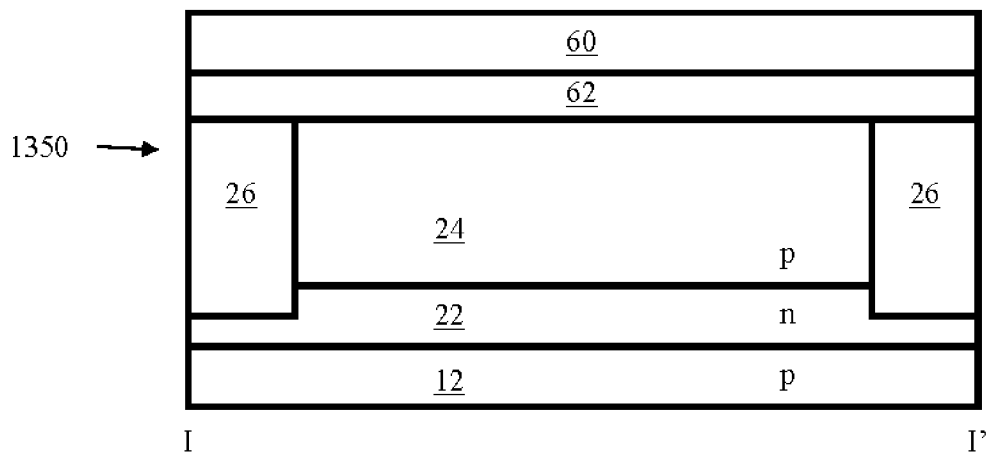


FIG. 197K

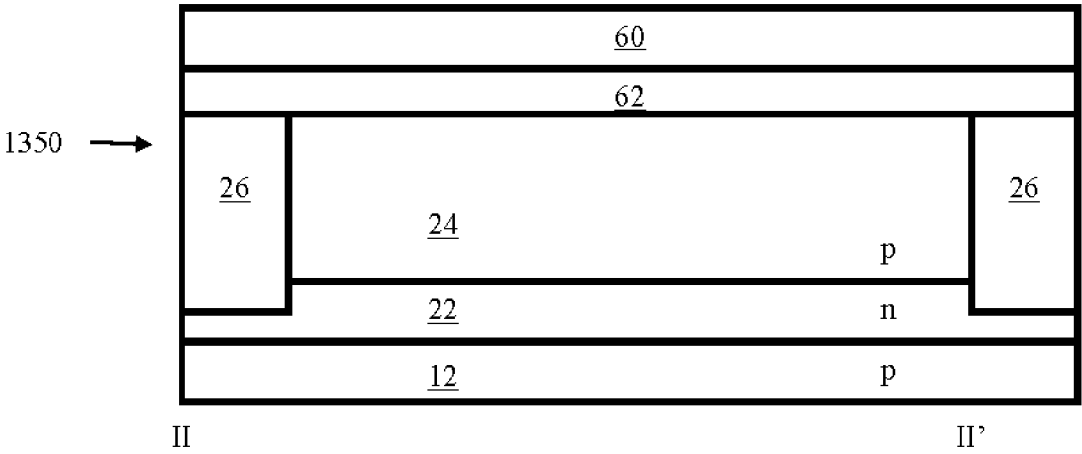


FIG. 197L

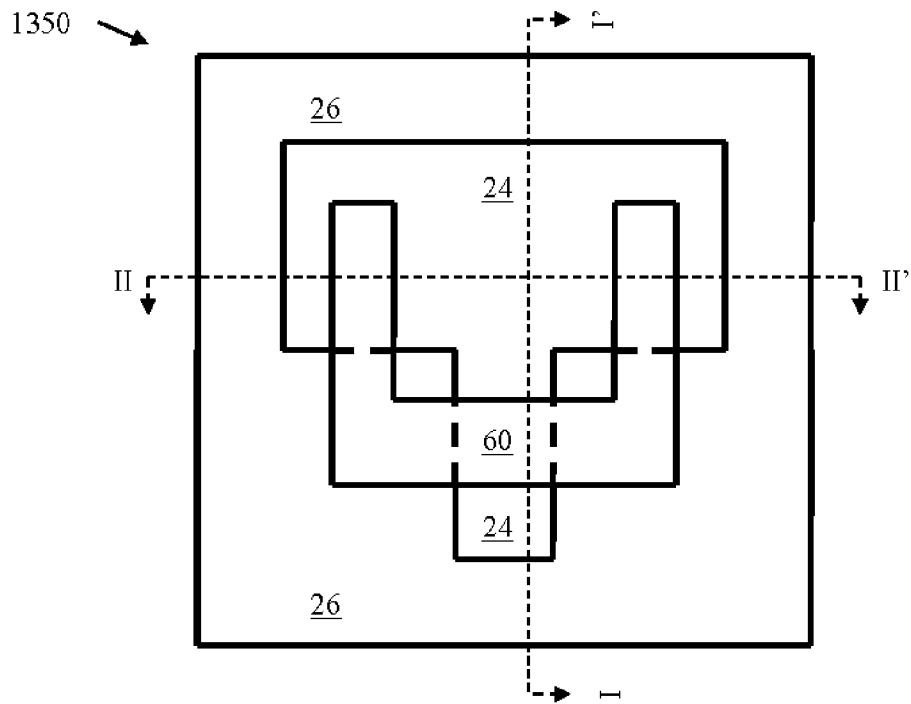


FIG. 197M

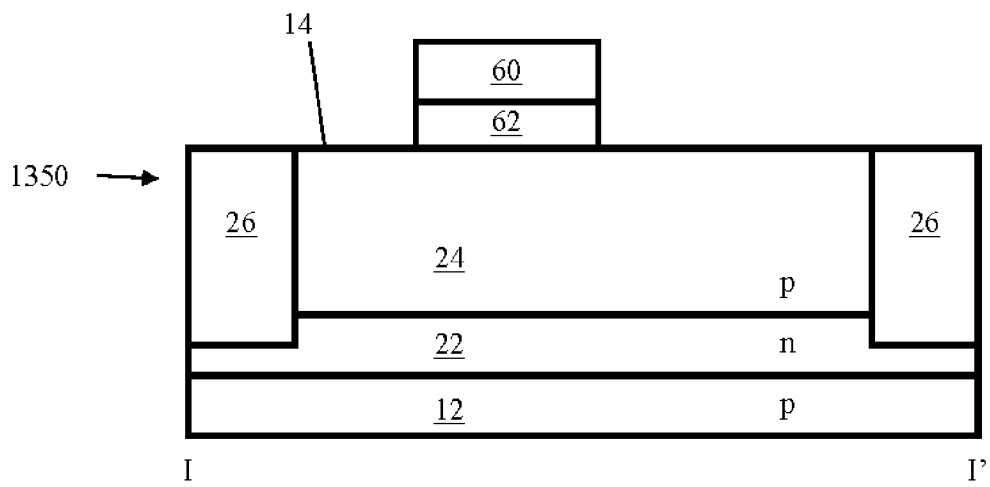


FIG. 197N

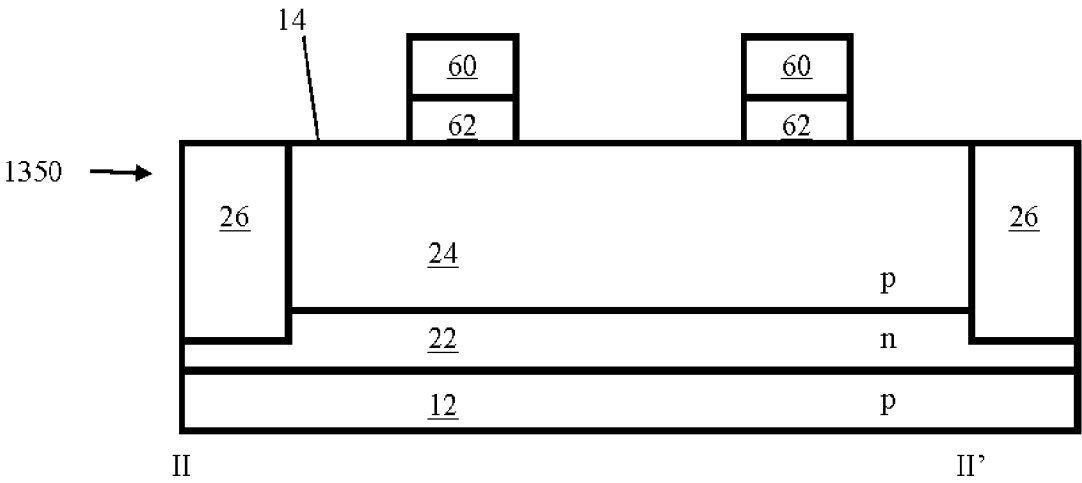


FIG. 197O

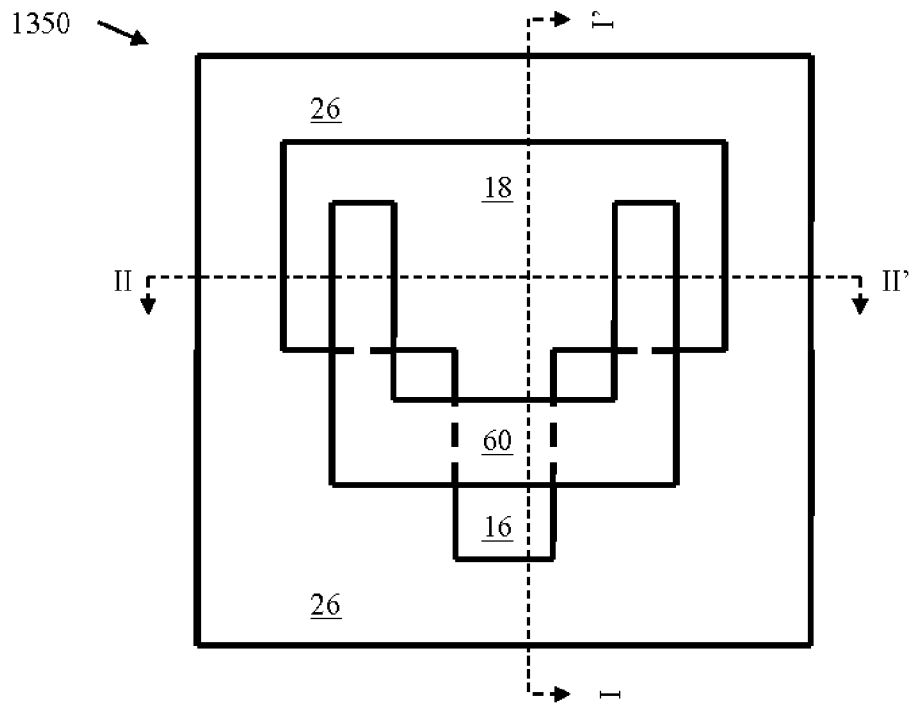


FIG. 197P

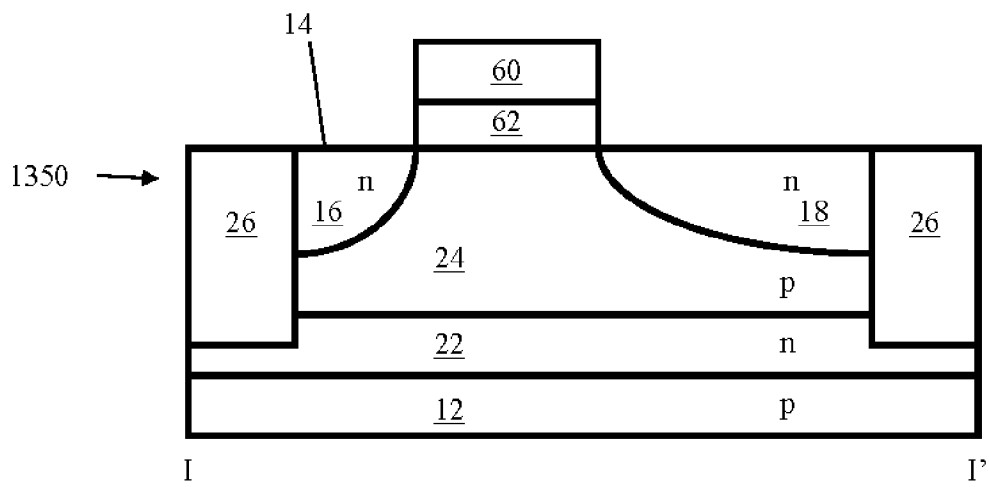


FIG. 197Q

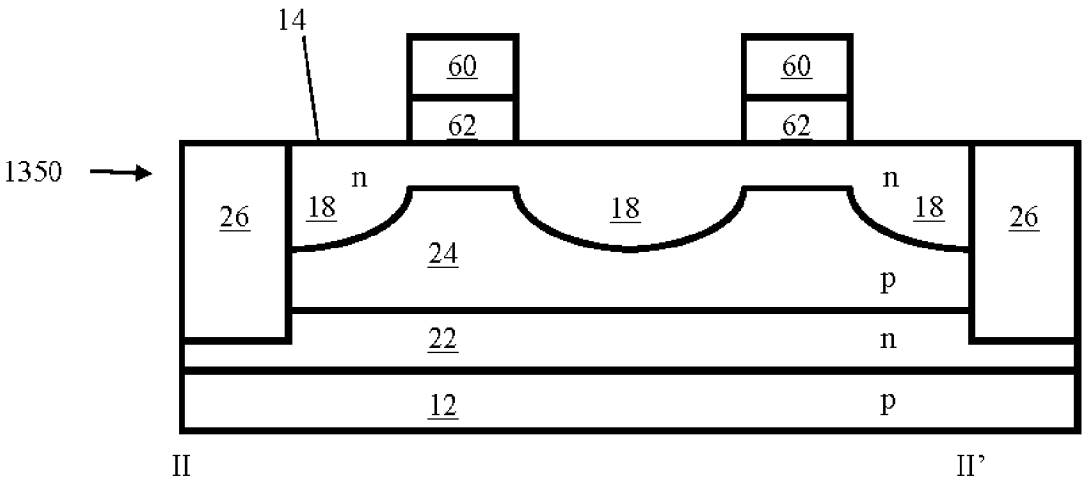


FIG. 197R

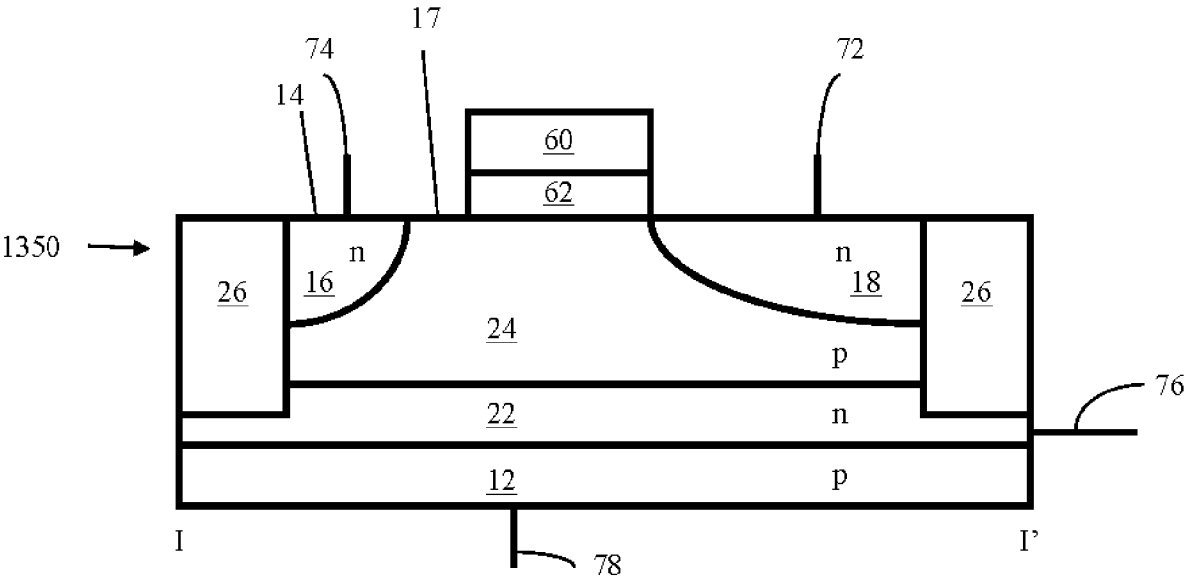


FIG. 198

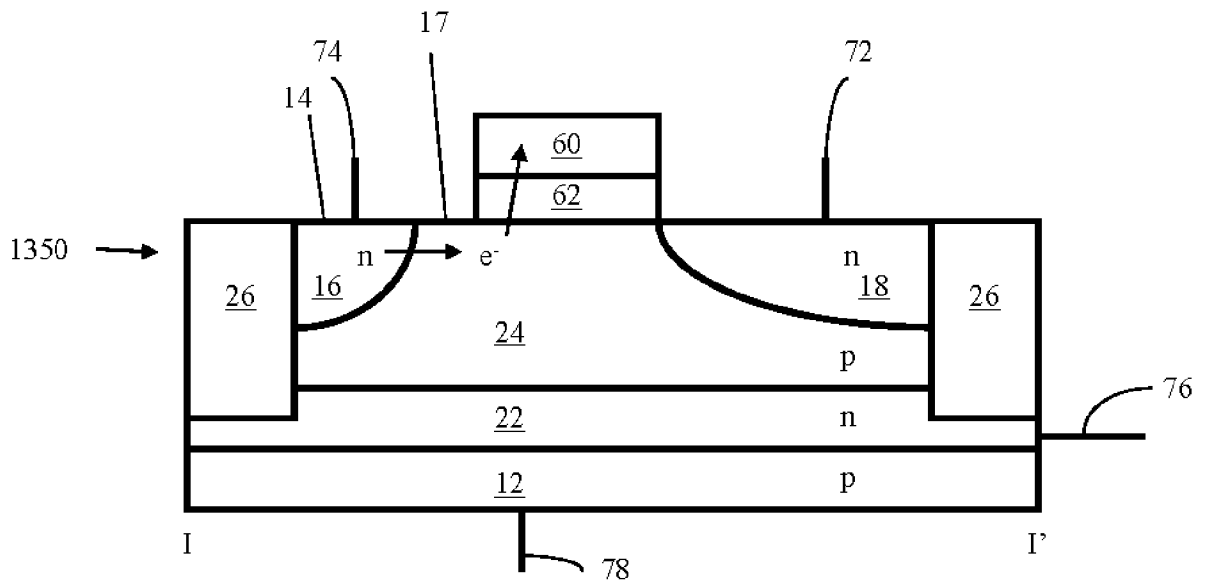


FIG. 199A

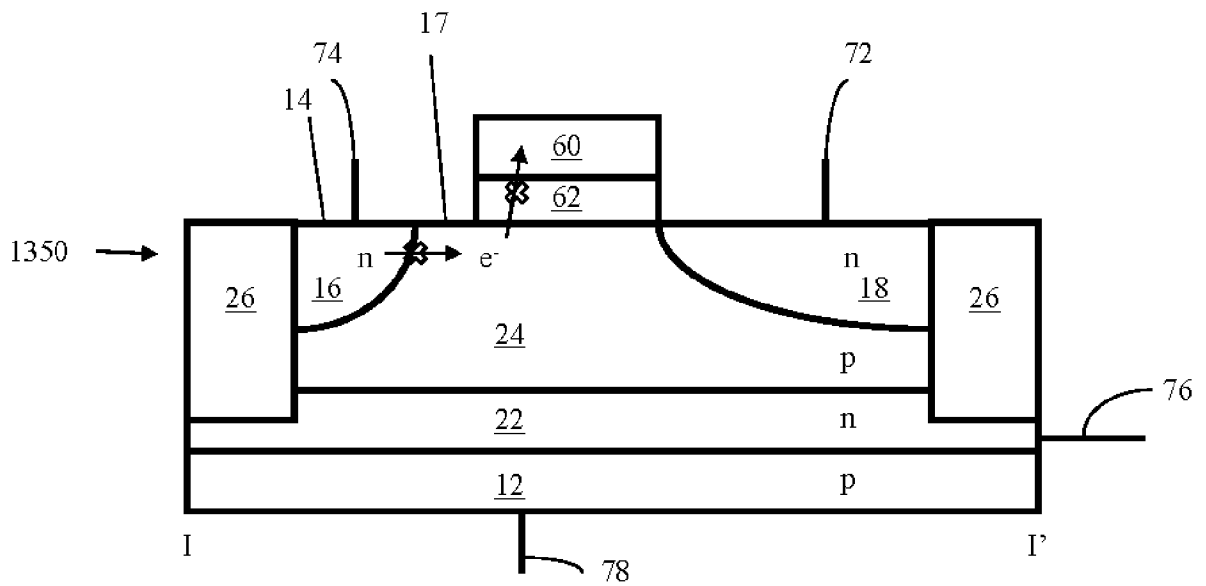


FIG. 199B

Restore Operation
(All Memory Cells 1350)

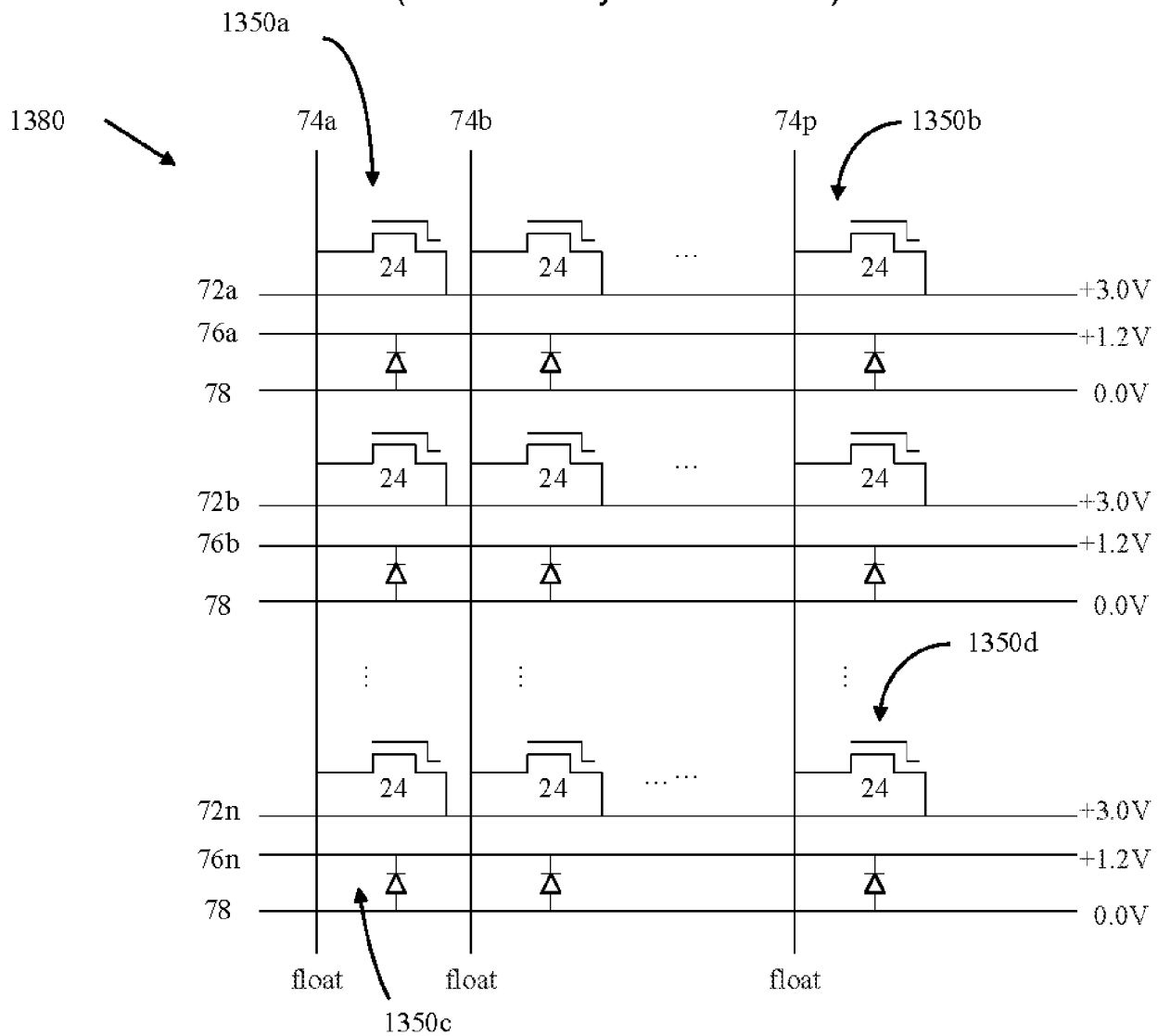


FIG. 200A

Reset Operation (All Memory Cells 1350)

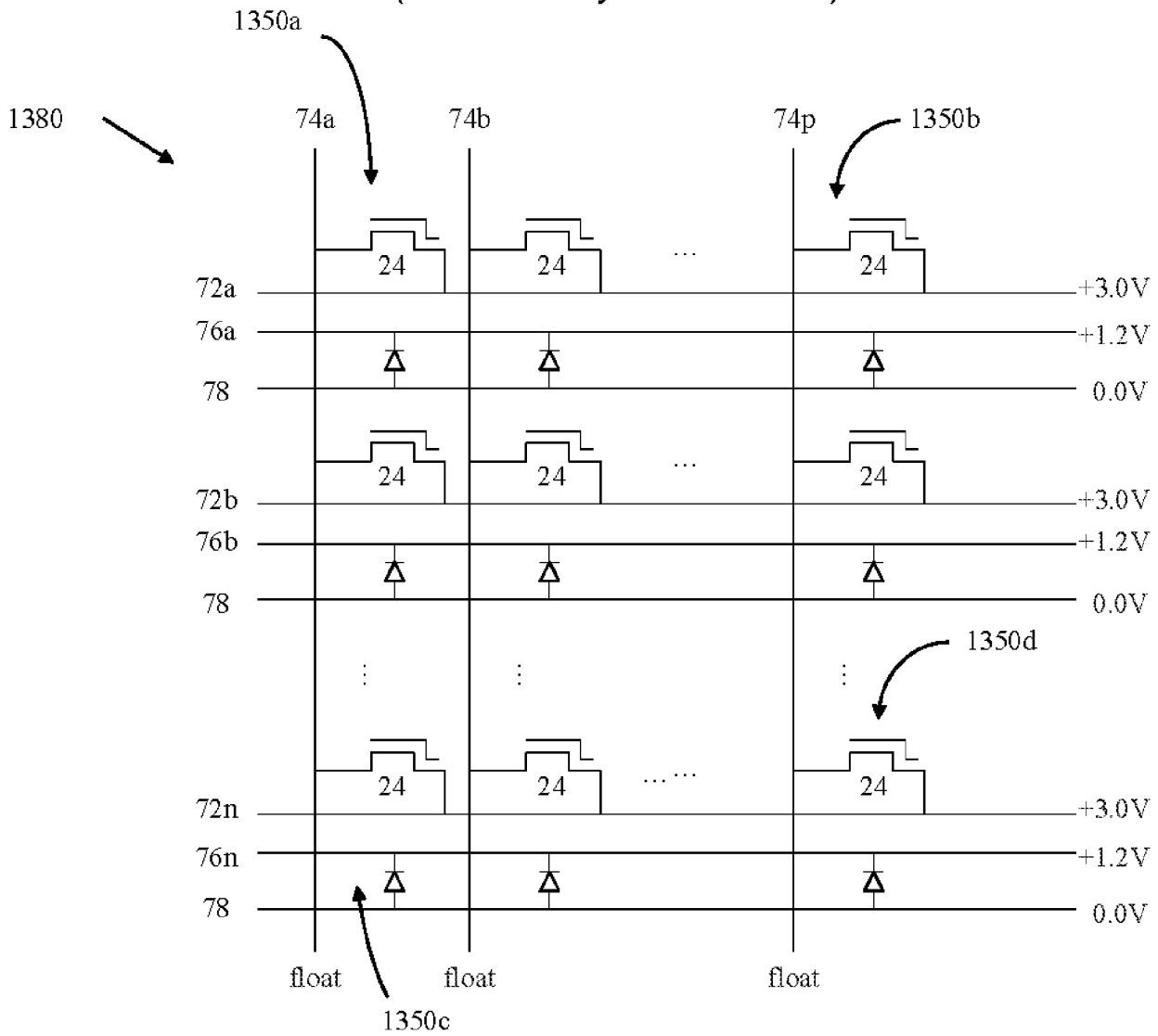


FIG. 201

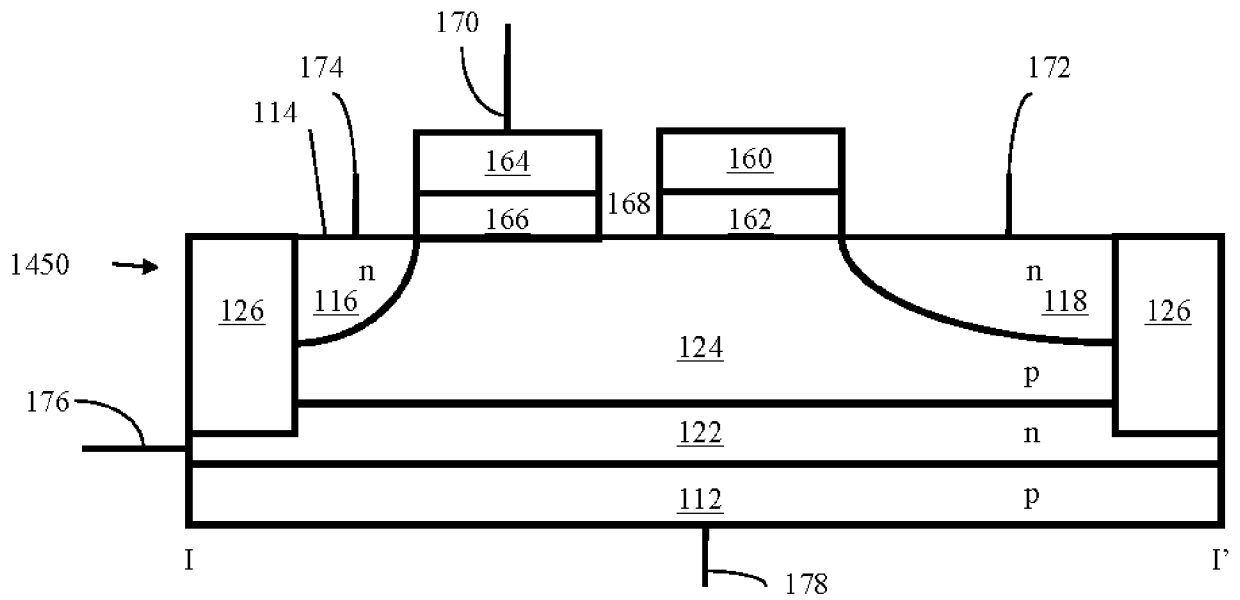


FIG. 202A

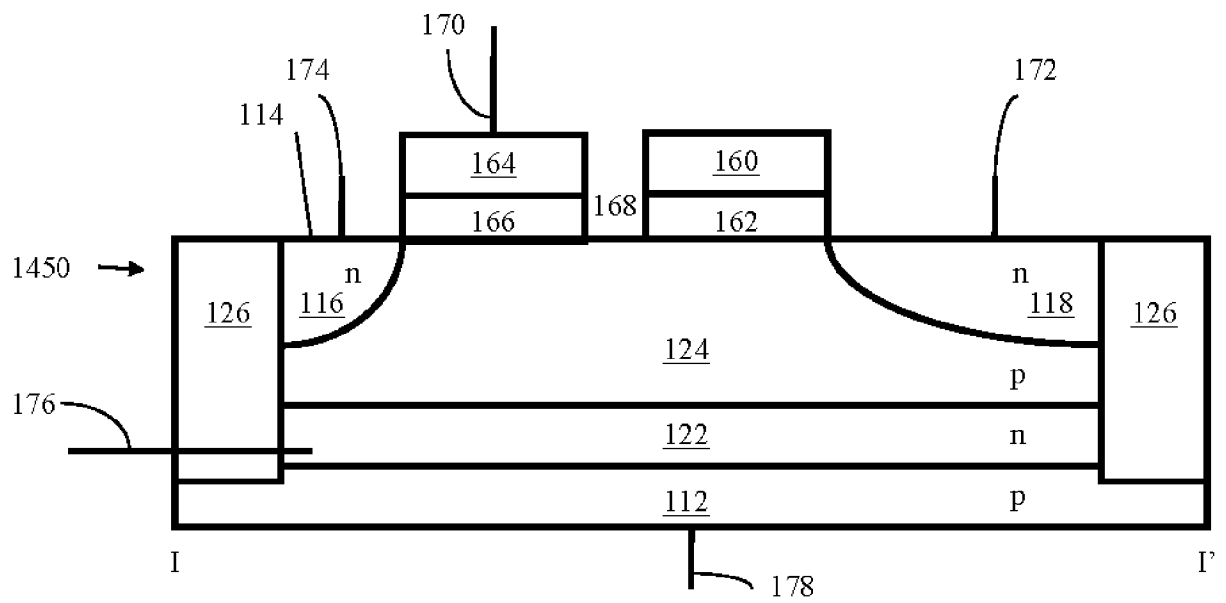


FIG. 202B

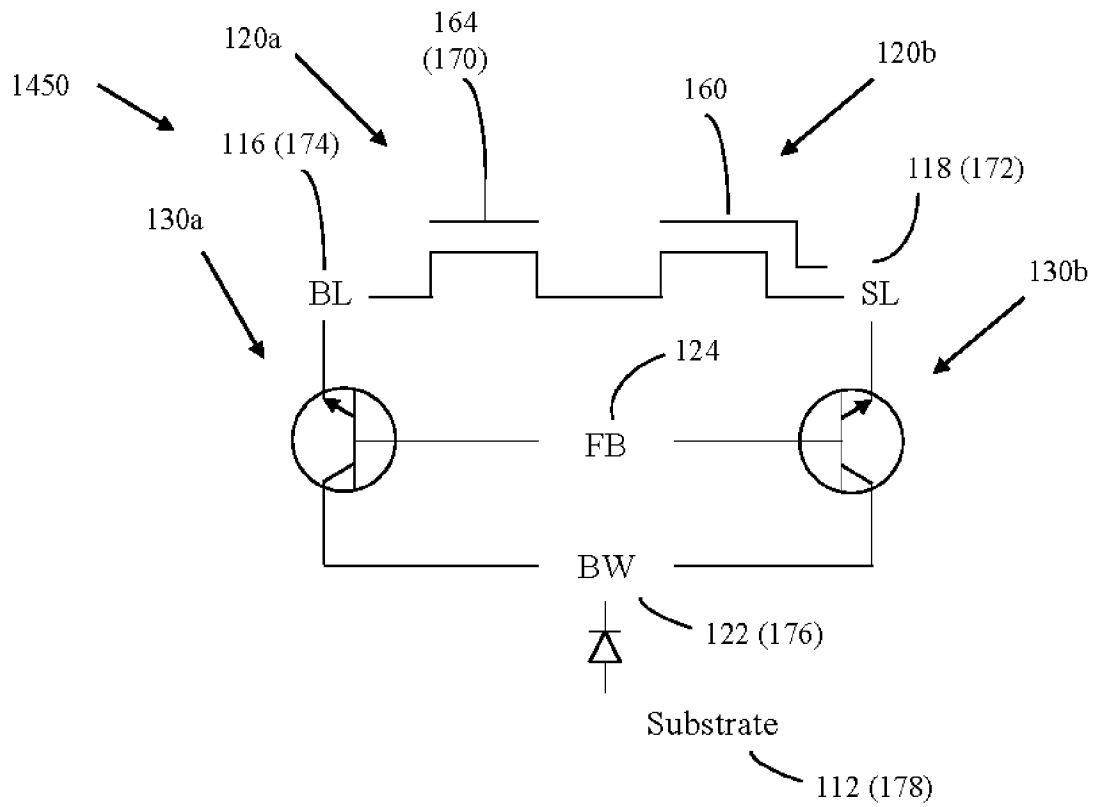


FIG. 203

Exemplary Memory Array 1480 with
Representative Memory Cells 1450a, 1450b, 1450c
and 1450d

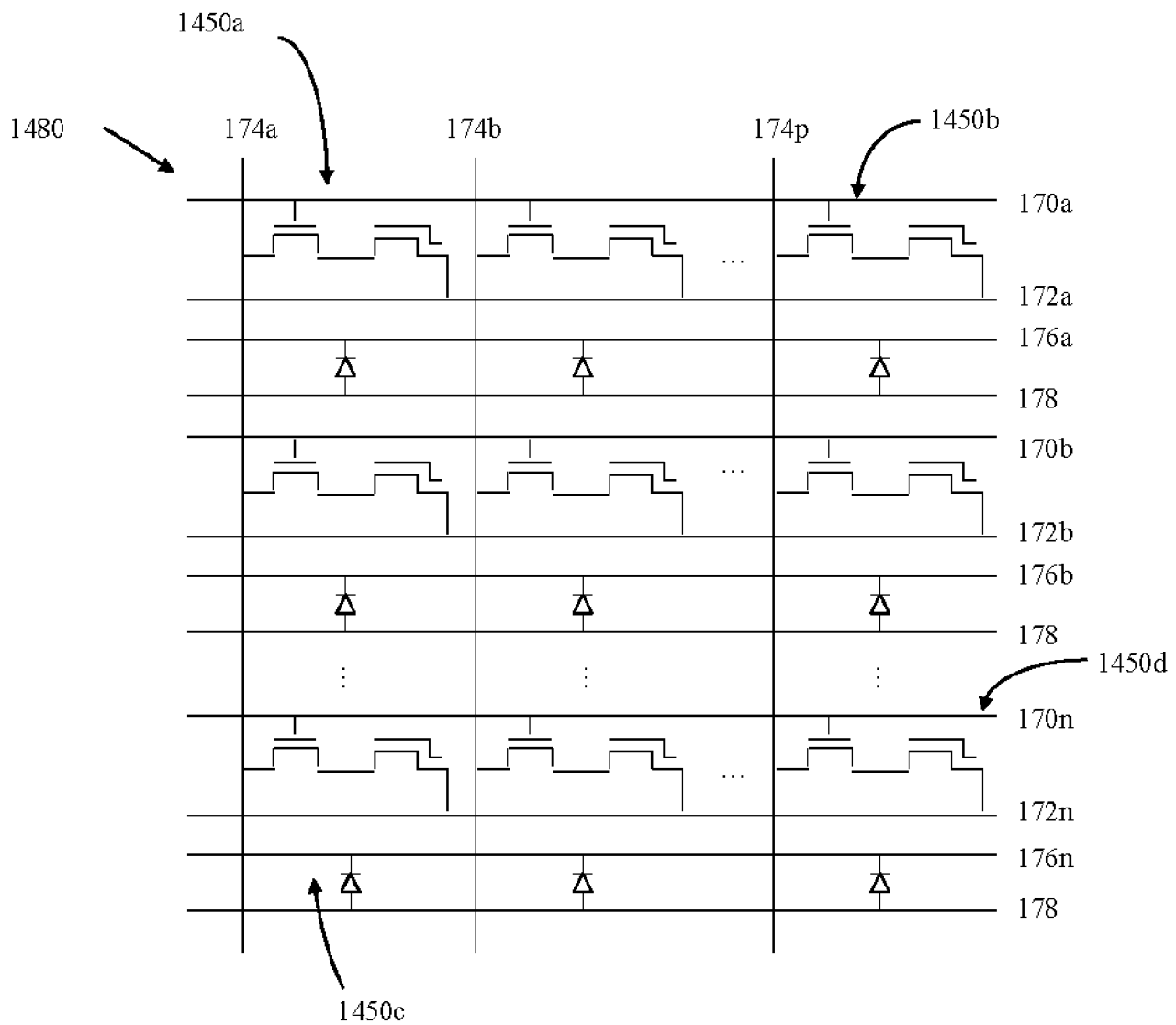


FIG. 204

Array Hold Operation (All Memory Cells 1450)

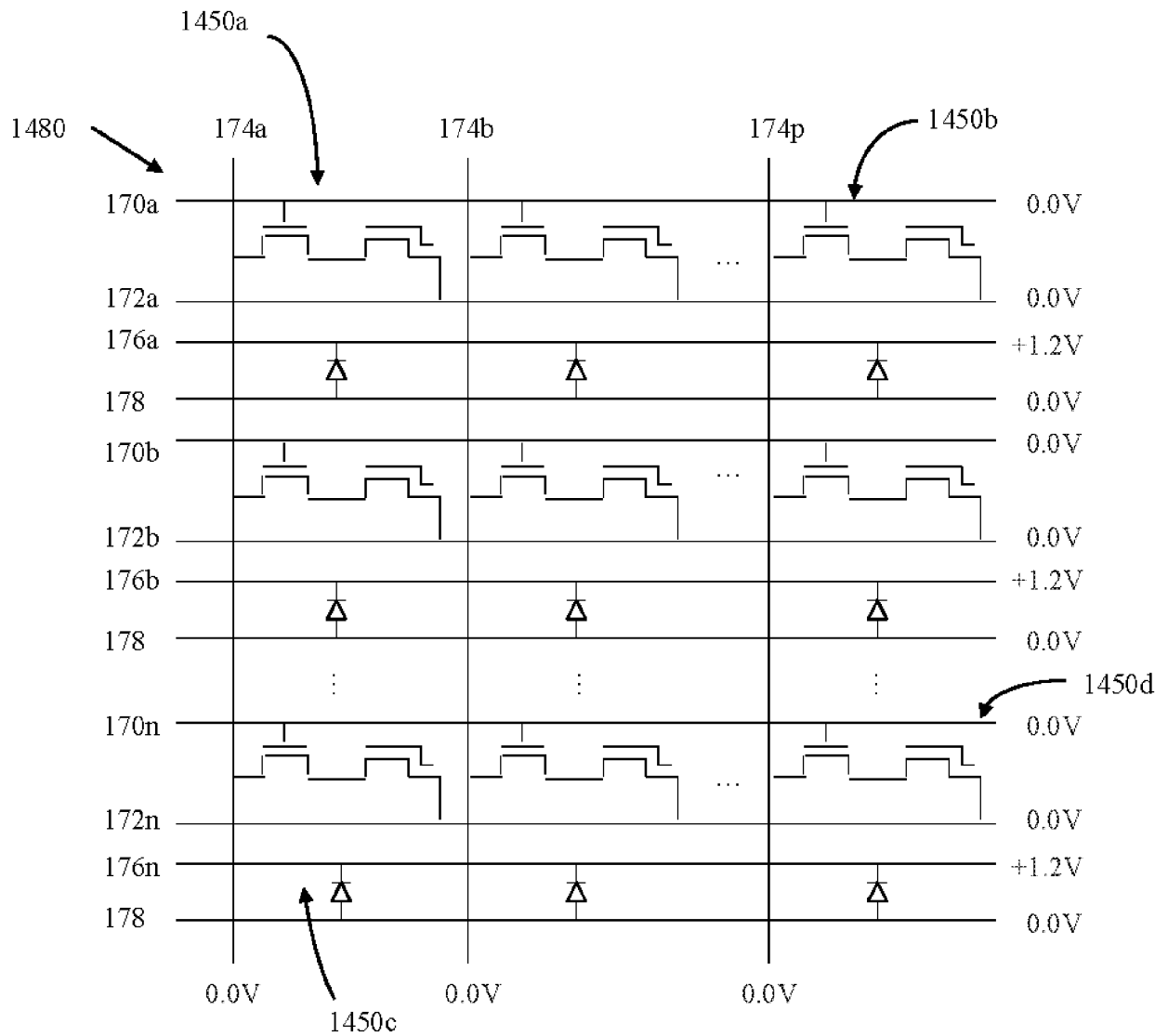


FIG. 205

FIG. 206

Write Logic-0 Operation (Memory Cells 1450a, 1450b)

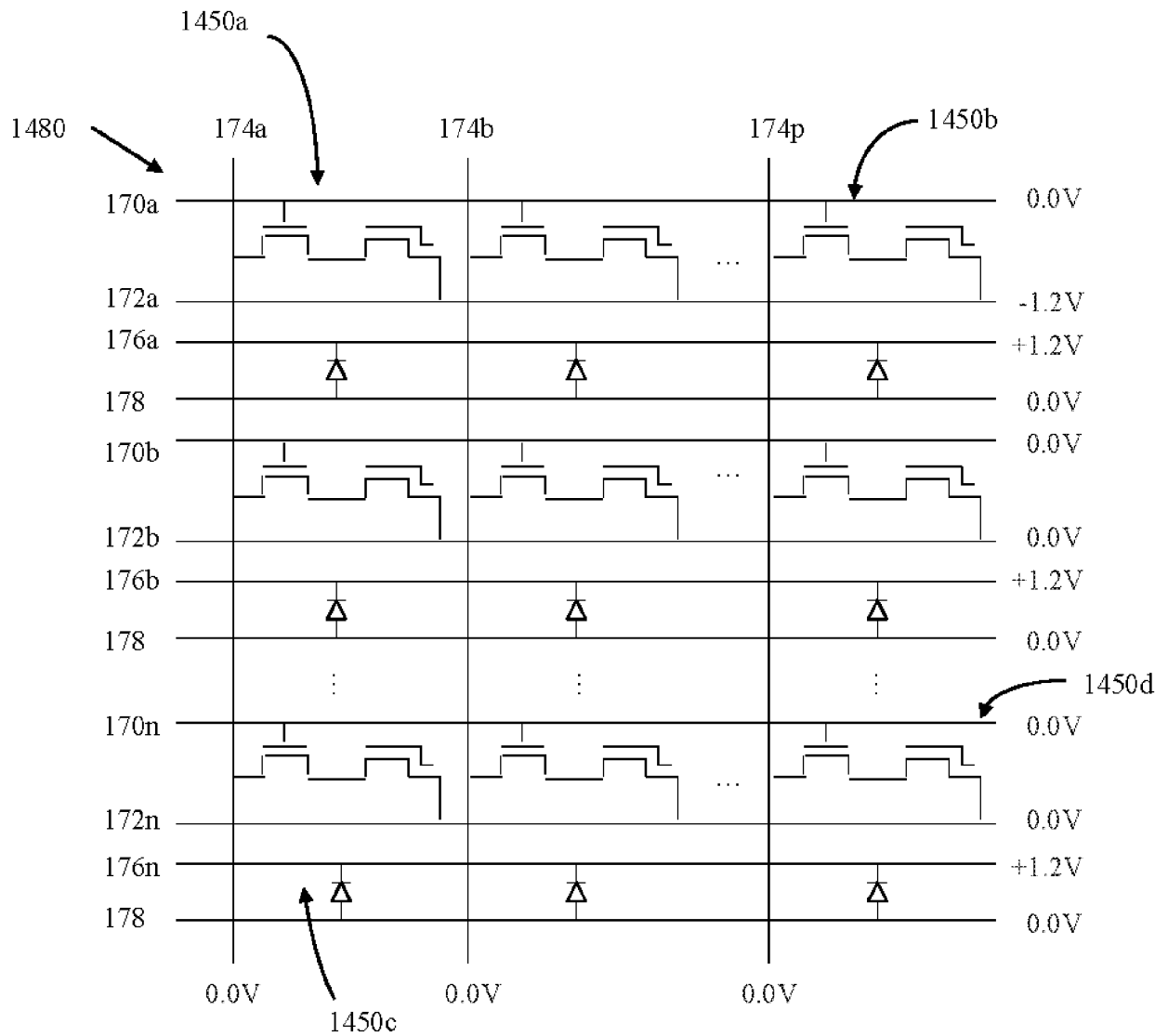


FIG. 207A

Write Logic-0 Operation (Memory Cells 1450a, 1450c)

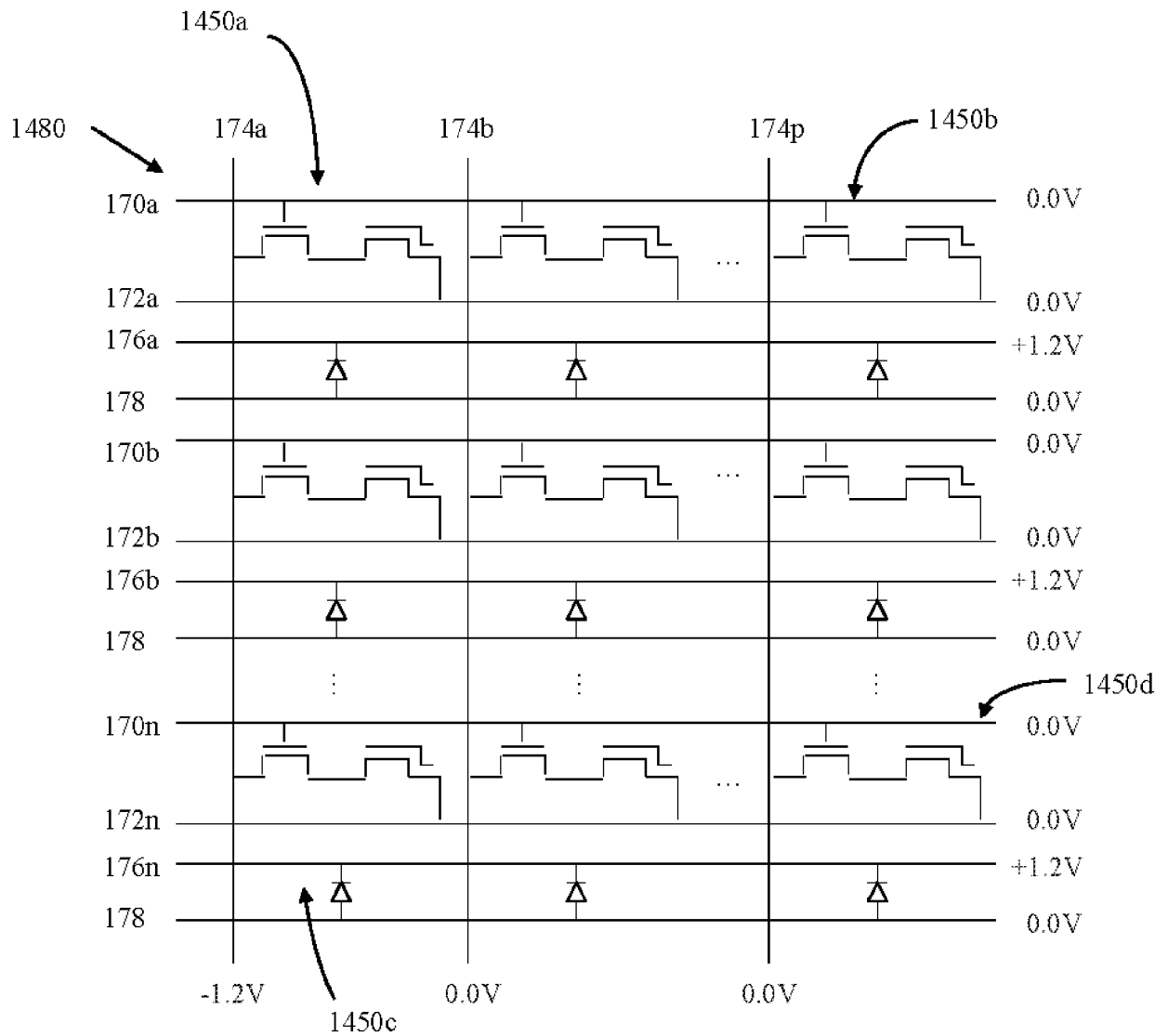


FIG. 207B

Write Logic-0 Operation (Memory Cell 1450a)

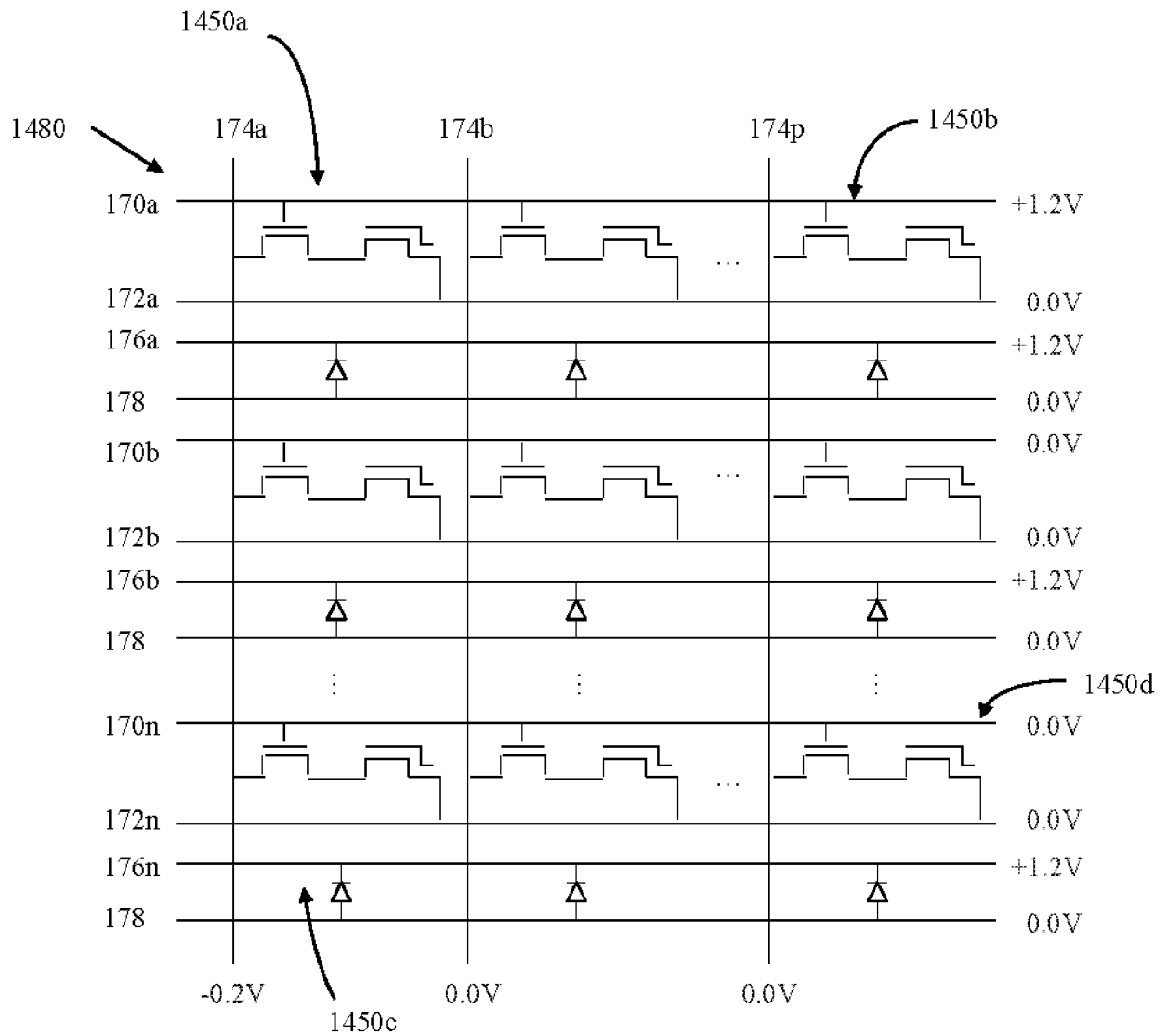


FIG. 207C

Write Logic-1 Operation (Memory Cell 1450a)

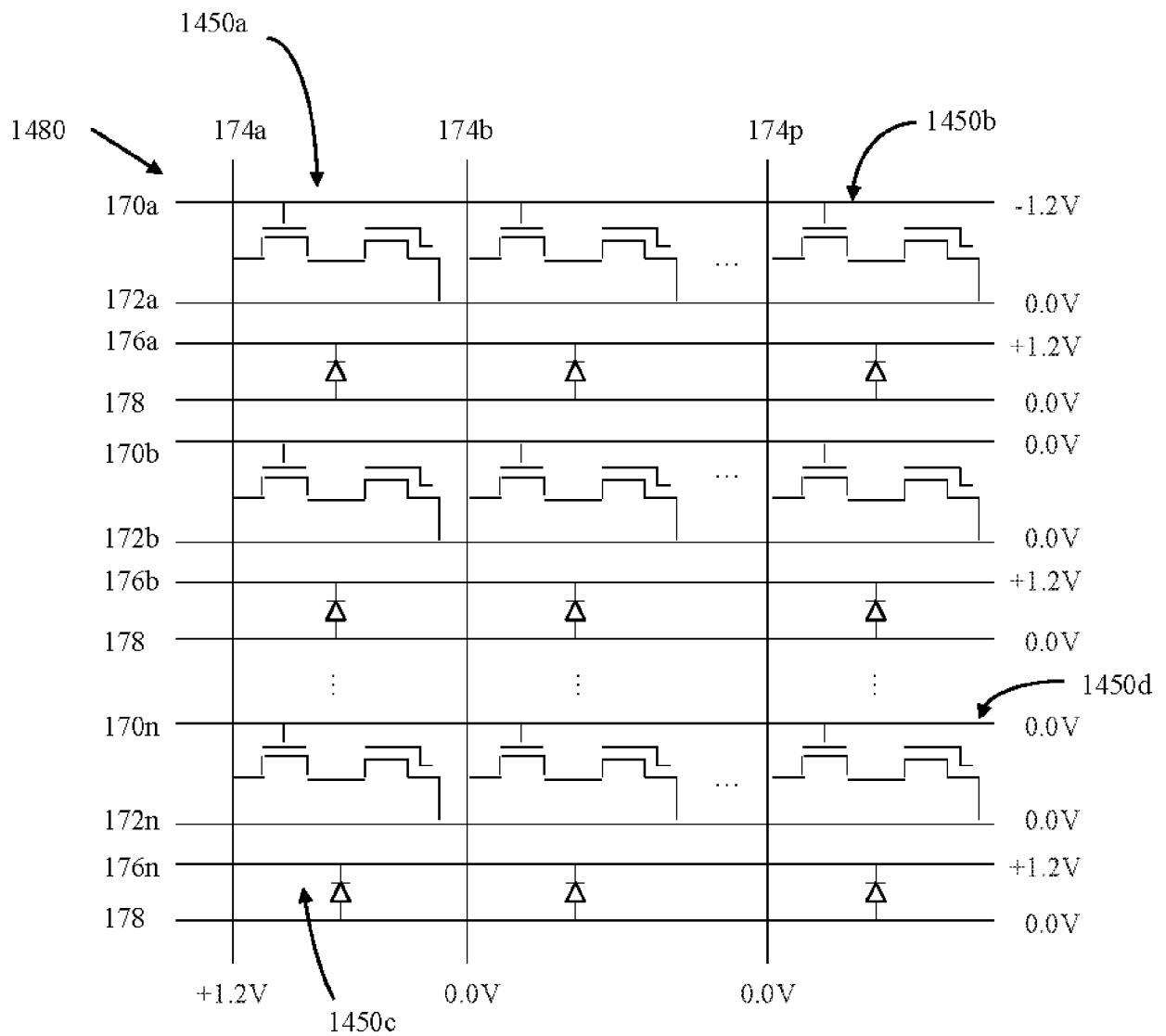


FIG. 208A

Write Logic-1 Operation (Memory Cell 1450a)

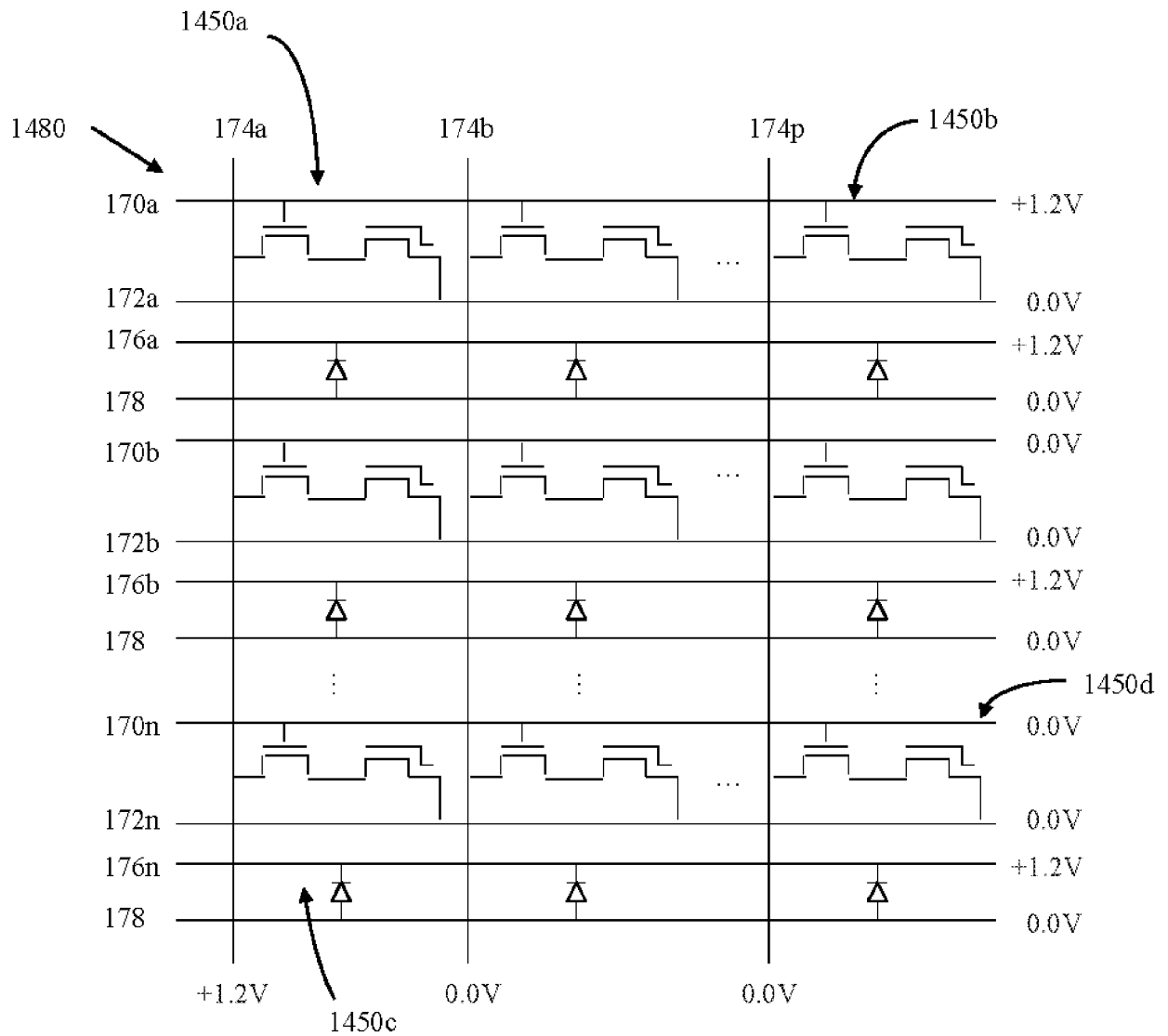


FIG. 208B

Shadowing Operation (All Memory Cells 1450)

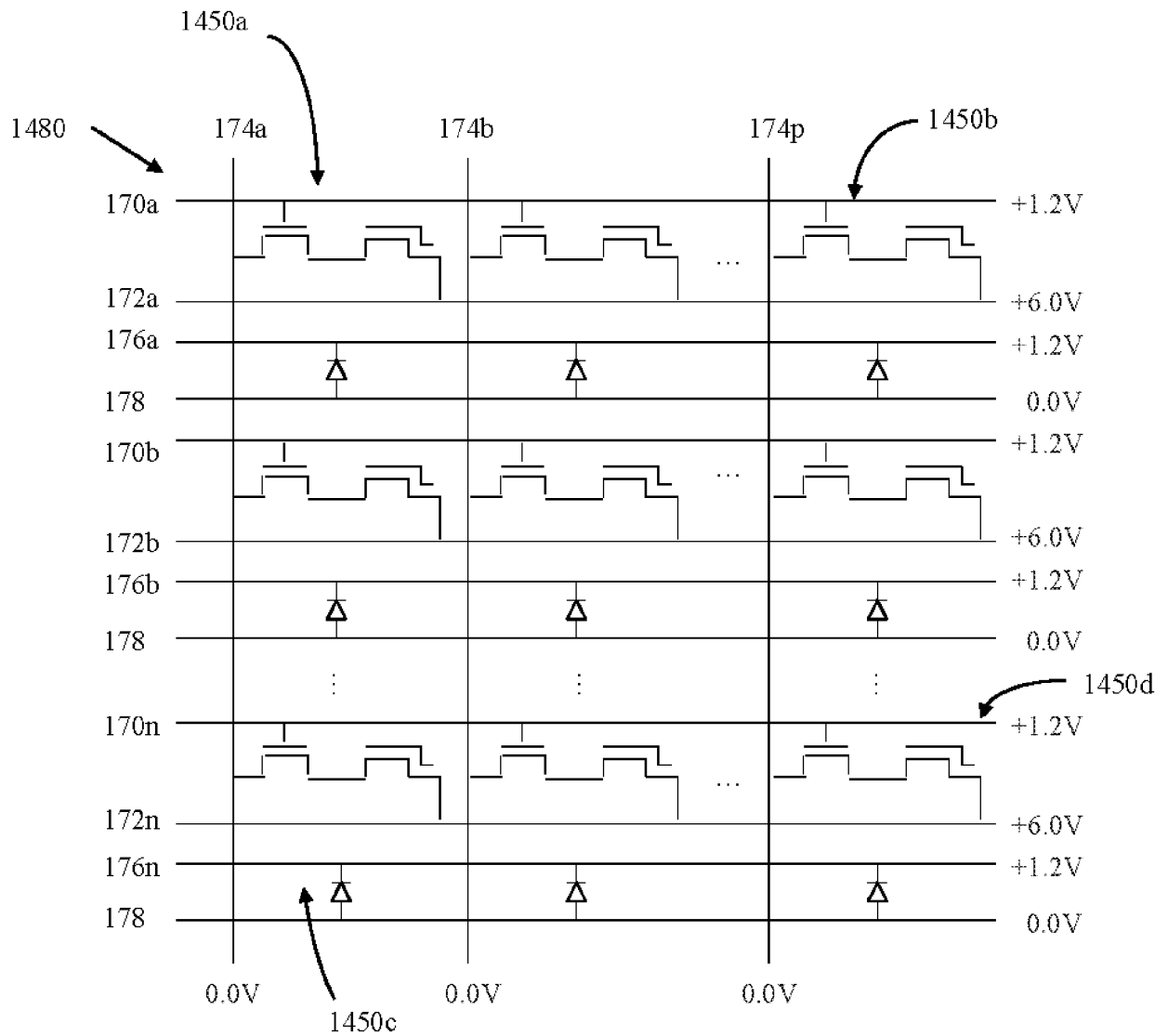


FIG. 209

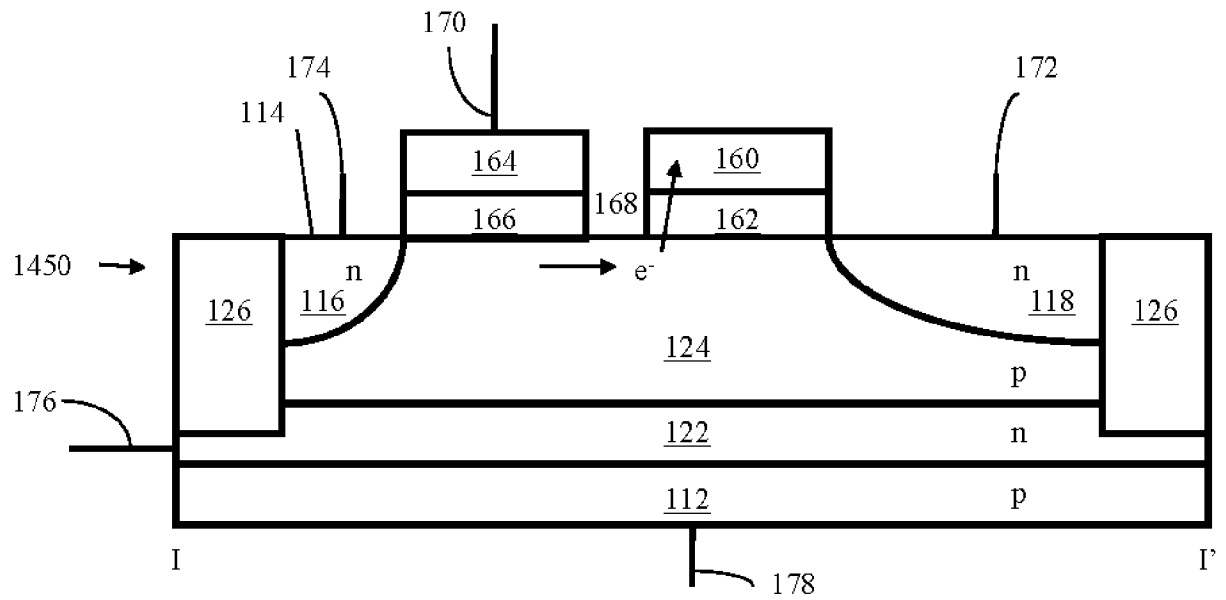


FIG. 210A

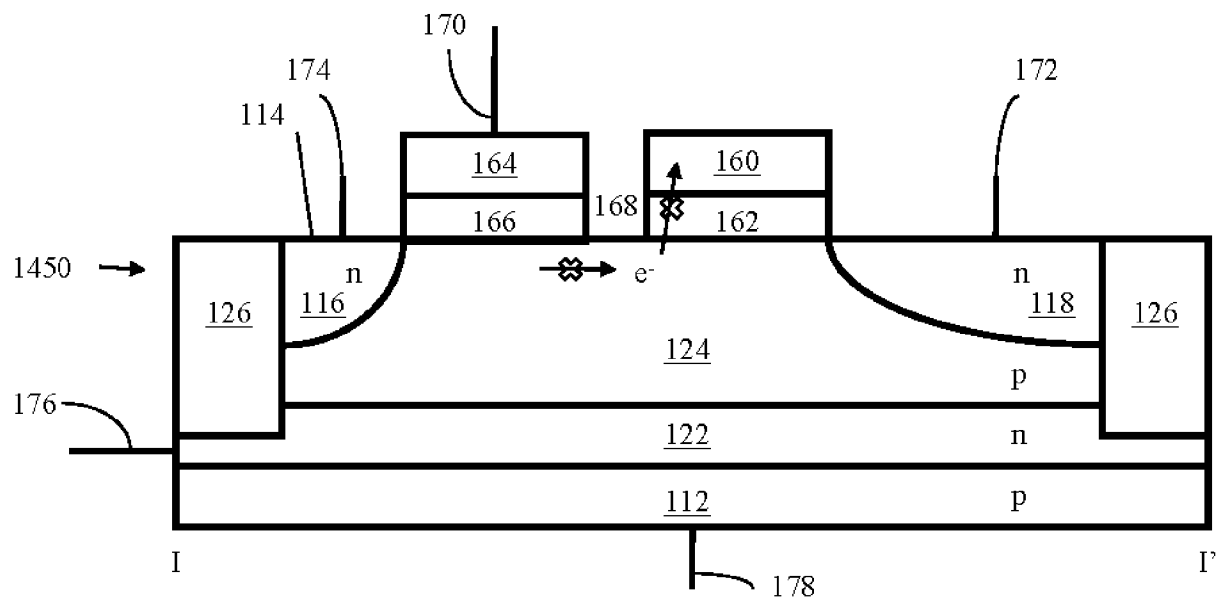


FIG. 210B

Restore Operation (All Memory Cells 1450)

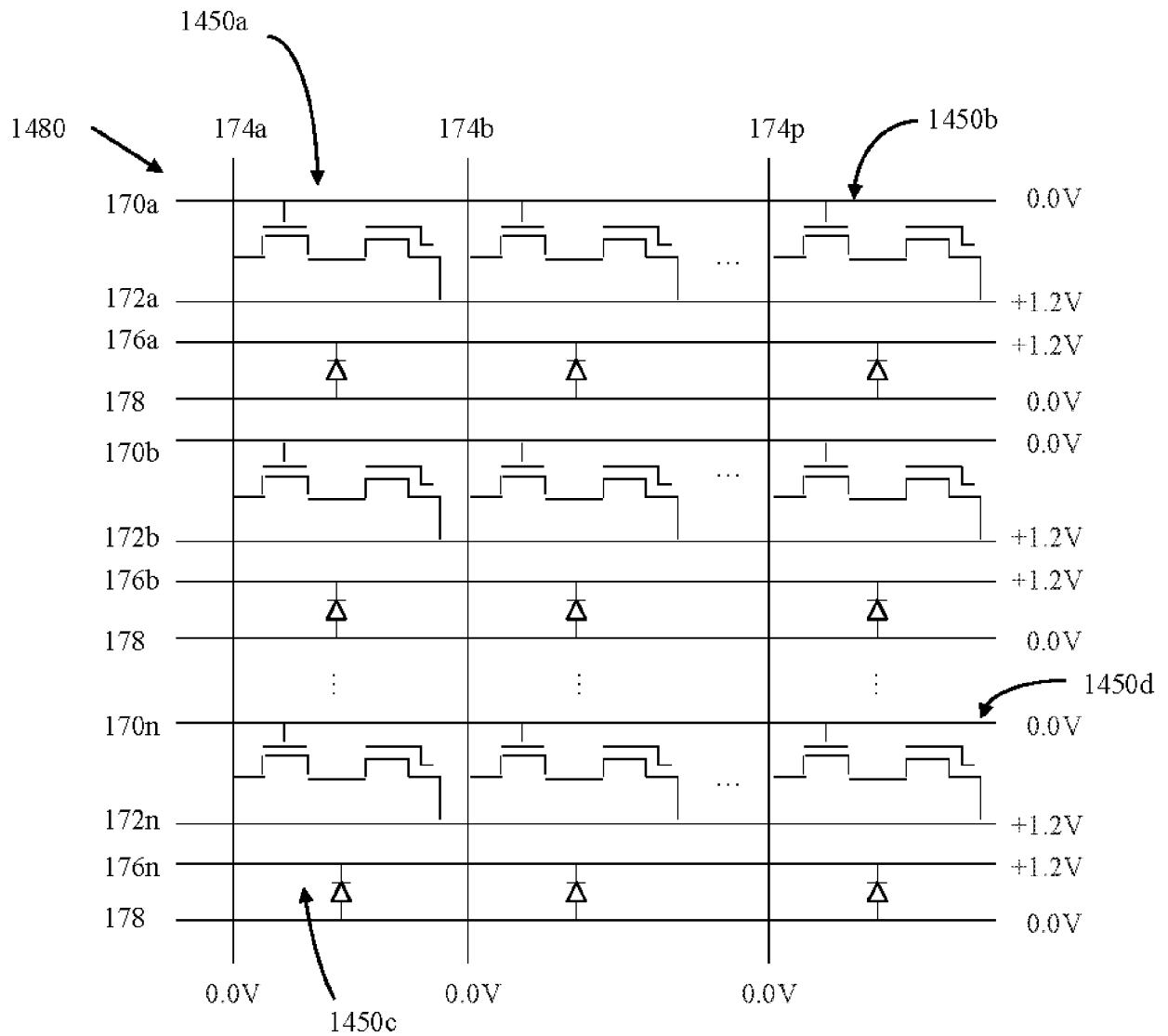


FIG. 211

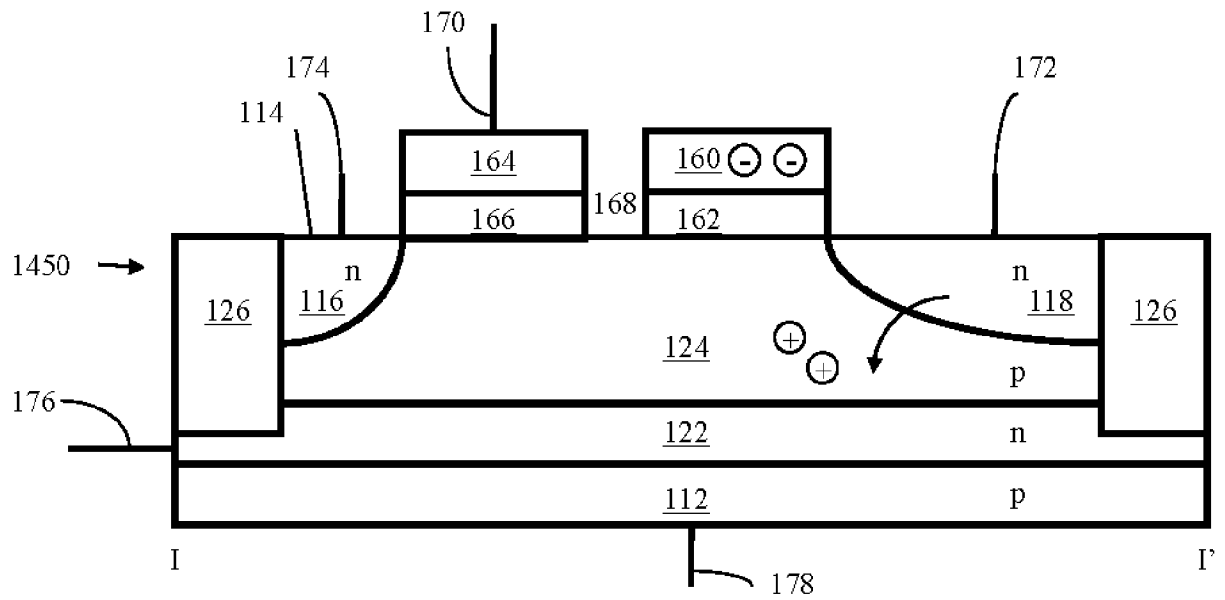


FIG. 212A

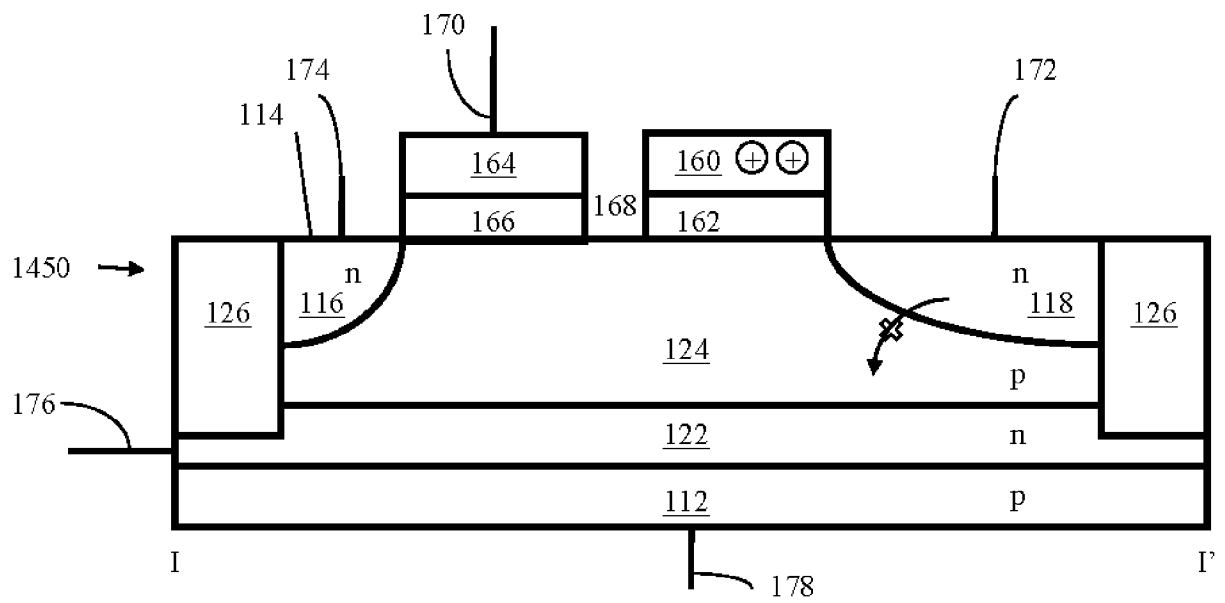


FIG. 212B

Reset Operation (All Memory Cells 1450)

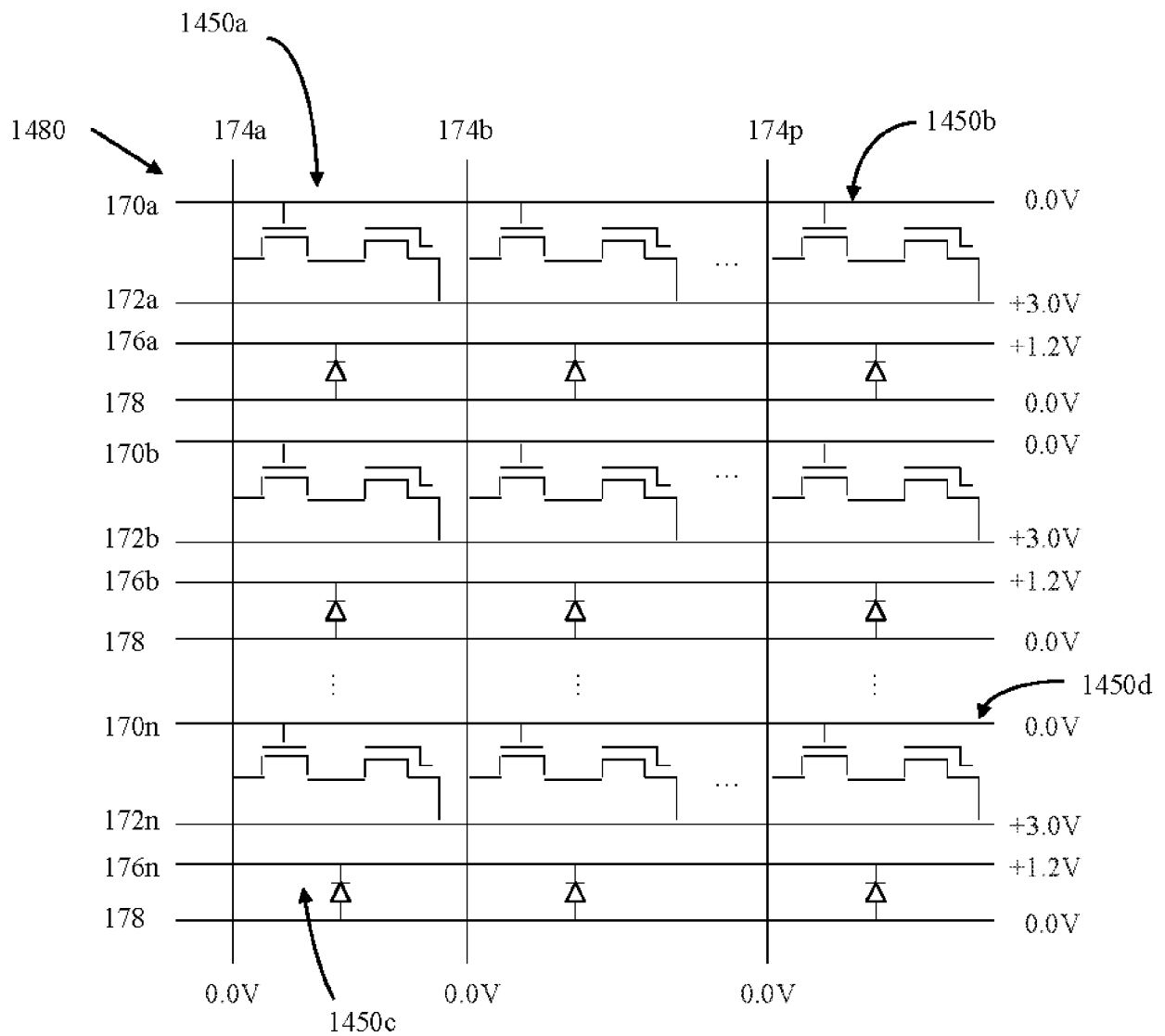


FIG. 213A

Reset Operation (All Memory Cells 1450)

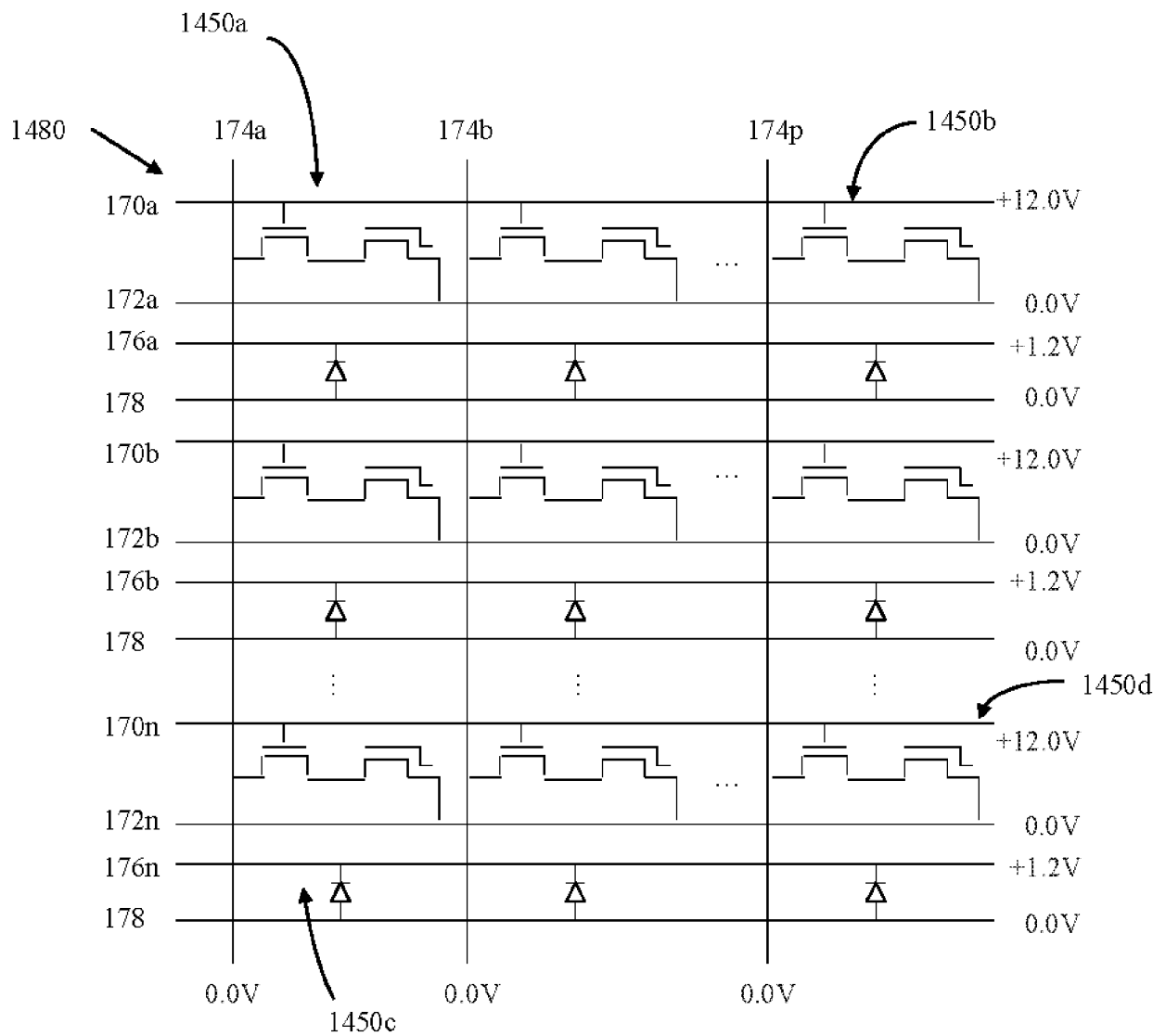


FIG. 213B

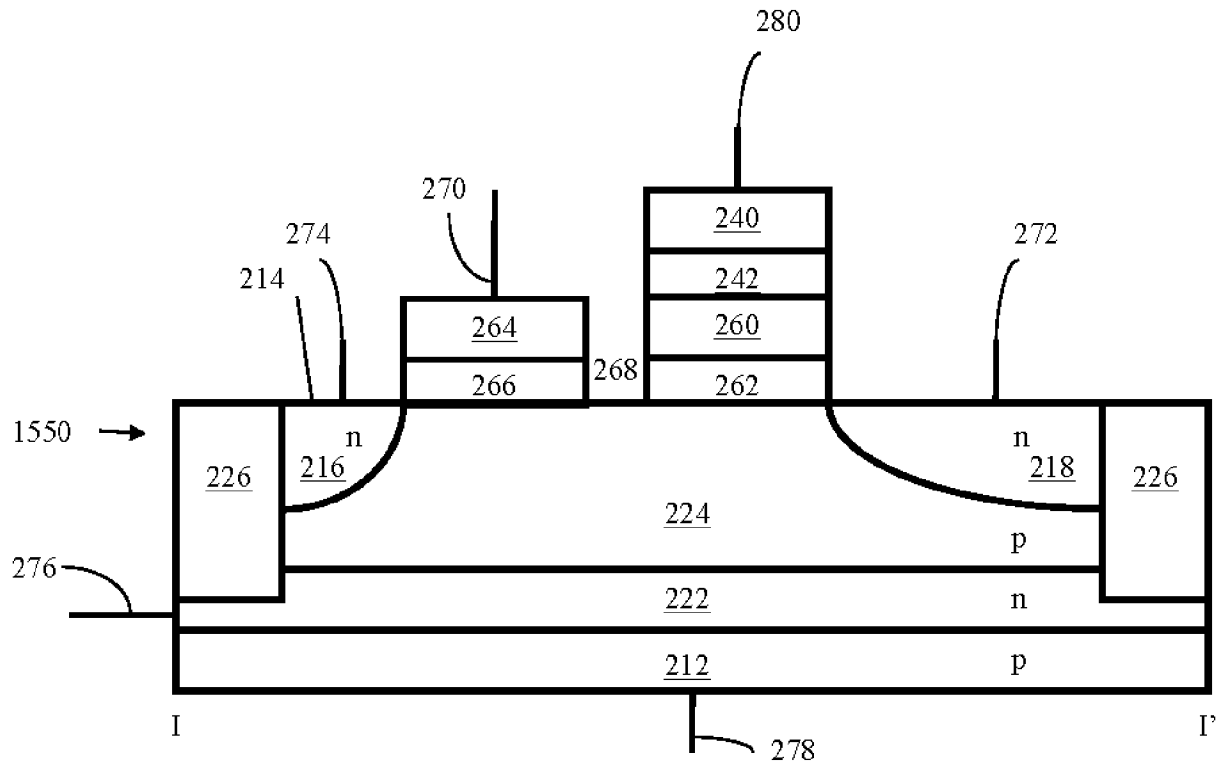


FIG. 215A

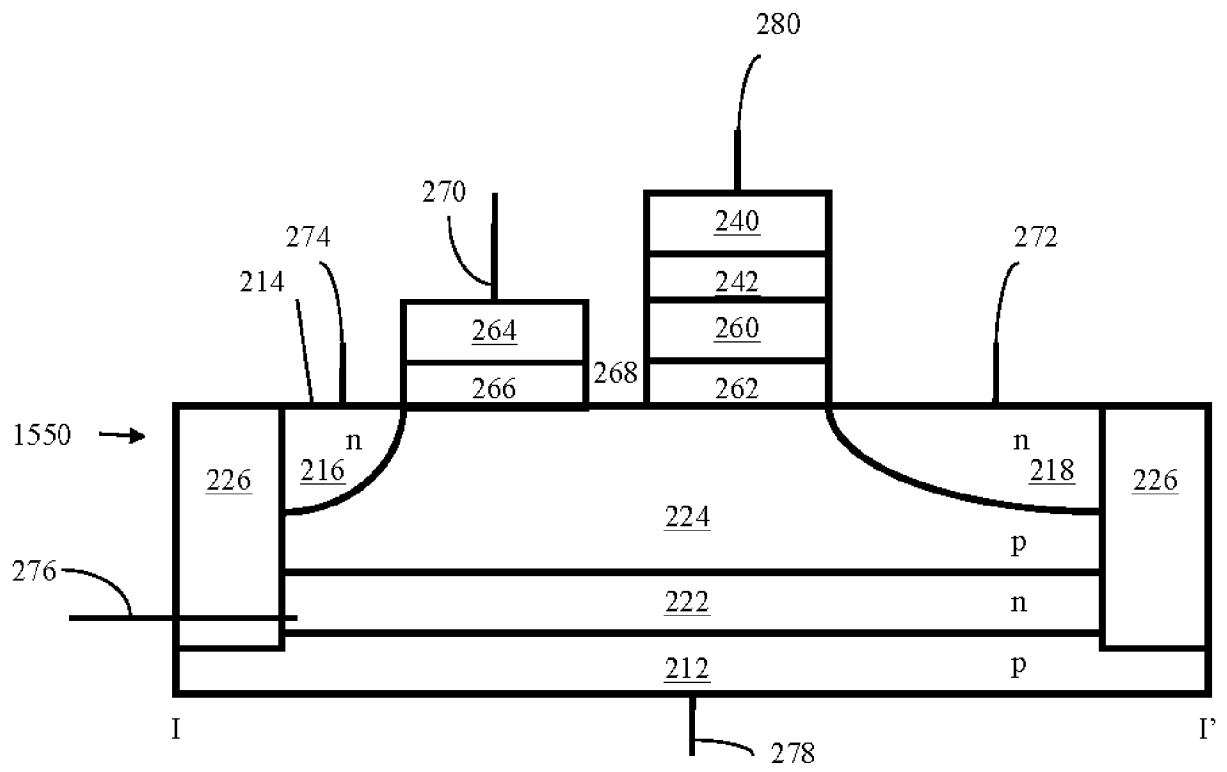


FIG. 215B

Exemplary Memory Array 1580 with
Representative Memory Cells 1550a, 1550b, 1550c
and 1550d

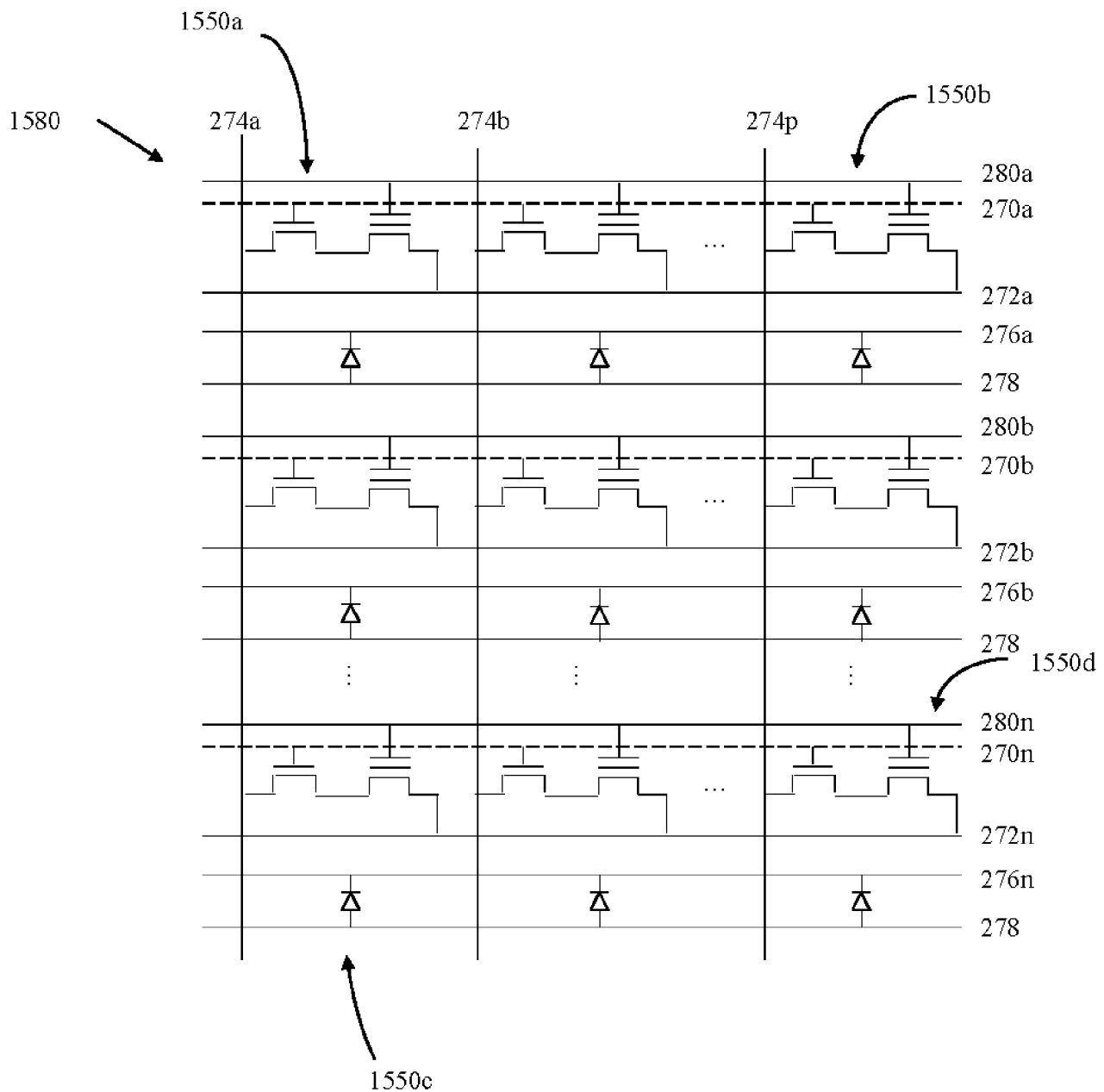


FIG. 217

Array Hold Operation (All Memory Cells 1550)

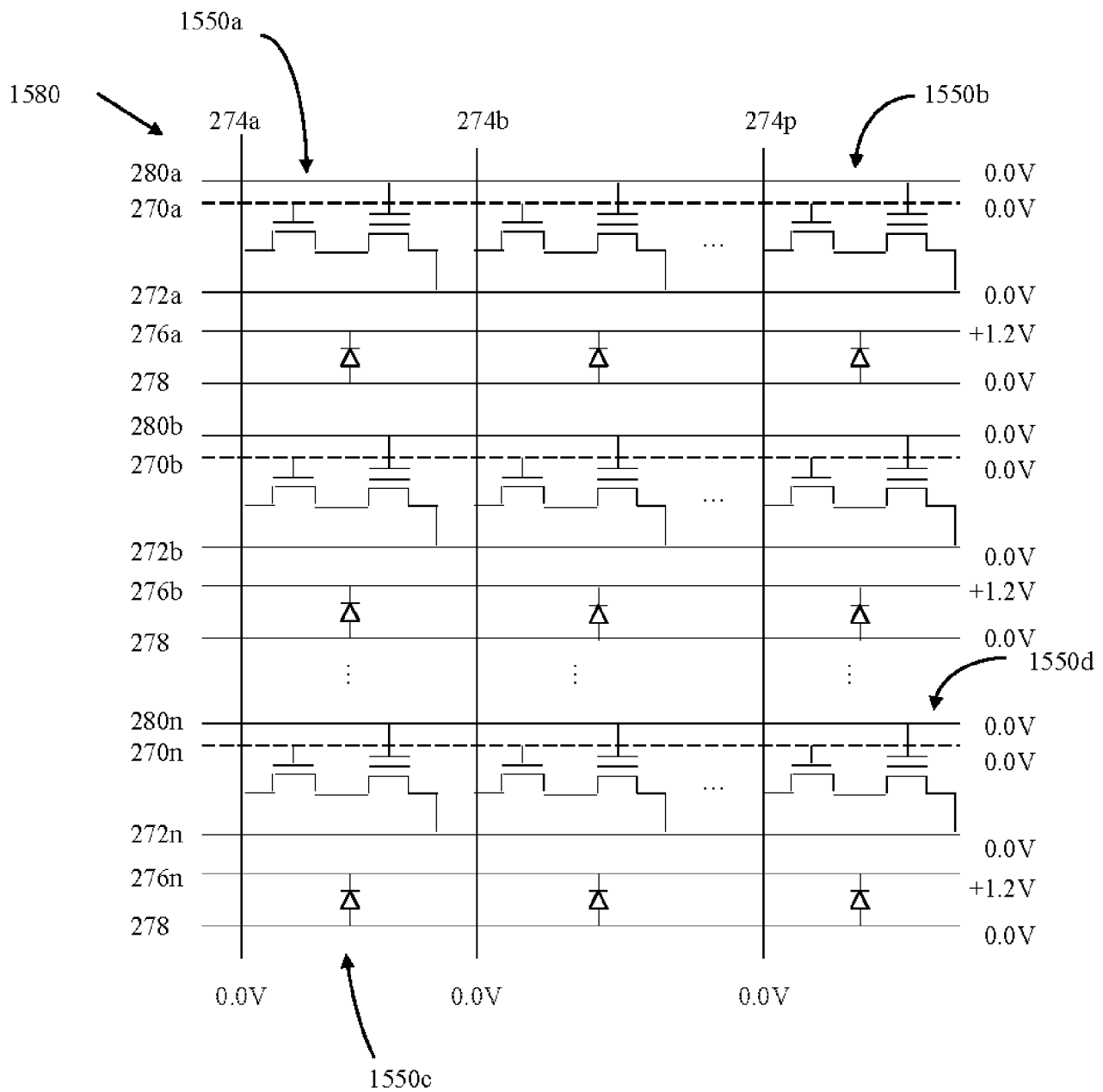


FIG. 218

Read Operation (Memory Cell 1550a)

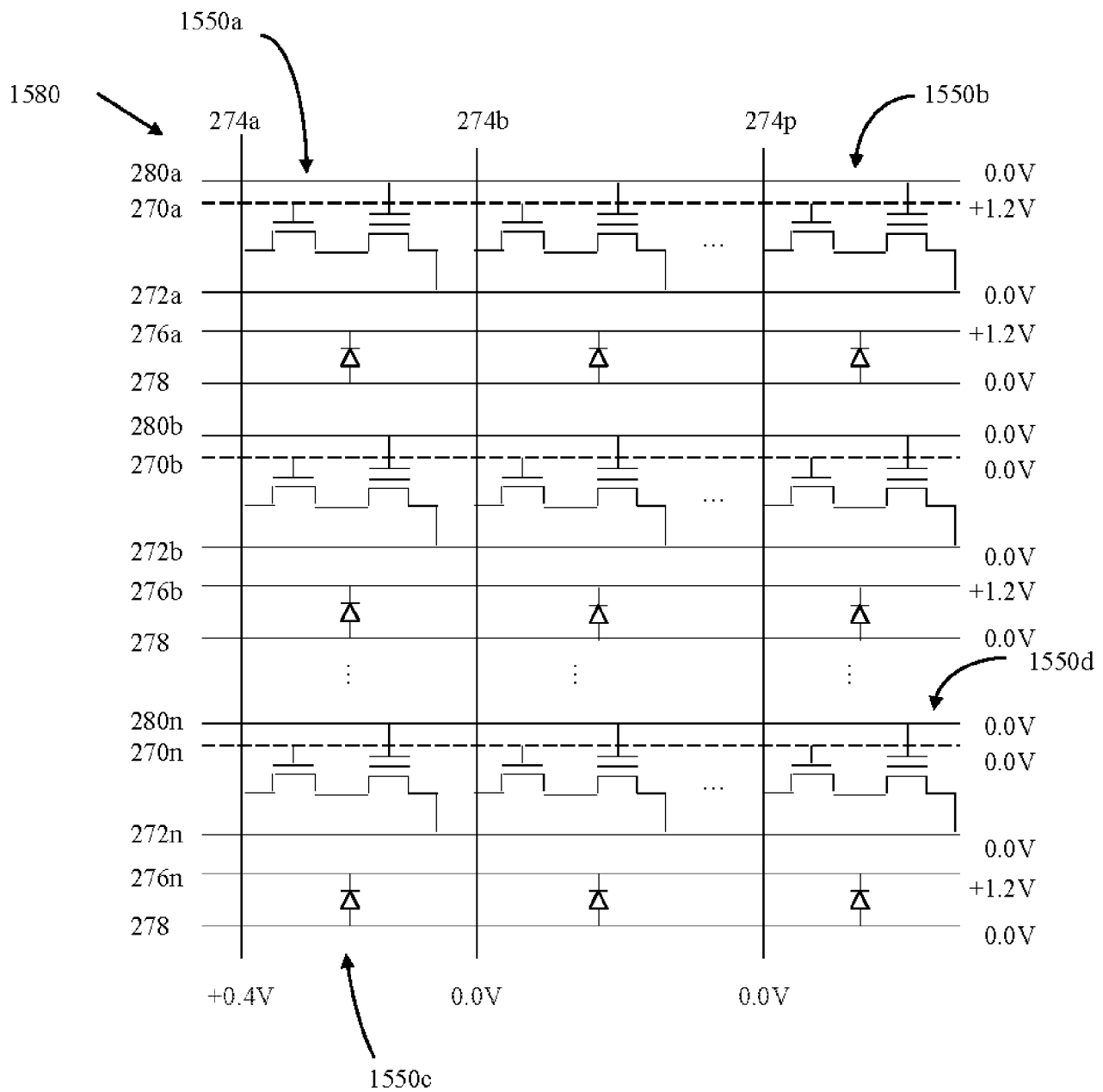


FIG. 219

Write Logic-0 Operation (Memory Cells 1550a, 1550b)

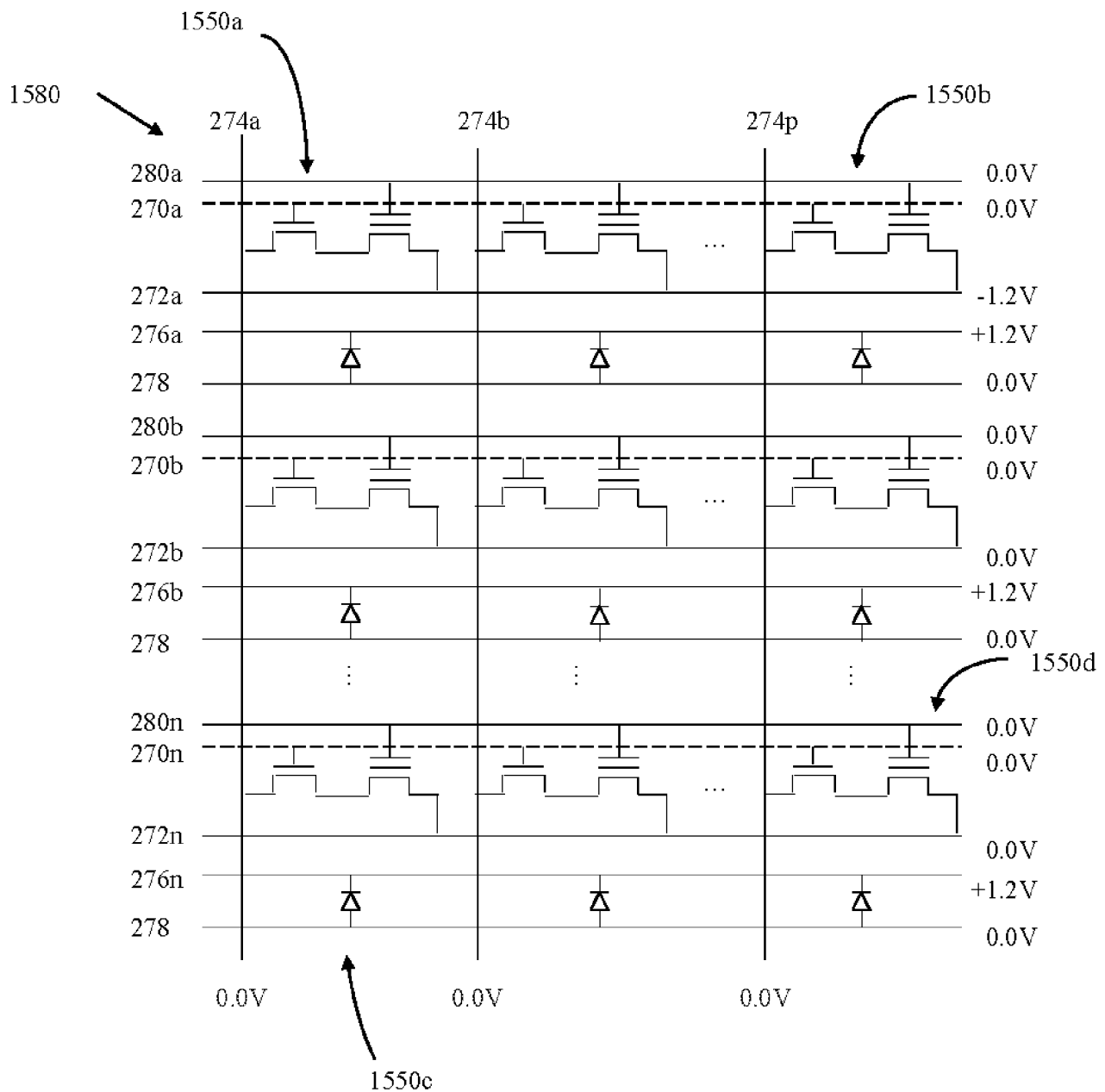


FIG. 220A

Write Logic-0 Operation (Memory Cells 1550a, 1550c)

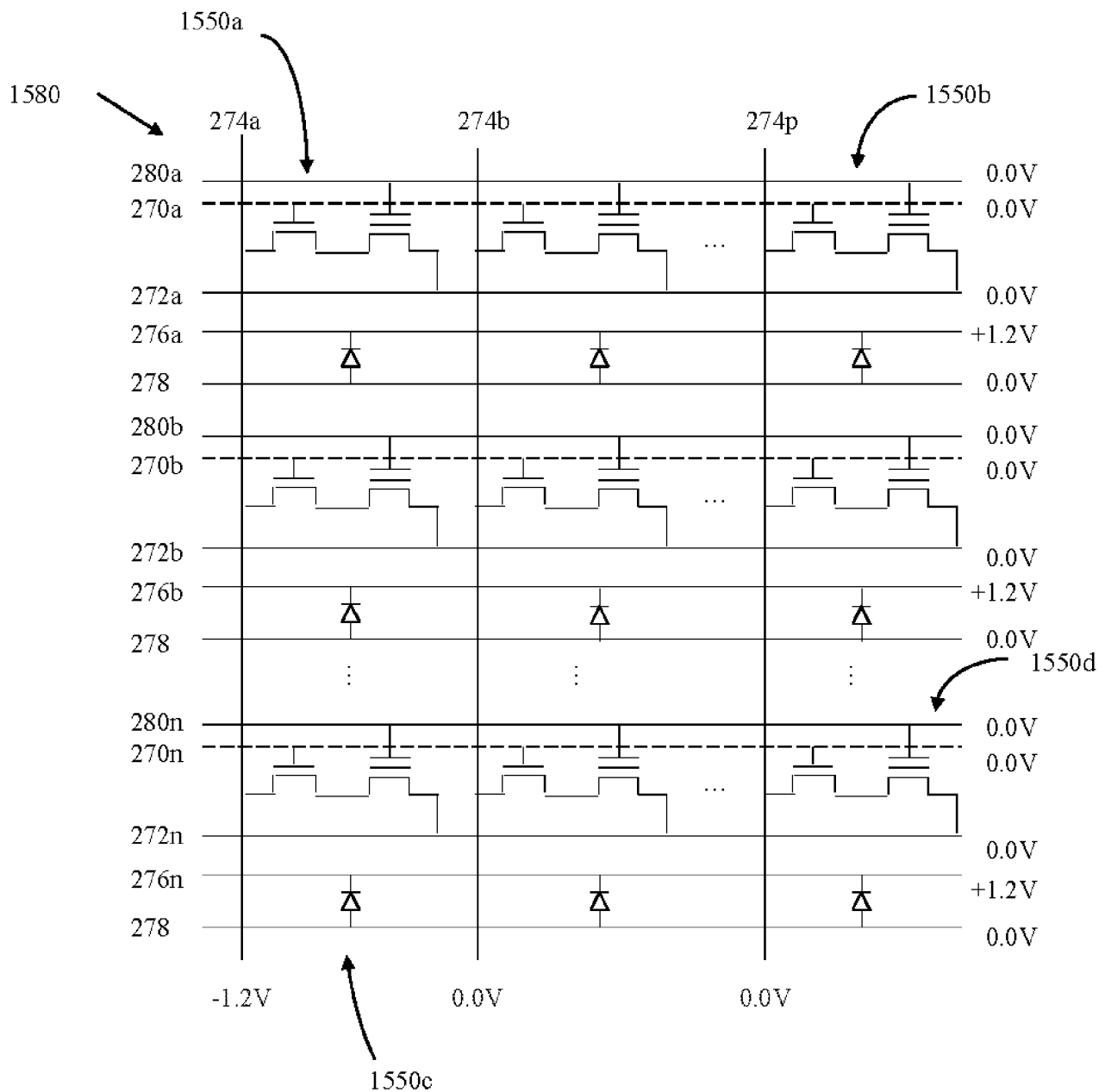


FIG. 220B

Write Logic-0 Operation (Memory Cell 1550a)

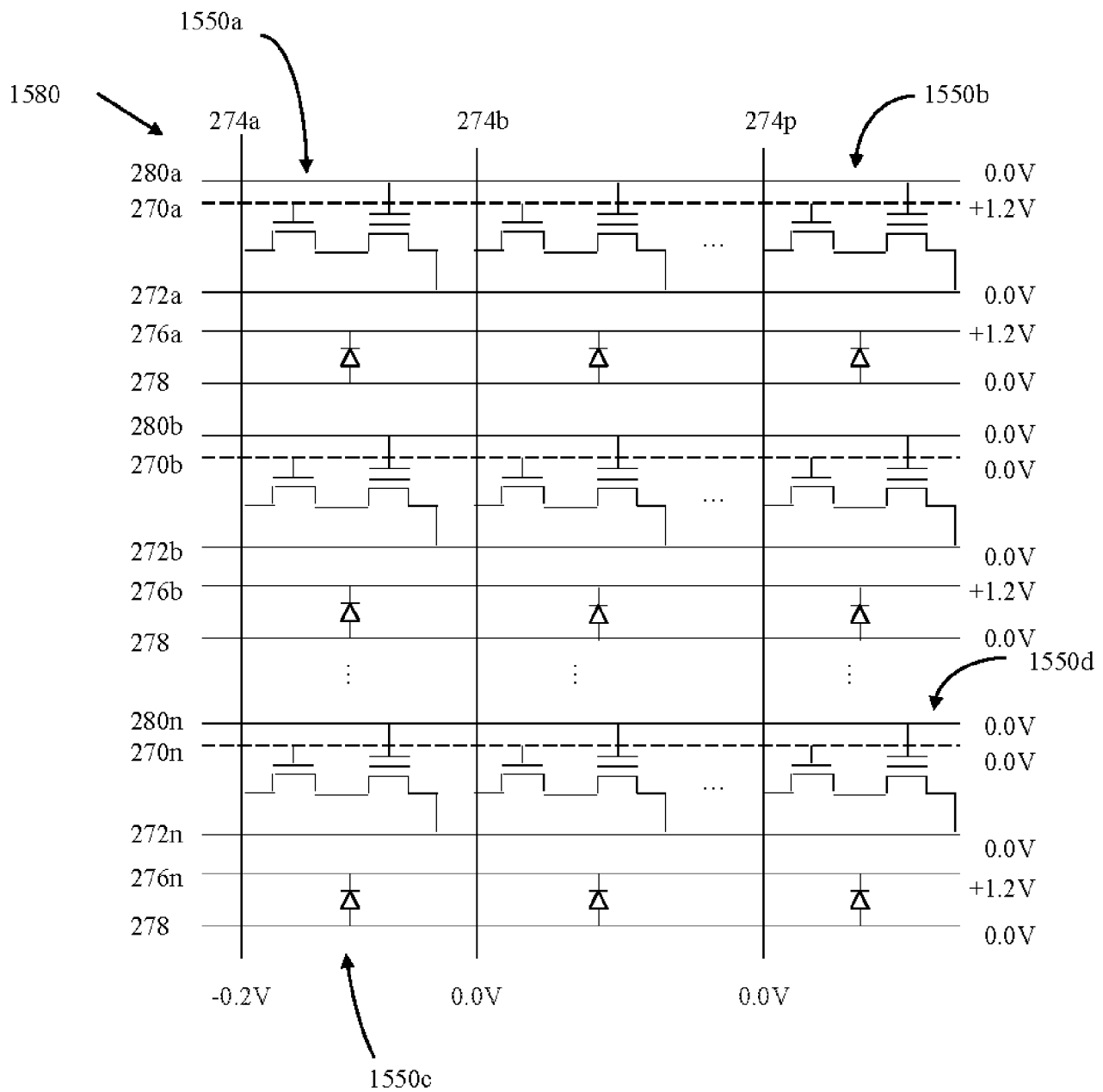


FIG. 221

Write Logic-1 Operation (Memory Cell 1550a)

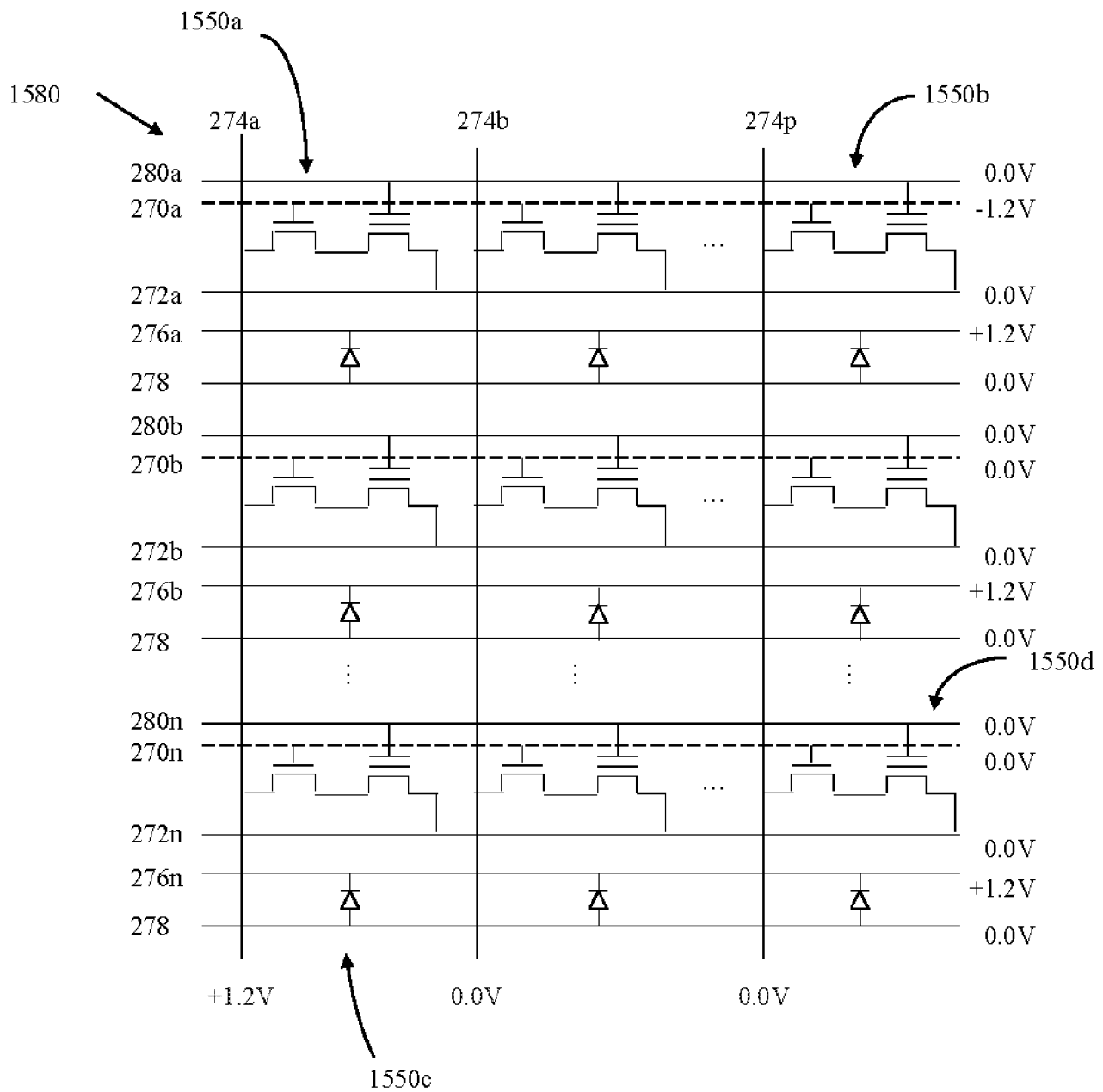


FIG. 222A

Write Logic-1 Operation (Memory Cell 1550a)

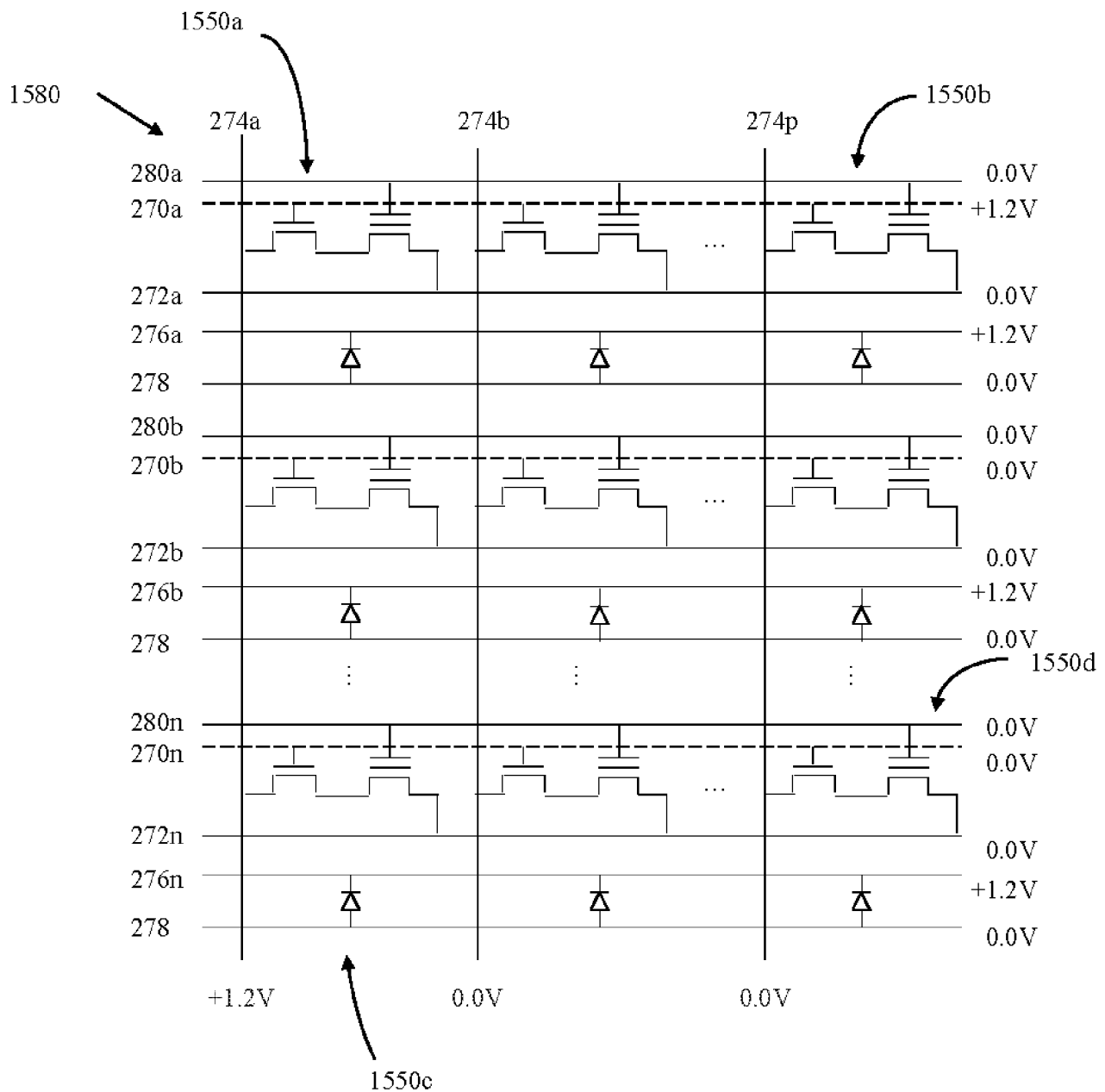


FIG. 222B

Shadowing Operation (All Memory Cells 1550)

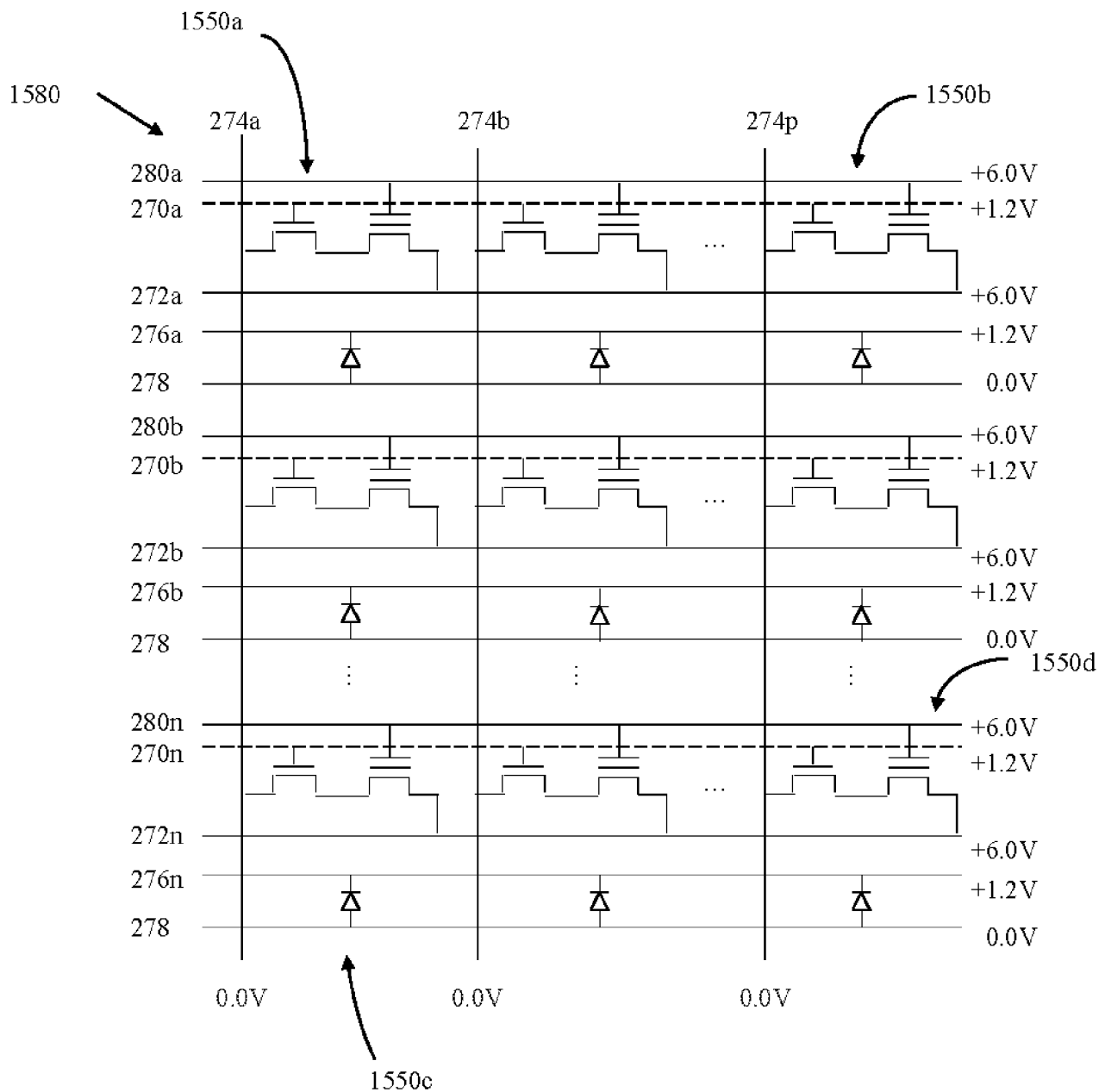


FIG. 223A

Shadowing Operation (All Memory Cells 1550)

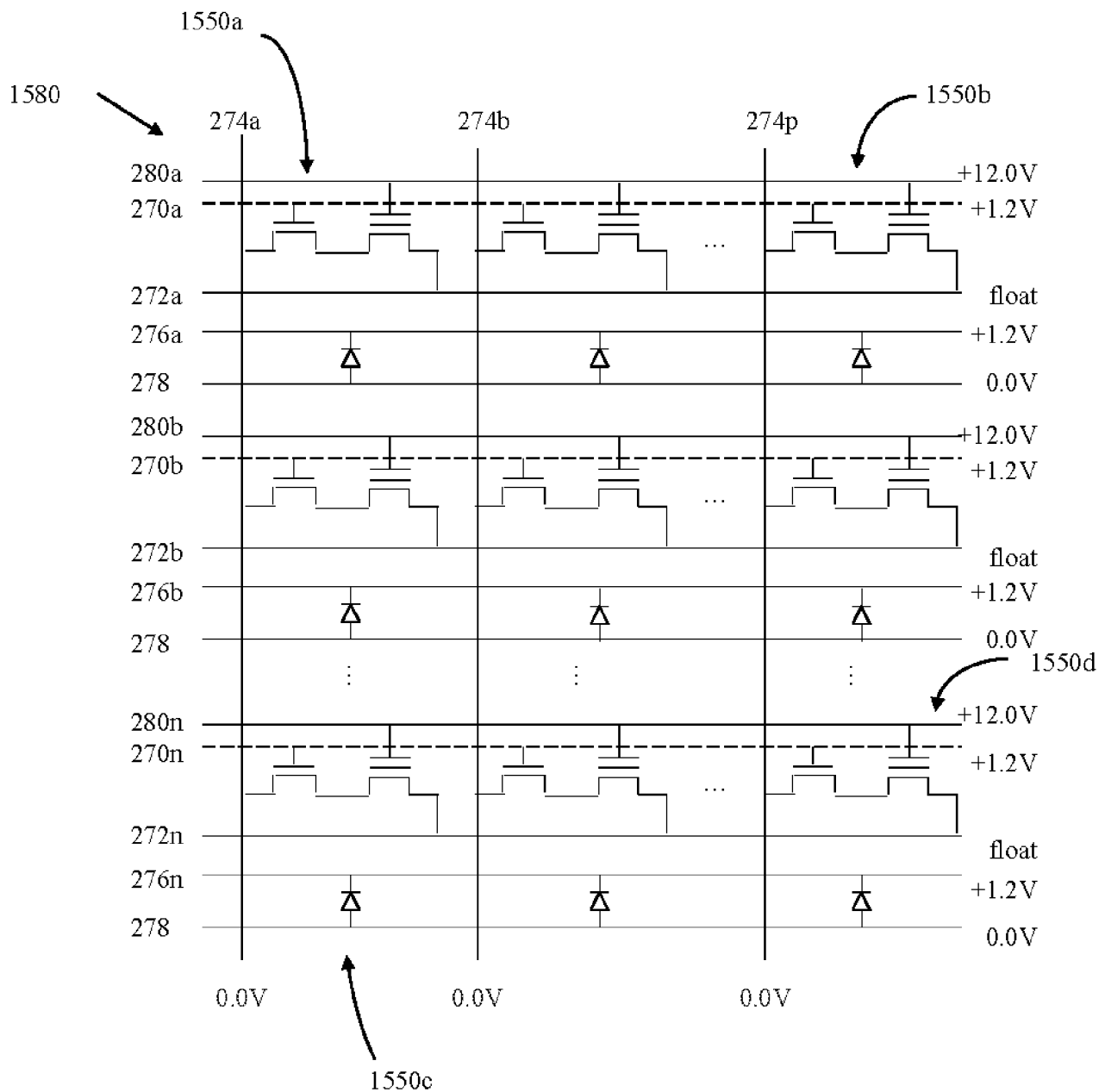


FIG. 223B

Restore Operation (All Memory Cells 1550)

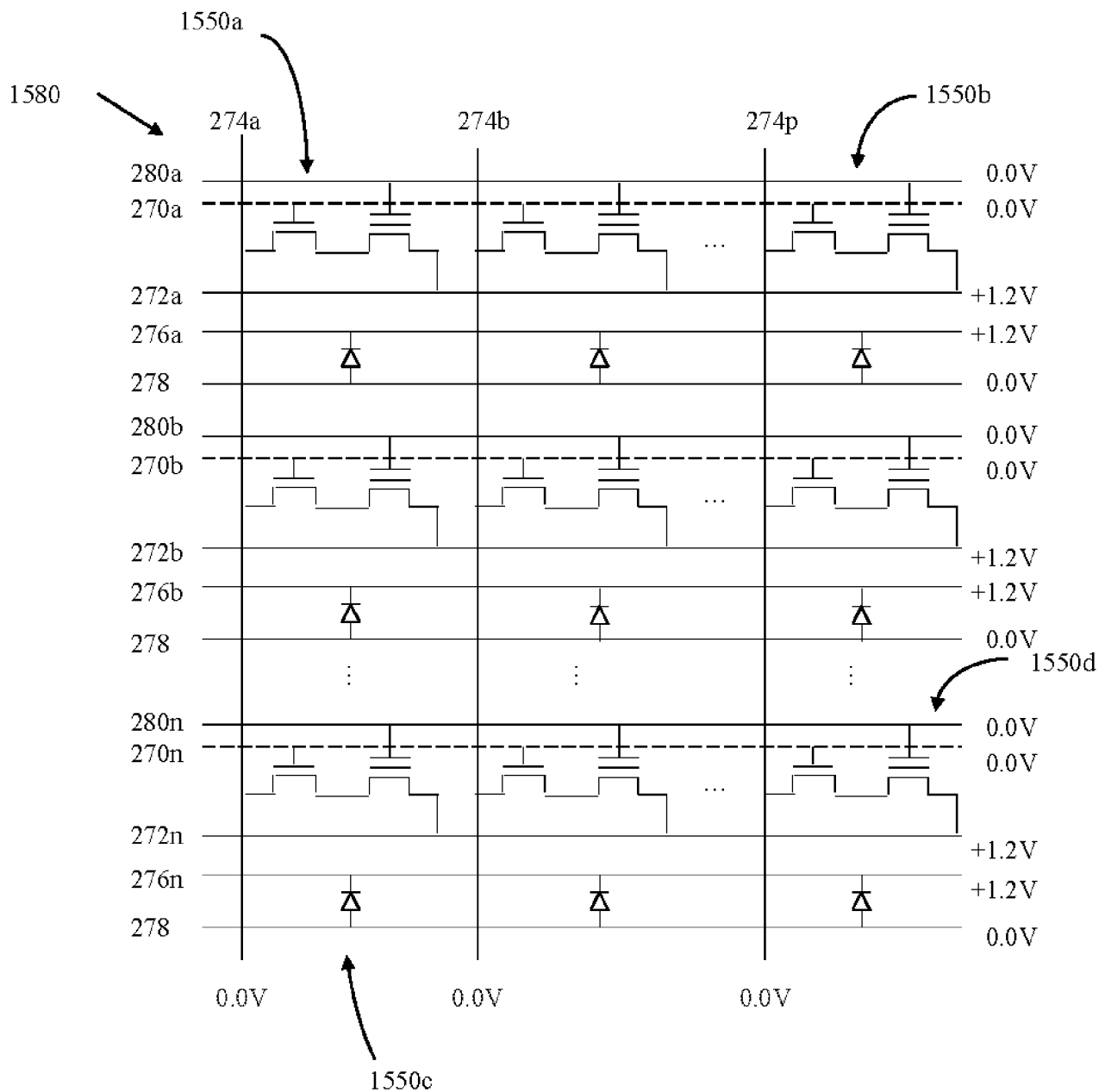


FIG. 224

Reset Operation (All Memory Cells 1550)

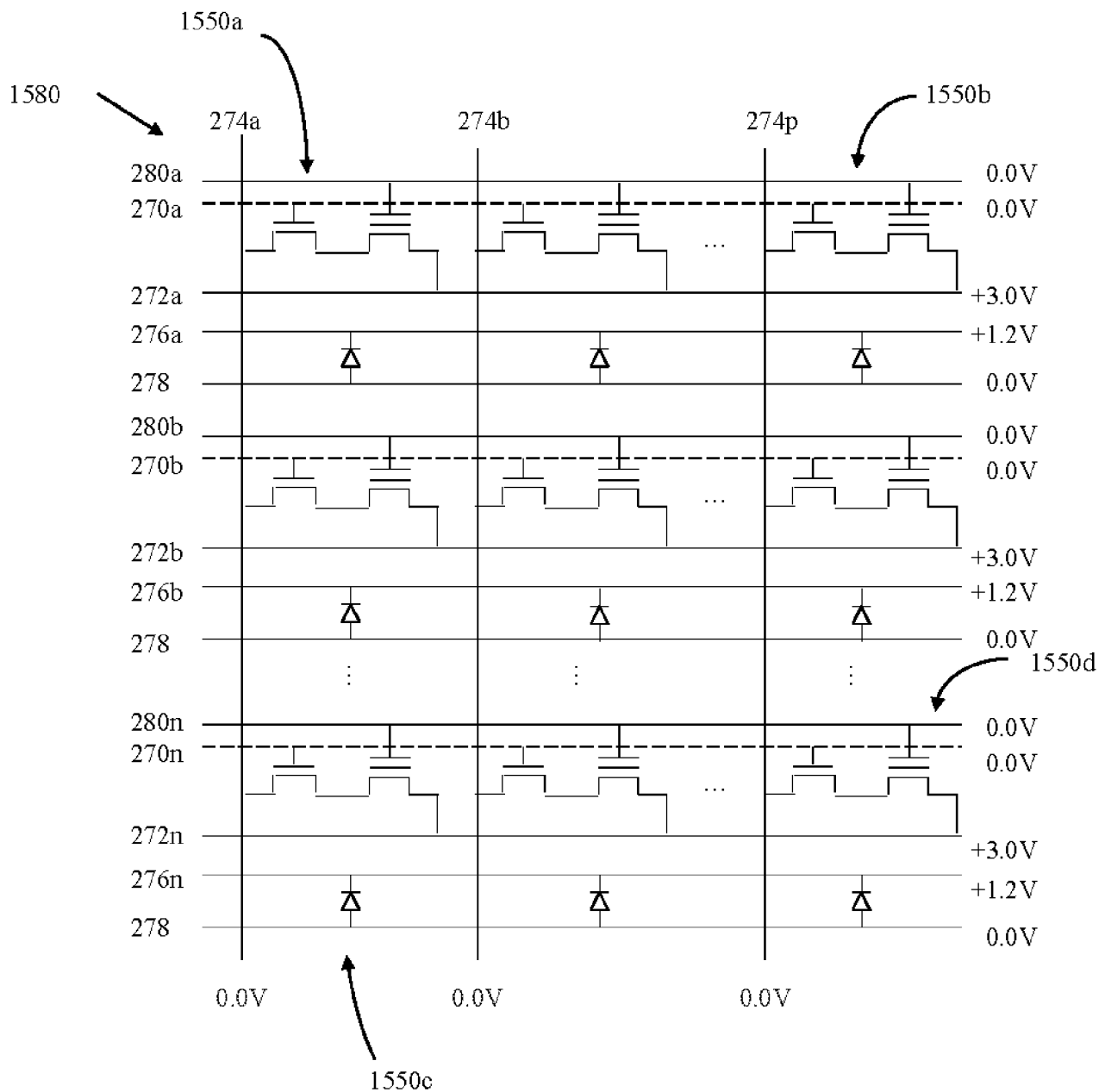


FIG. 225A

Reset Operation (All Memory Cells 1550)

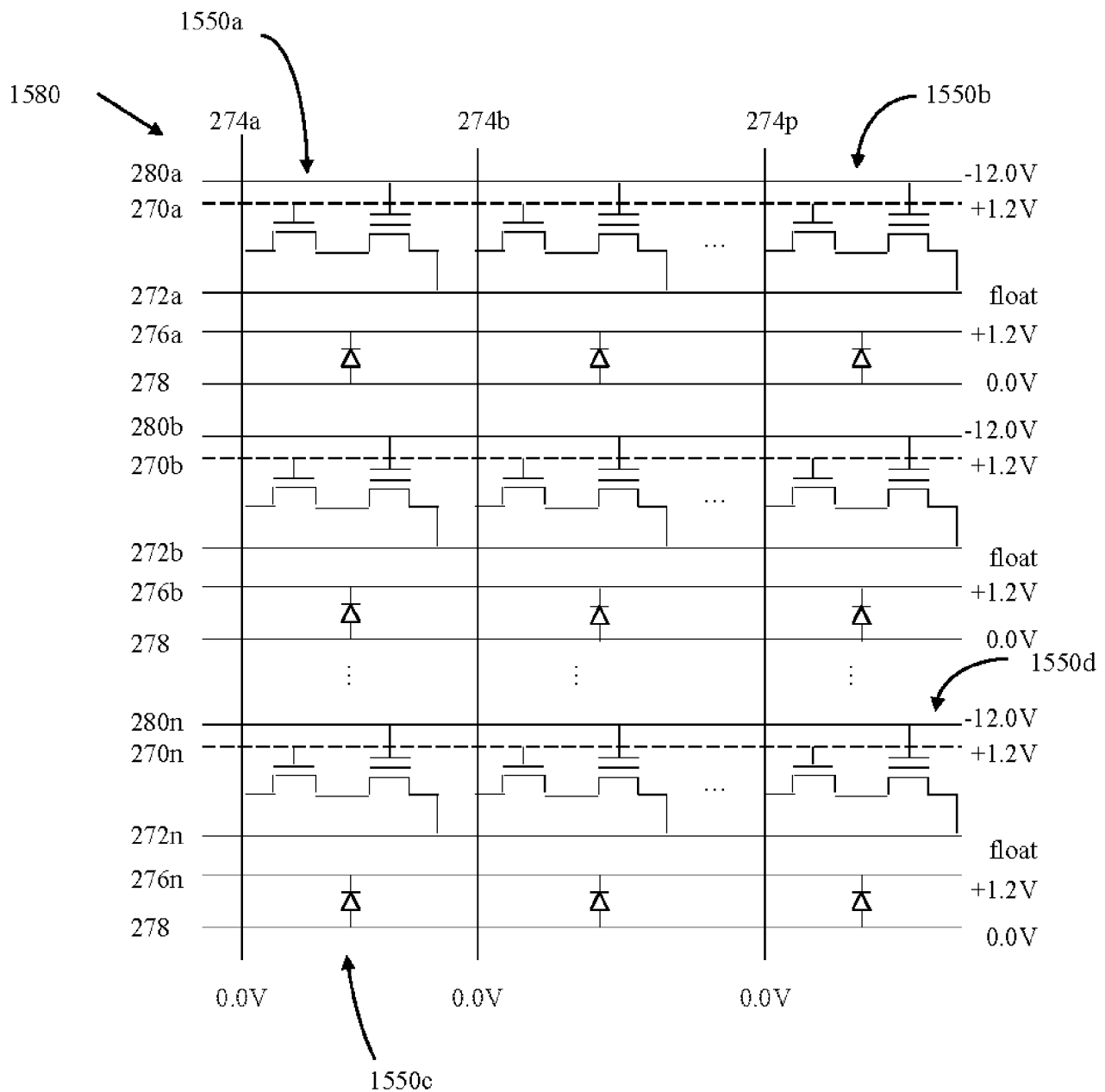


FIG. 225B

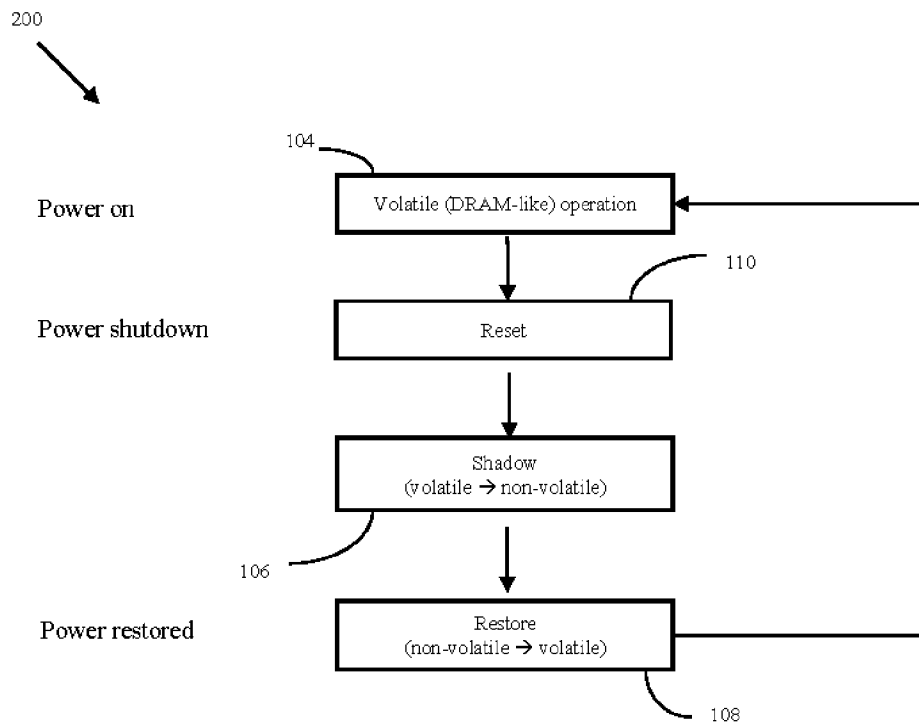


FIG. 226

Read Operation (Memory Cell 1550a)

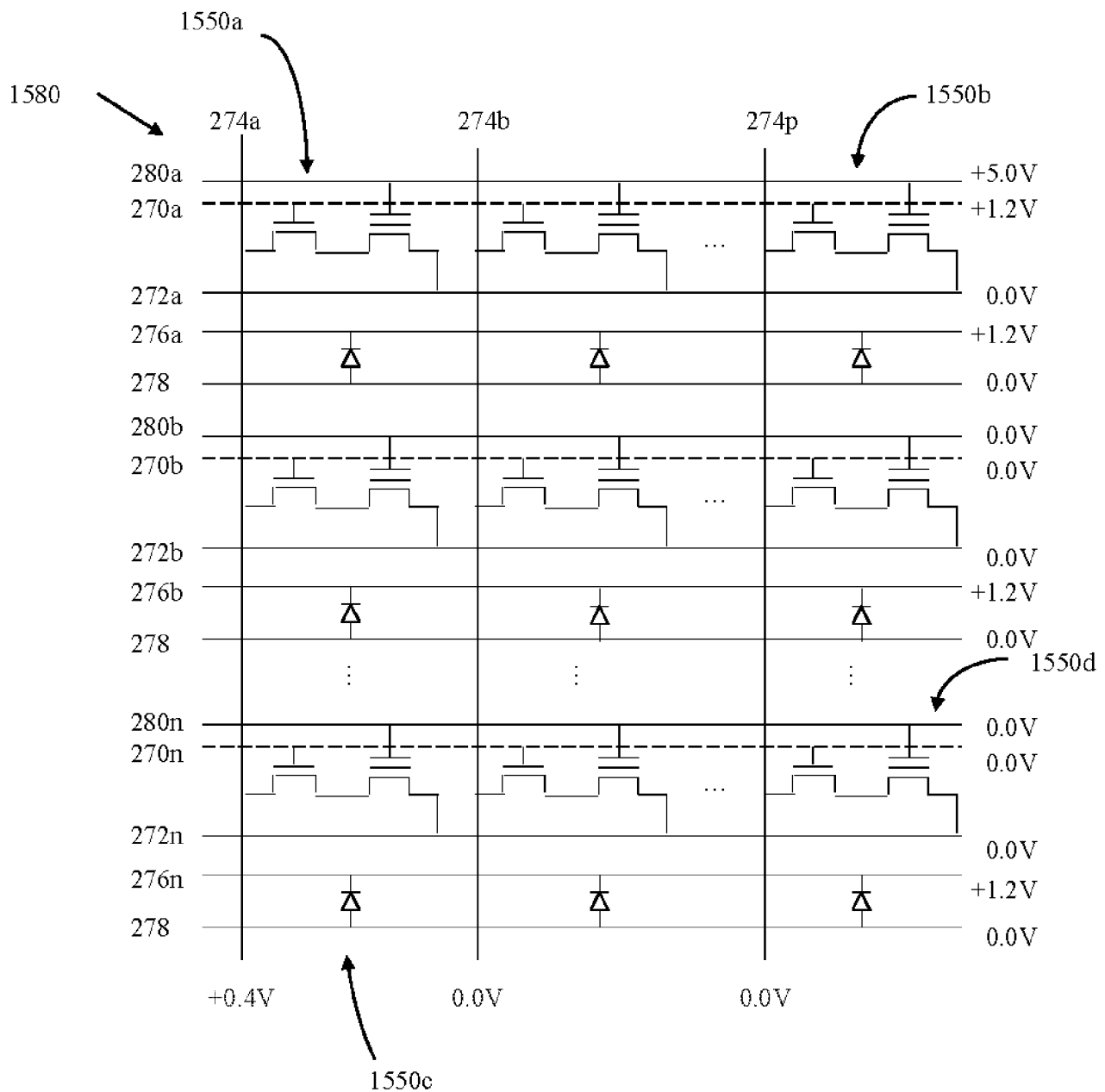


FIG. 227

Write Logic-1 Operation (Memory Cell 1550a)

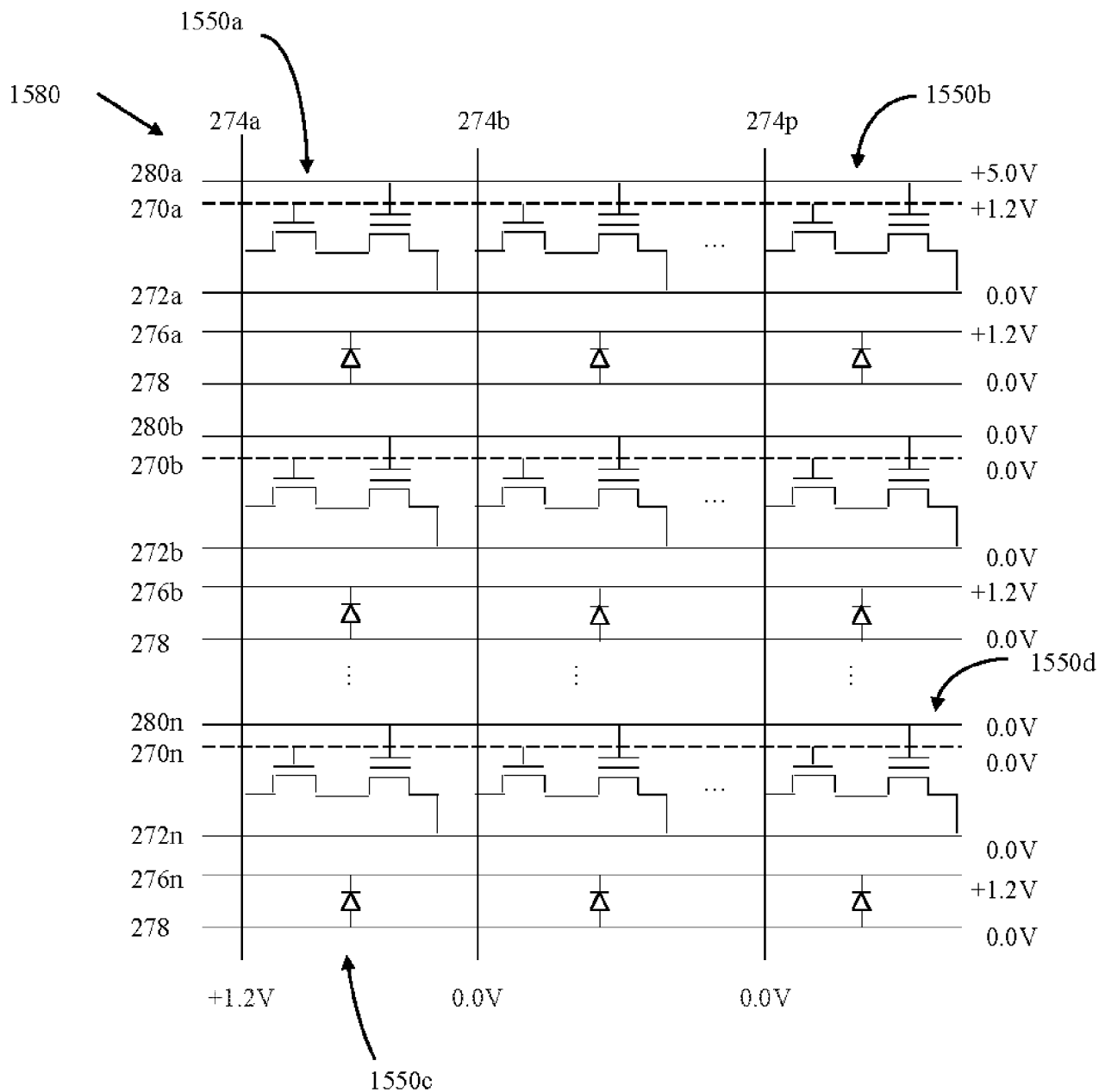


FIG. 228

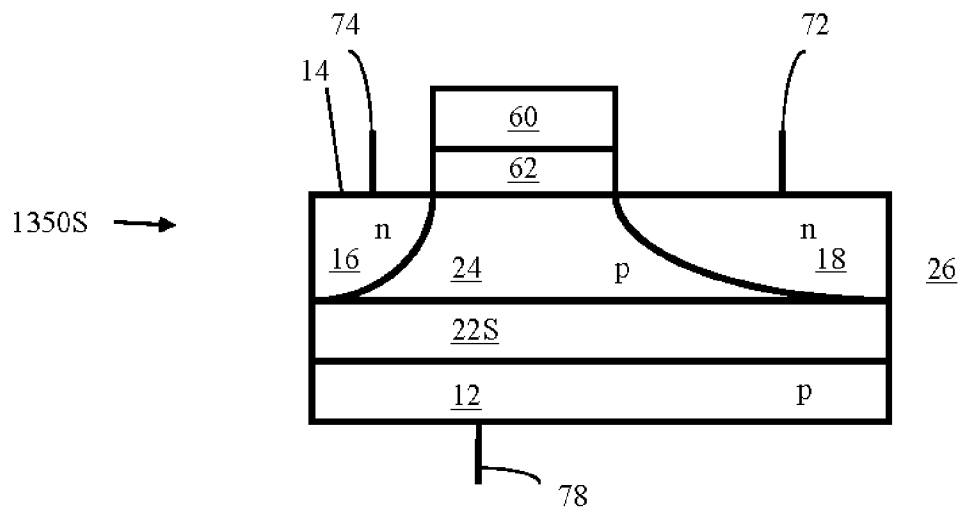


FIG. 229A

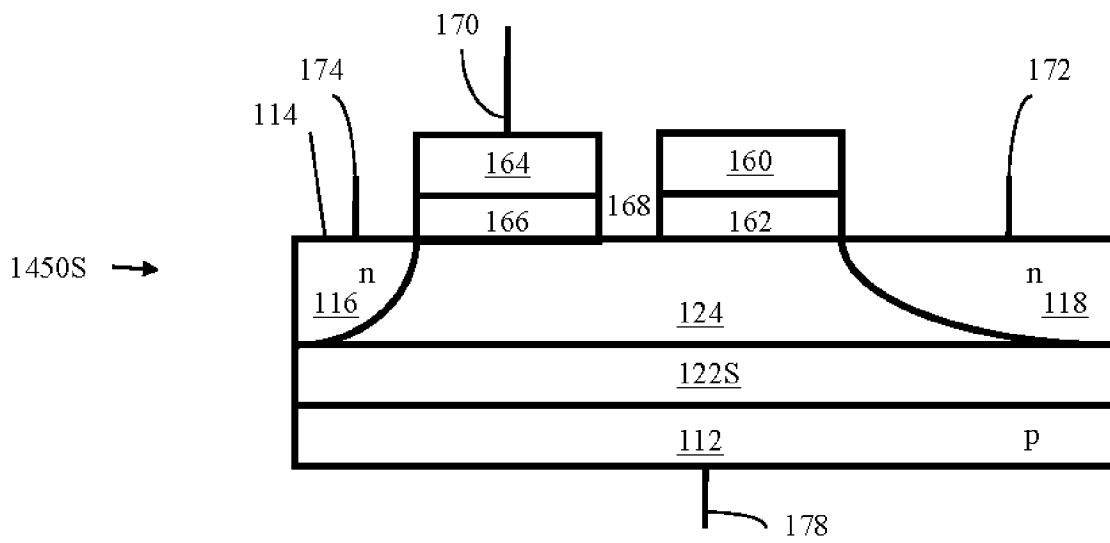


FIG. 229B

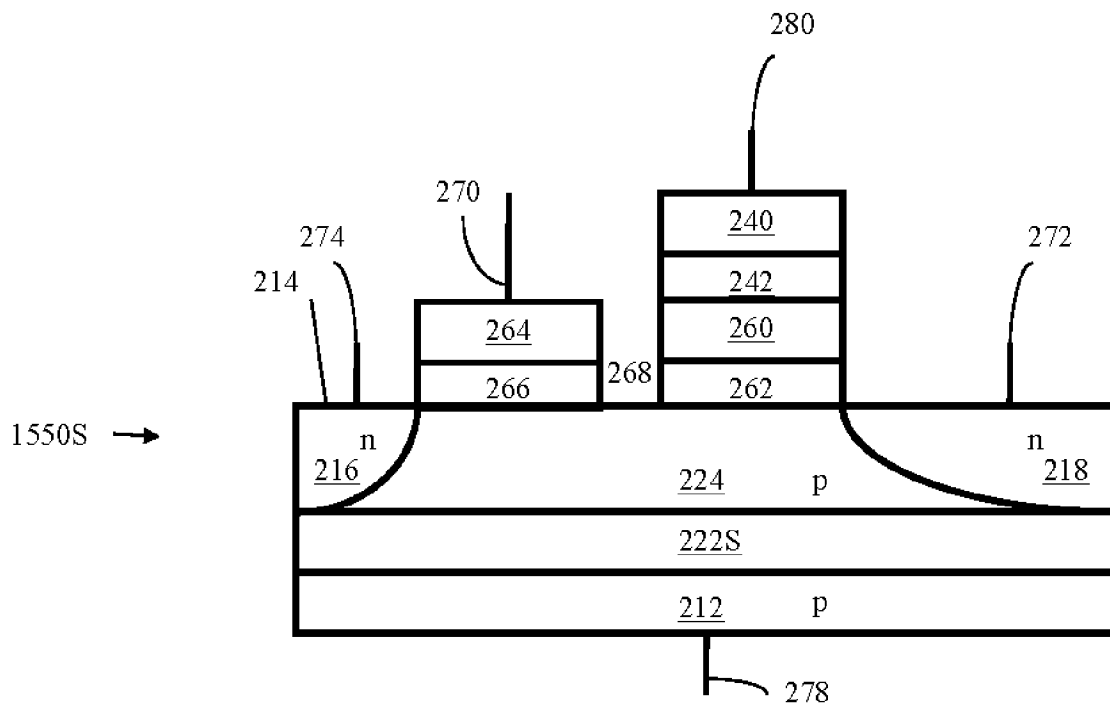


FIG. 229C

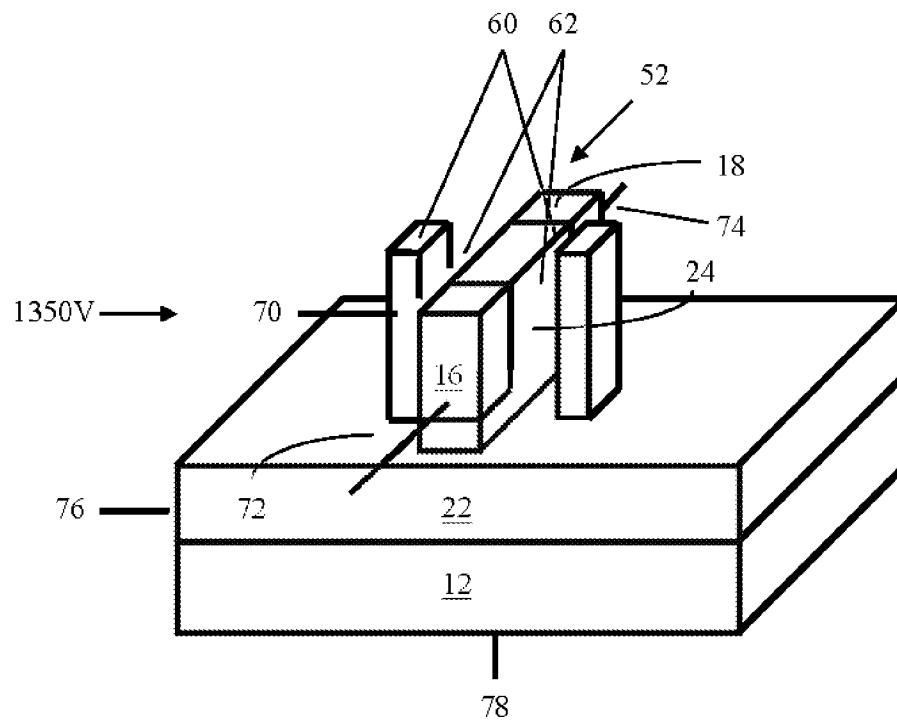


FIG. 230A

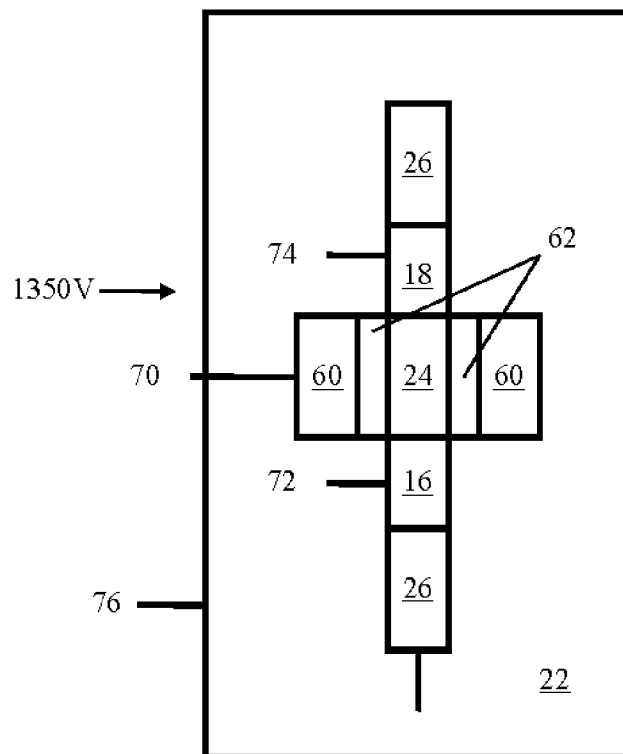


FIG. 230B

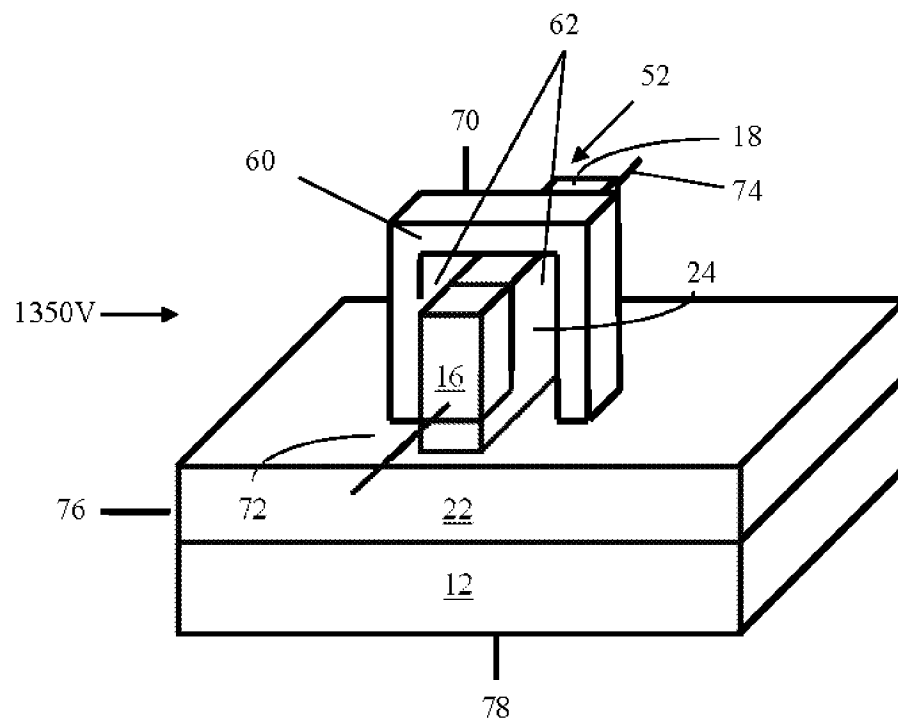


FIG. 230C

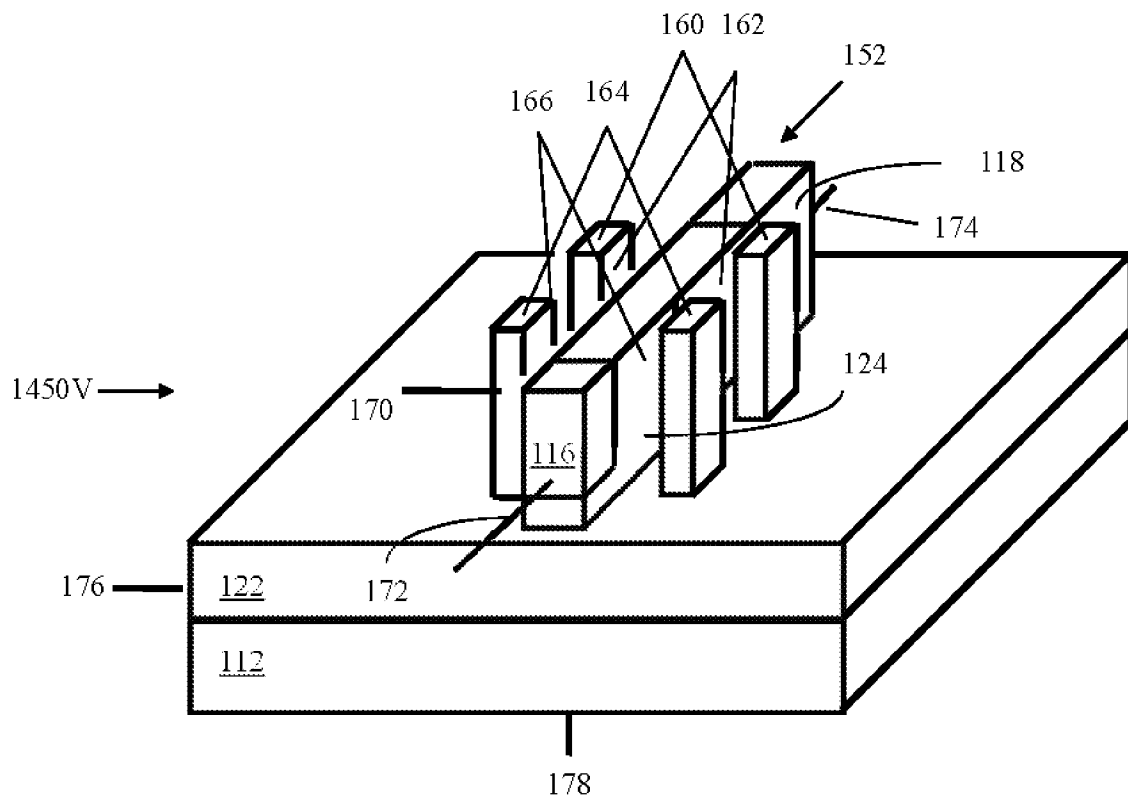


FIG. 230D

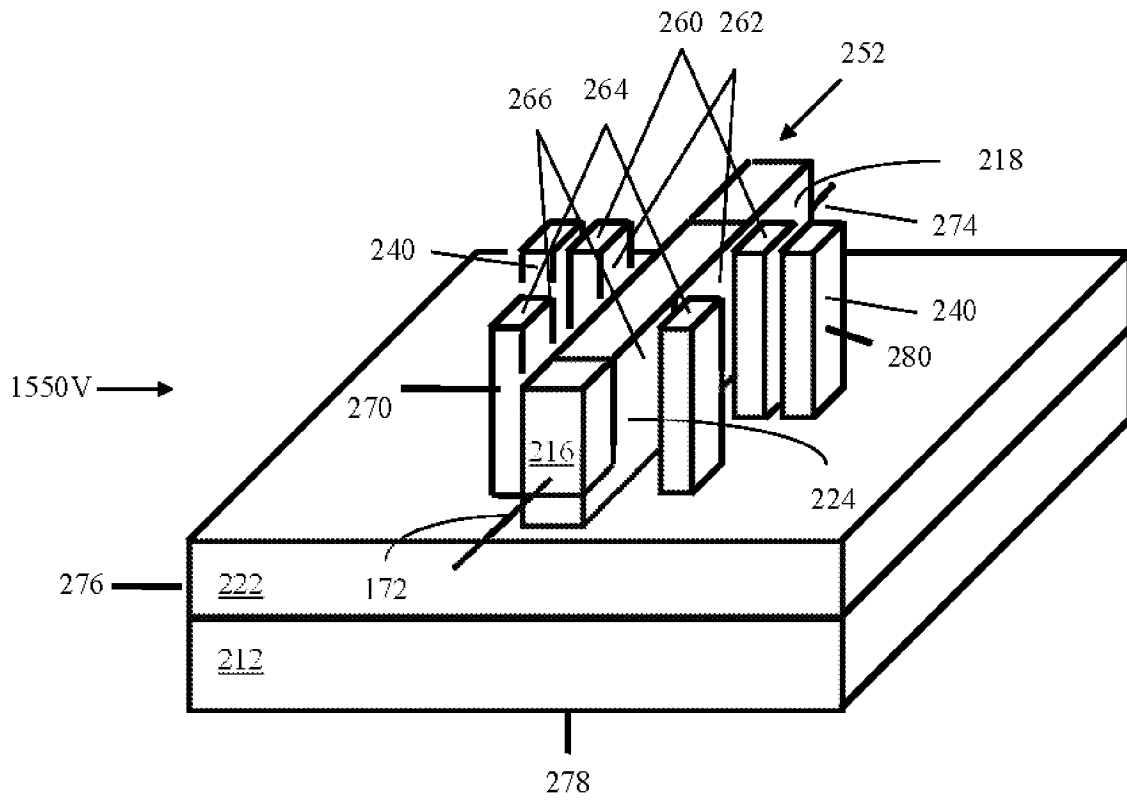


FIG. 230E