

THIN-OXIDE DEVICES FOR HIGH VOLTAGE I/O DRIVERS

CROSS REFERENCE

[0001] This Continuation-In-Part application claims the benefits of U.S. Patent Application Serial No. 10/808,122, which was filed on March 24, 2004 entitled "High Voltage CMOS Switch With Reduced High Voltage Junction Stresses."

BACKGROUND

[0002] The present invention relates generally to integrated circuit designs, and more particularly to high voltage input/output (I/O) drivers without using thick-oxide devices.

[0003] Semiconductor technology is evolving into the very deep sub-micron geometries of less than 100 nanometers (nm) to integrate more complex functionality at higher performance on a single chip. Sub-100nm devices offer more complex functionality and higher performance, but not without a cost.

[0004] It has been observed that when a transistor channel length is small enough, current continues to flow even during standby states because of leakage. Therefore, the supply voltage must be scaled down accordingly to minimize such leakage. However, the I/O voltage for conventional I/O drivers still remains at a high voltage level, such as 3.3V or 2.5V, for compatibility with existing parts. Conventionally, thick-oxide devices are usually used for I/O drivers and thin-oxide devices are used for other circuits operating with the down-scaled supply voltage. The conventional I/O drivers using thick-oxide devices require additional masks during fabrication process, thereby making the process costly and time consuming.

For example, it is typical that in order to include thick-oxide devices in semiconductor processing, four or five additional masks must be added to produce those devices. While there have been attempts to solve this issue, those attempts are either too complicated or limited for practical uses.

[0005] Desirable in the art of integrated circuit designs are designs that eliminate the need of using thick-oxide devices in high voltage I/O drivers.

SUMMARY

[0006] Disclosed herein is an input/output (I/O) driver operating as an I/O voltage. In one embodiment disclosed herein, the I/O driver includes a pull-down module and pull-up module. The pull-down module has one or more NMOS transistors serially coupled between ground and an output node. The pull-up module has one or more PMOS transistors serially coupled between a first voltage and the output node. The gates of the PMOS and NMOS transistors can be controlled by a set of differential biases for selectively pulling the output node to the first voltage or ground. The differential biases are separately set for each of the transistors so that a voltage difference across each of the transistors does not exceed a predetermined value, thereby preventing the same from damage.

[0006a] In one aspect, there is provided an input/output (I/O) circuit for outputting an output signal of a first voltage in response to an input signal of a second voltage lower than the first voltage, comprising: a pull-down module having one or more NMOS transistors serially coupled between ground and an output node; a pull-up module having one or more PMOS transistors serially coupled between an I/O voltage and the output node; and a level shifter responsive to the input signal for generating a set of differential biases selectively enabling or disabling the pull-down and pull-up models to pull the output node to the I/O voltage or ground, wherein the differential biases are separately set for each of the PMOS transistors so that a voltage difference across each of the PMOS transistors does not exceed a predetermined value, thereby preventing the same from damage, wherein the level shifter further comprises: a first PMOS transistor coupled to the I/O voltage; a first group of one or more voltage dropping PMOS transistors each of which has its gate connected to its drain, serially coupled to a drain of the first PMOS transistor; a first NMOS transistor serially coupled between the first group of the voltage dropping PMOS transistors and ground, having a gate controlled by the input signal; a second PMOS transistor coupled to the I/O voltage in parallel to the first PMOS transistor,

wherein the gate of the second PMOS transistor is coupled to the drain of the first PMOS transistor, and the gate of the first PMOS transistor is coupled to the drain of the second PMOS transistor; a second group of one or more voltage dropping PMOS transistors each of which has its gate connected to its drain, serially coupled to a drain of the second PMOS transistor; and a second NMOS transistor serially coupled between the second group of voltage dropping PMOS transistors and ground, having a gate controlled by a complement of the input signal, wherein the drains of the first and second PMOS transistors and the first and second groups of the voltage dropping PMOS transistors provide the differential biases.

[0006b] In another aspect, there is provided an input/output I/O circuit for outputting an output signal of a first voltage in response to an input signal of a second voltage lower than the first voltage, comprising : a pull-down module having one or more NMOS transistors serially coupled between ground and an output node; a pull-up module having one or more PMOS transistors serially coupled between an I/O voltage and the output node; and a level shifter responsive to the input signal for generating a set of differential biases selectively enabling or disabling the pull-down and pull-up models to pull the output node to the I/O voltage or ground, wherein the differential biases are separately set for each of the PMOS transistors so that a voltage difference across each of the PMOS transistors does not exceed a predetermined value, thereby preventing the same from damage, wherein the level shifter further comprises: a first PMOS transistor coupled to the I/O voltage; a first group of one or more capacitors serially coupled to a drain of the first PMOS transistor for receiving the input signal; a second PMOS transistor coupled to the I/O voltage in parallel to the first PMOS transistor, wherein the gate of the second PMOS transistor is coupled to the drain of the first PMOS transistor and the gate of the first PMOS transistor is coupled to the drain of the second PMOS transistor; and a second group of one or more capacitors serially coupled to a drain of the second PMOS transistor for receiving a complement of the input signal wherein the drains of the first and second PMOS transistors provide the differential biases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIGs. 1A to 1C illustrate three I/O drivers with thin-oxide devices in accordance with one embodiment of the present invention.

[0008] FIGs. 2A and 2B illustrate two level shifters in accordance with another embodiment of the present invention.

[0009] FIG. 3 illustrates a circuit with an I/O driver controlled by a set of differential biases generated by a level shifter in accordance with another embodiment of the present invention.

DESCRIPTION

[0010] FIG. 1A illustrates an I/O driver 100 with thin-oxide devices in accordance with one embodiment of the present invention. The I/O driver 100 is shown to be implemented with only thin-oxide devices. Thin-oxide PMOS transistors 102 and 104 are serially placed in a stack formation along with thin-oxide NMOS transistors 106 and 108 between an I/O power supply having an I/O voltage (VDDI) and ground. The transistors 106 and 108 collectively function as a pull-down module to pull the voltage at the output node 110 low. The transistors 102 and 104 collectively function as a pull-up module to pull the voltage at the output node 110 high. The I/O voltage (VDDI) is higher than a core voltage VDDC used for operation of a core circuitry (not shown in this figure). Proper differential biases are applied to the gates of the transistors to sustain the higher I/O voltage. These differential biases can be a fixed bias such as the core voltage VDDC, or a swing bias switching between a first voltage value and a second voltage value, depending on the needs of the driver's designs. If the swing bias switches with the same polarity as the output signal of the I/O driver, when the value of the output signal switches from zero to one, the swing bias switches from the low voltage value to the high voltage value. If the swing bias switches with the reversed polarity as the output signal of the I/O driver, when the value of the output signal switches from zero to one, the swing bias switches from the high voltage value to the low voltage value. Properly controlling the transistors with the various differential biases can make sure that a voltage difference across each of the PMOS transistors 102 and 104 does not exceed a predetermined value, which is set to keep the transistors operating

normally without burning out due to an excessive voltage. This prevents the PMOS transistors 102 and 104 from damage which would have resulted from a high voltage difference thereacross due to the high I/O voltage VDDI.

[0011] The transistors 102 and 108 are configured as switches. Both gates of the transistors 104 and 106 are clamped to core voltage VDDC. The gate of transistor 108 is driven by a swing bias switching between 0V and the core voltage VDDC. The gate of transistor 102 is biased by a swing bias switching between the I/O voltage VDDI at the high end and the core voltage VDDC at the low end. When output at the output node 110 is to be logic 0, the I/O voltage VDDI is applied to the gate of transistor 102 for complete cutoff. When the output at the output node 110 is to be logic 1, the gate of the transistor 102 will be biased to $VDDI - |V_{tp}|$ with a proper margin, where $|V_{tp}|$ is the absolute threshold voltage value of the transistor 102. This turns on the transistor 102, and pulls the output node 110 high. With such proper biasing, the voltage drops across the transistors 102 and 104 would not exceed a predetermined value, thereby preventing the same from damage.

[0012] For example, in a design where the core voltage VDDC is 1.0V and the I/O voltage is 1.8V, the transistors 104 and 106 will be clamped by the core voltage VDDC of 1.0V. The gate of the transistor 102 will be biased to 1.8V when the output needs to be a logic 0. Assuming the threshold voltage of the transistor 102 is 0.4V, when the output needs to be a logic 1, the gate of the transistor 102 is biased to a voltage lower than 1.4V, such as 1.3V. With a proper bias applied to the gate of the transistor 102, only a fraction of the I/O voltage 1.8V will reach the source of the transistor 104. By controlling the bias, the voltage difference across the transistor 102 can be controlled under a predetermined value, thereby preventing the same from damage. Likewise, the voltage difference across the transistor 104 can be controlled under a predetermined value, thereby preventing the same from damage.

Since both the transistors 102 and 104 are biased properly, high I/O voltage VDDI of 1.8V can be generated from the output node 110.

[0013] FIG. 1B illustrates an I/O driver 112 with thin-oxide devices in accordance with one embodiment of the present invention. Thin-oxide PMOS transistors 114, 116, and 118 are serially placed in a stack formation along with thin-oxide NMOS transistors 120, 122, and 124 between the I/O power supply having the I/O voltage VDDI and ground. The transistors 120, 122 and 124 collectively function as a pull-down module to pull the voltage at the output node 126 low. The transistors 114, 116 and 118 collectively function as a pull-up module to pull the voltage at the output node 126 high. Since there are more transistors placed in cascade formation in the I/O driver 112 than in the I/O driver 100, I/O voltage can be even higher. In other words, the number of the PMOS transistors in the pull-up module increases when the value of the I/O voltage increases. For example, if the I/O driver 100 can handle a high voltage of 1.8V, the I/O driver 112 will be able to handle an even higher voltage such as 2.5V. Proper differential biases are applied to the gates of each transistor to sustain the high I/O voltage. These gate voltages can be a fixed bias such as the core voltage VDDC, a swing bias switching with the same polarity as the output signal at the output node 126, or a swing bias switching with the reverse polarity as the output signal, depending on the needs of the driver's designs. The selective application of the three kinds of biases can be used to clamp the thin-oxide transistors within a safe operation region.

[0014] The transistors 114, 116, 118, and 124 are configured as switches. The I/O driver 112 functions similarly to the I/O driver 100, because both accept input and provide output in a higher voltage. As an example of the embodiment, when the output node 126 outputs the I/O voltage, the bias applied to the gate of the transistor 114 is set proximately equal to $V_d + 3 |V_{tp}|$, where V_d is a voltage drop

across the transistor 114 and $|V_{tp}|$ is the threshold voltage of the same. The biases applied to the gates of the transistors 116 and 118 are set proximately equal to $V_{DDI} - V_d - |V_{tp}|$. When the output node 126 outputs 0V, the bias applied to the gate of the transistor 114 is set proximately equal to V_{DDI} , the bias applied to the gate of the transistor 116 is set proximately equal to $V_{DDI} - V_d - |V_{tp}|$, and the bias applied to the gate of the transistor 118 is set proximately equal to $2|V_{tp}|$.

[0015] For example, in a design where the core voltage V_{DDC} is 1.0V, the I/O voltage is 2.5V, the voltage drop across the transistor 114 is 0.7V, and the threshold voltage of the same is 0.4V, the devices within the I/O driver 112 are biased by a set of differential biases. The gate of the transistor 114 can be biased to 2.5V when output needs to be logic 0, and 1.9V when output is to be a logic 1. When the output is to be a logic 0, with the bias of the transistor 114 and a voltage drop thereacross, only 1.8V will reach the source of the transistor 116, thereby preventing the transistor 114 from damage. The transistor 116 is biased to 1.4V whether the output is a logic 0 or 1. After another voltage drop, only 1.2V can reach the source of the transistor 118, thereby preventing the transistor 116 from damage. The gate of the transistor 118 is biased to 0.8V when output needs to be logic 0 and 1.4V when output is to be a logic 1. With the transistors 114, 116, and 118 biased properly the voltage differences across the PMOS transistors are controlled within a safe range. To avoid high voltage damage, the transistors in the pull-down module of the I/O driver 112 are also properly biased according to the values of the output signals.

[0016] FIG. 1C illustrates an I/O driver 128 with thin-oxide devices in accordance with another embodiment of the present invention. Thin-oxide PMOS transistors 130, 132, and 134 are placed in a pull-up module, while a NMOS transistor 136 in series with another NMOS transistor 138 are placed in a pull-down module. This configuration allows the drain of the transistor 136 to be able to sustain a higher

voltage so that the source can be clamped at a lower voltage. The backgate bias of the transistor 136 can be set to be very low such that this device does not need to be on a separate P-well. With this high voltage device implemented, it allows the PMOS transistors to be used in the pull-up module without an additional NMOS transistor in the pull-down module as shown in FIG. 1B.

[0017] The PMOS transistors used in the I/O drivers as shown in FIGs. 1A through 1C are controlled by the differential biases so that the voltage difference across each transistor would not exceed a predetermined value. This allows the transistor to be made of thin-oxide layers, without damage caused by the high I/O voltage.

[0018] FIG. 2A illustrates a level shifter 200 for generating the differential biases in accordance with one embodiment of the present invention. The level shifter 200 can generate the differential biases for proper clamping of the transistors within the I/O drivers 100, 112, and 128 as shown in FIGs. 1A through 1C. A PMOS transistor 202 coupled to an I/O power supply having the I/O voltage VDDI. One or more voltage dropping PMOS transistors 206, 210 and 214, each of which having its gate connected to its drain, are serially coupled to the drain of the transistor 202. An NMOS transistor, having a gate controlled by an input signal D, is serially coupled between the transistor 214 and ground. A PMOS transistor 204 is coupled to the I/O power supply in parallel to the transistor 202. The gate of the transistor 204 is coupled to the drain of the transistor 202, and the gate of the transistor 202 is coupled to the drain of the transistor 204. One or more voltage dropping PMOS transistors 208, 212 and 216, each of which having its gate connected to its drain, are serially coupled to the drain of the transistor 204. An NMOS transistor is serially coupled between the transistor 216 and ground, having a gate controlled by a complementary input signal DB.

[0019] The PMOS transistors 202 and 204 form a cross-coupled structure that can latch data when input signals D and DB are switching. It is understood that the complementary input signal DB is the inverse of the input signal D. The PMOS transistors 206, 210, and 214 are arranged in a diode configuration, while the PMOS transistors 208, 212, and 216 are arranged in another diode configuration to provide multiple voltage drops. It is understood that at nodes 218 and 220, two leakers can help prevent voltages from dropping to ground when either the transistor 202 or 204 is cut off.

[0020] Three different kinds of biases can be extracted from the level shifter 200. The node 220, as well as nodes 222 and 224 can provide biases for clamping with the same polarity as the input signal D, while the node 218, as well as nodes 226 and 228 can provide biases for clamping with the reversed polarity as the input signal DB. A pair of PMOS transistors, having their gates coupled to their drains and receiving outputs from nodes 222 and 226, provide a fixed bias R. Other nodes provide swing biases depending on the switch from the input signal D to the complementary input signal DB.

[0021] It is understood that the PMOS transistors 206, 208, 210, 212, 214 and 216 can be NMOS diodes, PMOS diodes, NMOS transistors, P-N junction diodes, or the combination thereof. If a NMOS transistor is connected as a diode, its gate is connected to its drain. Similarly, if a PMOS transistor is connected as a diode, its gate is connected to its drain.

[0022] FIG. 2B illustrates a level shifter 230 for generating the differential biases in accordance with another embodiment of the present invention. A PMOS transistor 244 is coupled to the I/O power supply with an I/O voltage VDDI. One or more capacitors 232, 236 and 240 are serially coupled to the drain of the PMOS

transistor 244 for receiving an input signal D. A PMOS transistor 246 is coupled to the I/O power supply in parallel to the PMOS transistor 244. The gate of the transistor 246 is coupled to the drain of the transistor 244, and the gate of the transistor 244 is coupled to the drain of the transistor 246. One or more capacitors 234, 238 and 242 are serially coupled to the drain of the transistor 246 for receiving a complement of the input signal D.

[0023] A diode 252 is coupled to the I/O power supply in parallel to the transistor 244. A PMOS transistor 248 is serially coupled to the diode 252, and having a gate connected to its drain, which is further coupled to the drain of the transistor 244. A second diode 254 is coupled to the I/O power supply in parallel to the transistor 246. A PMOS transistor 250 is serially coupled to the diode 254, and having a gate connected to its drain, which is further coupled to the drain of the transistor 246.

[0024] It is understood that this level shifter 230 can generate the differential biases for proper clamping of transistors within I/O drivers shown in FIG. 1A, 1B, and 1C. The level shifter 230 is a bootstrap level shifter composed of six bootstrap NMOS capacitors 232, 234, 236, 238, 240, and 242, which can be seen as capacitance devices providing an arbitrary capacitance value for determining the biases. The NMOS capacitors 232, 236, and 240 in a stack formation can be seen as a bootstrap module and the NMOS capacitors 234, 238, and 242 in a stack formation can be seen as another bootstrap module. An input signal D switches from low to high or high to low, while a node 256 will be coupled high or low accordingly. The combination of the transistors 244 and 246 form a cross-coupled structure for latching a signal. The diode 252 or 254 works along with the transistor 248 or 250 to provide a leakage path if either the node 256 or 258 is floating. As such, the node 258 or 256 outputs a bias that controls the I/O drivers in response to the input signal D.

[0025] The level shifter 230 has several advantages. The level shifter 230 can perform faster while allowing the bias to be generated arbitrarily depending on capacitance ratios which is easier than counting on fixed threshold voltages. There is also no temperature dependence during generation of bias. Furthermore, the level shifter 230 puts less oxide stress on devices and has less leakage. All MOS capacitors also share the same bulks, meaning it will take up less area.

[0026] It is understood that the MOS devices shown in FIG. 2B can be zero-V_t devices, depletion devices, N⁺ on N-bulk MOS capacitors, or P⁺ on P-bulk MOS capacitors.

[0027] FIG. 3 illustrates a circuit 300 with an I/O driver 302 biased by a level shifter 304 in accordance with one embodiment of the present invention. The I/O driver 302 is equivalent to the I/O driver 100 shown in FIG. 1A, with one of its thin-oxide devices biased by the level shifter 304. The level shifter 304 operates in the same way as the level shifter 230 shown in FIG. 2B, except that it has one less NMOS capacitor.

[0028] Thin-oxide PMOS transistors 306 and 308 are placed in a pull-up module along with thin-oxide NMOS transistors 310 and 312 in a pull-down module. Both the gates of the transistors 308 and 310 are clamped to core voltage VDDC while the gate of the transistor 312 can be driven by an inverter 314, thereby allowing it to swing between 0 volts to core voltage VDDC. The gate of the transistor 306 is biased by a voltage at a node 316 of the level shifter 304, thereby allowing it to switch between a high voltage value and a low voltage value, depending on the changing value of input signal D.

[0029] The level shifter 304 operates similarly to the bootstrap level shifter 230 of FIG. 2B. In the level shifter 304, capacitors 318, 320, 322, and 324 are charged to

VDDI - VDDC initially through the leakers composed of diodes 326 and 328 and PMOS transistors 330 and 332. If an input signal D is set to low, a PMOS transistor 334 is turned off, while a PMOS transistor 336 is turned on, thereby allowing high voltage VDDI to reach the node 316, thereby turning off the transistor 306. Meanwhile, the input signal D also drives the inverter 314 and turns on the transistor 312 of the I/O driver 304. With the transistor 306 turned off and the transistor 312 turned on, the output voltage at a node 338 is 0V. When the input signal D is switching from low to high, a node 340 is bootstrapped to high and equal to VDDI. The node 316 will be coupled low, equaling to VDDC. The voltage at the node 316 will then be sufficient to turn on the transistor 306 such that the node 338 of the I/O driver 304 can be pulled high.

[0030] According to the embodiments of the invention, multiple thin-oxide devices can be placed in a cascade formation where each device is controlled by a proper bias provided by level shifters. The bias voltage at the gate of each thin-oxide devices allows them to operate under higher voltage without sustaining high voltage damage. This makes high voltage I/O driver implemented with only thin-oxide devices possible, thereby removing the need of additional masks for thick-oxide devices and thus saving cost and fabrication time.

[0031] The above illustration provides many different embodiments or embodiments for implementing different features of the invention. Specific embodiments of components and processes are described to help clarify the invention. These are, of course, merely embodiments and are not intended to limit the invention from that described in the claims.

[0032] Although the invention is illustrated and described herein as embodied in one or more specific examples, it is nevertheless not intended to be limited to the

details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention, as set forth in the following claims.

WHAT IS CLAIMED IS:

1. An input/output (I/O) circuit for outputting an output signal of a first voltage in response to an input signal of a second voltage lower than the first voltage, comprising:

a pull-down module having one or more NMOS transistors serially coupled between ground and an output node;

a pull-up module having one or more PMOS transistors serially coupled between an I/O voltage and the output node; and

a level shifter responsive to the input signal for generating a set of differential biases selectively enabling or disabling the pull-down and pull-up models to pull the output node to the I/O voltage or ground,

wherein the differential biases are separately set for each of the PMOS transistors so that a voltage difference across each of the PMOS transistors does not exceed a predetermined value, thereby preventing the same from damage, wherein the level shifter further comprises:

a first PMOS transistor coupled to the I/O voltage;

a first group of one or more voltage dropping PMOS transistors each of which has its gate connected to its drain, serially coupled to a drain of the first PMOS transistor;

a first NMOS transistor serially coupled between the first group of the voltage dropping PMOS transistors and ground, having a gate controlled by the input signal;

a second PMOS transistor coupled to the I/O voltage in parallel to the first PMOS transistor, wherein the gate of the second PMOS transistor is coupled to the drain of the first PMOS transistor, and the gate of the first PMOS transistor is coupled to the drain of the second PMOS transistor;

a second group of one or more voltage dropping PMOS transistors each of which has its gate connected to its drain, serially coupled to a drain of the second PMOS transistor; and

a second NMOS transistor serially coupled between the second group of voltage dropping PMOS transistors and ground, having a gate controlled by a complement of the input signal,

wherein the drains of the first and second PMOS transistors and the first and second groups of the voltage dropping PMOS transistors provide the differential biases.

2. The I/O circuit of claim 1 wherein the level shifter further comprises:

a third PMOS transistor having its gate coupled to its drain; and

a fourth PMOS transistor having its gate coupled to its drain, which is further coupled to the drain of the third PMOS transistor,

wherein the third and fourth PMOS transistors receive a complementary pair of the differential biases from the drains of the first and second groups of the voltage dropping PMOS transistors, and output a fixed bias.

3. An input/output I/O circuit for outputting an output signal of a first voltage in response to an input signal of a second voltage lower than the first voltage, comprising :

a pull-down module having one or more NMOS transistors serially coupled between ground and an output node;

a pull-up module having one or more PMOS transistors serially coupled between an I/O voltage and the output node; and

a level shifter responsive to the input signal for generating a set of differential biases selectively enabling or disabling the pull-down and pull-up modules to pull the output node to the I/O voltage or ground,

wherein the differential biases are separately set for each of the PMOS transistors so that a voltage difference across each of the PMOS transistors does not exceed a predetermined value, thereby preventing the same from damage, wherein the level shifter further comprises:

a first PMOS transistor coupled to the I/O voltage;

a first group of one or more capacitors serially coupled to a drain of the first PMOS transistor for receiving the input signal;

a second PMOS transistor coupled to the I/O voltage in parallel to the first PMOS transistor, wherein the gate of the second PMOS transistor is coupled to the drain of the first PMOS transistor and the gate of the first PMOS transistor is coupled to the drain of the second PMOS transistor; and

a second group of one or more capacitors serially coupled to a drain of the second PMOS transistor for receiving a complement of the input signal

wherein the drains of the first and second PMOS transistors provide the differential biases.

4. The I/O circuit of claim 3 wherein the level shifter further comprises:

a first diode coupled to the I/O voltage in parallel to the first PMOS transistor;
and

a third PMOS transistor serially coupled to the first diode, and having a gate connected to a drain of the same, which is further coupled to the drain of the first PMOS transistor.

5. The I/O circuit of claim 3 wherein the level shifter further comprises:

a second diode coupled to the I/O voltage in parallel to the second PMOS transistor; and

a fourth PMOS transistor serially coupled to the second diode, and having a gate connected to a drain of the same, which is further coupled to the drain of the second PMOS transistor.