

LOGICAL CHANNEL PRIORITIZATION

TECHNICAL FIELD

[0001] The present disclosure relates to wireless communications, and more specifically to user equipment (UE) and methods for supporting logical channel prioritization.

BACKGROUND

[0002] A wireless communications system may include one or multiple network communication devices, such as base stations, which may be otherwise known as an eNodeB (eNB), a next-generation NodeB (gNB), or other suitable terminology. Each network communication devices, such as a base station may support wireless communications for one or multiple user communication devices, which may be otherwise known as UE, or other suitable terminology. The wireless communications system may support wireless communications with one or multiple user communication devices by utilizing resources of the wireless communication system (e.g., time resources (e.g., symbols, slots, subframes, frames, or the like) or frequency resources (e.g., subcarriers, carriers). Additionally, the wireless communications system may support wireless communications across various radio access technologies including third generation (3G) radio access technology, fourth generation (4G) radio access technology, fifth generation (5G) radio access technology, among other suitable radio access technologies beyond 5G (e.g., sixth generation (6G)).

[0003] Delay status report of buffered data is enabled for extended reality (XR) service. That is, a UE reports delay status of buffered data to a base station for delay awareness scheduling for the data.

[0004] However, logical channel prioritization (LCP) procedure does not consider delay status of the buffered data but a priority of a logical channel. The delay critical data may not be multiplexed to a medium access control (MAC) protocol data unit (PDU) for an uplink (UL) grant during the MAC PDU assembling procedure, and the delay critical data may be discarded. Thus, the capacity is impacted.

SUMMARY

[0005] The present disclosure relates to UE and methods that support logical channel prioritization. With the UE and methods, logical channel prioritization based on delay awareness may be achieved.

[0006] Some implementations of a UE described herein may include a processor and a transceiver coupled to the processor, wherein the processor is configured to: determine first delay status of data of a first LCH; and prioritize transmission of the data of the first LCH based on the first delay status of the data. In some implementations, the processor is configured to prioritize transmission of the data of the first LCH based on the first delay status of the data by prioritizing transmission of a first type of data of the first LCH. The first delay status comprises first remaining time of the first type of data, the first remaining time of the first type of data is below a remaining time threshold.

[0007] In some implementations, the processor is configured to prioritize transmission of the data of the first LCH based on the first delay status of the data by one of the following: prioritizing transmission of the data of the first LCH over data of a second LCH, or prioritizing transmission of the first type of data of the first LCH over the data of the second LCH, or prioritizing transmission of the first type of data of the first LCH over a second type of data of the first LCH, wherein the first delay status comprises second remaining time of the second type of data, the second remaining time of the second type of data is above the remaining time threshold.

[0008] In some implementations, the processor is configured to prioritize transmission of the data of the first LCH based on the first delay status of the data by one of the following: allocating resources for the data of the first LCH and the data of the second LCH in a decreasing order of priority levels of the first LCH and the second LCH; or allocating resources for the first type of data of the first LCH and the data of the second LCH in a decreasing order of a first priority level for the first type of data and a priority level for the second LCH; or allocating resources for the first type of data of the first LCH and the second type of data of the first LCH in a decreasing order of the first priority level for the first type of data and a second priority level for the second type of data.

[0009] In some implementations, the processor is configured to prioritize the transmission of the data of the first LCH by increasing a first priority level for the first type of data of the first LCH to a target priority level.

[0010] In some implementations, the data of the first LCH further comprises a second type of data, the first delay status comprises second remaining time of the second type of data, the second remaining time of the second type of data is above the remaining time threshold. In such implementations, the processor is configured to prioritize the transmission of the data of the first LCH by keeping the first priority level for the second type of data of the first LCH unchanged.

[0011] In some implementations, the processor is configured to prioritize the transmission of the data of the first LCH by increasing a priority level for the data of the first LCH to a target priority level.

[0012] In some implementations, the target priority level is higher than one or more priority levels for a group of one or more LCHs.

[0013] In some implementations, the target priority level is higher than or equal to a third priority level for a third LCH, and the group of one or more LCHs excludes the third LCH.

[0014] In some implementations, the target priority level is lower than a fourth priority level for a fourth LCH.

[0015] In some implementations, the processor is further configured to: determine second delay status of data of a fifth LCH. The data of the fifth LCH comprises at least the first type of data, the second delay status comprises third remaining time of the first type of data of the fifth LCH, the third remaining time of the first type of data is below the remaining time threshold. In such implementations, the processor is configured to prioritize the transmission of the data of the first LCH by: prioritizing the transmission of the data of the first LCH based on determining that a first priority level for the first LCH is higher than a fifth priority level for the fifth LCH.

[0016] In some implementations, the processor is configured to prioritize transmissions of the data of the first LCH and the data of the fifth LCH by: prioritizing the transmissions of the data of the first LCH and the data of the fifth LCH in an decreasing order of the first priority level and the third priority level.

[0017] In some implementations, the processor is further configured to: determine second delay status of data of a fifth LCH, wherein the data of the fifth LCH comprises at least the first type of data, the second delay status comprises third remaining time of

the first type of data of the fifth LCH, the third remaining time of the first type of data is below the remaining time threshold; and the processor is configured to prioritize the transmission of the data of the first LCH by: prioritizing transmissions of the data of the first LCH and the data of the fifth LCH based on the first remaining time and the third remaining time.

[0018] In some implementations, the processor is configured to prioritize transmissions of the data of the first LCH and the data of the fifth LCH by: prioritizing the transmissions of the data of the first LCH and the data of the fifth LCH in an increasing order of the first remaining time and the third remaining time.

[0019] In some implementations, the processor is configured to prioritize transmissions of the data of the first LCH and the data of the fifth LCH by: prioritizing the transmissions of the data of the first LCH and the data of the fifth LCH based on the following: the first remaining time, the third remaining time, a first priority level for the first LCH, and a fifth priority level for the fifth LCH.

[0020] In some implementations, the processor is configured to prioritize transmissions of the data of the first LCH and the data of the fifth LCH by: prioritizing the transmissions of the data of the first LCH and the data of the fifth LCH in an decreasing order of the first priority level and the fifth priority level and then in an increasing order of the first remaining time and the third remaining time; or prioritizing the transmissions of the data of the first LCH and the data of the fifth LCH in the increasing order of the first remaining time and the third remaining time and then in the decreasing order of the first priority level and the fifth priority level.

[0021] In some implementations, the processor is configured to increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on at least one of the following: an absolute priority value, a priority offset value, or a factor.

[0022] In some implementations, the remaining time threshold is configured for the first LCH or for a logical channel group (LCG) comprising the first LCH.

[0023] In some implementations, the processor is configured to prioritize the transmission of the data of the first LCH by: prioritizing the transmission of the data of

the first LCH based on the delay status of the data and a value which is maintained for the first LCH.

[0024] In some implementations, the processor is further configured to: determine, based on at least one logical channel prioritization (LCP) configuration for the first LCH, the value which is maintained for the first LCH.

[0025] In some implementations, the at least one LCP configuration comprises a dedicated LCP configuration, the dedicated LCP configuration comprises at least one of the following: a second prioritized bit rate (PBR) or a second bucket size duration (BSD).

[0026] In some implementations, the at least one LCP configuration further comprises a first LCP configuration, the first LCP configuration comprises a first prioritized bit rate (PBR) and a first bucket size duration (BSD), the first PBR is separate from the second PBR, the first BSD is separate from the second BSD.

[0027] In some implementations, the processor is further configured to: determine, based on a size of a first type of data of the first LCH, the value which is maintained for the first LCH. The first delay status comprises first remaining time of the first type of data, the first remaining time of the first type of data is below a remaining time threshold.

[0028] In some implementations, the processor is configured to determine the value which is maintained for the first LCH by: based on determining that the value is less than the size of the first type of data, determining the size of the first type of data as the value.

[0029] In some implementations, the processor is configured to determine the value which is maintained for the first LCH by: based on determining that the size of the first type of data is greater than a bucket size associated with the first LCH, determining the bucket size as the size of the first type of data; and determining the value which is maintained for the first LCH based on the bucket size.

[0030] In some implementations, the processor is further configured to: receive, via the transceiver from a base station, a configuration for a bucket size associated with the first LCH; and determine, based on the bucket size, the value which is maintained for the first LCH.

[0031] In some implementations, the processor is further configured to: determine a bucket size based on a first size of a protocol data unit (PDU) Set comprising the first

type of data or a second size of a data burst comprising the first type of data; and determine the value which is maintained for the first LCH based on the first size and the second size.

[0032] In some implementations, the processor is configured to prioritize the transmission of the data of the first LCH based on the first delay status of the data based on determining one of the following: protocol data unit (PDU) set discard is configured for a data radio bearer (DRB) of the data of the first LCH; the PDU set discard is activated for the DRB of the data of the first LCH; the PDU set discard is deactivated for the DRB of the data of the first LCH; a first type of data of the first LCH has high importance; PDU set importance (PSI) based discard is configured for the DRB of the data of the first LCH; the PSI based discard is activated for the DRB of the data of the first LCH; or the PSI based discard is deactivated for the DRB of the data of the first LCH.

[0033] In some implementations, the processor is configured to prioritize the transmission of the data of the first LCH based on the first delay status of the data regardless of a value which is maintained for the first LCH.

[0034] In some implementations, the data of the first LCH is a first type of data of the first LCH, the first delay status comprises first remaining time of the first type of data, the first remaining time of the first type of data is below a remaining time threshold.

[0035] In some implementation, the UE 104 transmits capability to indicate whether to prioritize transmission of data of one or more LCHs based on delay status of the data.

[0036] In some implementations, the processor is further configured to: receive, via the transceiver from a base station, a first indication indicating whether to prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0037] In some implementations, the processor is configured to receive the first indication via a Layer 1, Layer 2 or Layer 3 signaling.

[0038] In some implementations, the processor is configured to receive the first indication together with an uplink (UL) grant. In such implementations, the processor is configured to prioritize the transmission of the data of the first LCH based on the first delay status of the data by: based on determining that the first indication indicates to prioritize the transmission of the data of the first LCH based on the first delay status of the data, prioritizing the transmission of the data of the first LCH for the UL grant.

[0039] In some implementations, the processor is further configured to: receive, via the transceiver from a base station, a second indication indicating to activate or deactivate the prioritizing of the transmission of the data of the first LCH based on the first delay status of the data.

[0040] Some implementations of a UE described herein may include a processor and a transceiver coupled to the processor, wherein the processor is configured to: receive, via the transceiver from a base station, a command indicating to prioritize transmission of data of a first LCH; and prioritize the transmission of the data of the first LCH based on the command.

[0041] In some implementations, the command indicates to prioritize the transmission of the data of the first LCH by indicating to increase a first priority level for a first type of data of the first LCH to a target priority level. First remaining time of the first type of data is below a remaining time threshold.

[0042] In some implementations, the processor is further configured to: determine the first remaining time of the first type of data.

[0043] In some implementations, the command indicates to prioritize the transmission of the data of the first LCH by indicating to increase a priority level for the data of the first LCH to a target priority level.

[0044] In some implementations, the command indicates information to determine the target priority level.

[0045] In some implementations, the command indicates the target priority level.

[0046] In some implementations, the command indicates the target priority level by indicating one of the following: an absolute priority value, a priority offset value, or a factor.

[0047] Some implementations of a base station described herein may include a processor and a transceiver coupled to the processor, wherein the processor is configured to: receive, via the transceiver from a UE, capability indicating whether to prioritize transmission of data of one or more LCHs based on delay status of the data; and transmit, via the transceiver to the UE, an indication indicating whether to prioritize the transmission of the data of the one or more LCHs based on the delay status of the data.

[0048] Some implementations of a method described herein may include: determining first delay status of data of a first LCH; and prioritizing transmission of the data of the first LCH based on the first delay status of the data.

[0049] Some implementations of a method described herein may include: receiving, from a base station, a command indicating to prioritize transmission of data of a first LCH; and prioritizing the transmission of the data of the first LCH based on the command.

[0050] Some implementations of a processor described herein may include at least one memory and a controller coupled with the at least one memory and configured to cause the controller to: determine first delay status of data of a first LCH; and prioritize transmission of the data of the first LCH based on the first delay status of the data.

[0051] Some implementations of a processor described herein may include at least one memory and a controller coupled with the at least one memory and configured to cause the controller to: receive, from a base station, a command indicating to prioritize transmission of data of a first LCH; and prioritize the transmission of the data of the first LCH based on the command.

[0052] It is to be understood that the summary section is not intended to identify key or essential features of embodiments of the present disclosure, nor is it intended to be used to limit the scope of the present disclosure. Other features of the present disclosure will become easily comprehensible through the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0053] Fig. 1 illustrates an example of a wireless communications system that supports logical channel prioritization in accordance with aspects of the present disclosure;

[0054] Fig. 2 illustrates an example of a legacy logical channel prioritization;

[0055] Fig. 3 illustrates a flowchart of a process for multiplexing a MAC PDU of a logical channel in accordance with aspects of the present disclosure;

[0056] Figs. 4, 5 and 6 illustrate a signaling chart illustrating an example process that supports logical channel prioritization in accordance with aspects of the present disclosure, respectively;

[0057] Fig. 7 illustrates an example of a device that supports logical channel prioritization in accordance with some aspects of the present disclosure;

[0058] Fig. 8 illustrates an example of a processor that supports logical channel prioritization in accordance with aspects of the present disclosure; and

[0059] Figs. 9 and 10 illustrate a flowchart of a method that supports logical channel prioritization in accordance with aspects of the present disclosure, respectively.

DETAILED DESCRIPTION

[0060] Principles of the present disclosure will now be described with reference to some embodiments. It is to be understood that these embodiments are described only for the purpose of illustration and help those skilled in the art to understand and implement the present disclosure, without suggesting any limitation as to the scope of the disclosure. The disclosure described herein may be implemented in various manners other than the ones described below.

[0061] In the following description and claims, unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skills in the art to which this disclosure belongs.

[0062] References in the present disclosure to “one embodiment,” “an example embodiment,” “an embodiment,” “some embodiments,” and the like indicate that the embodiment(s) described may include a particular feature, structure, or characteristic, but it is not necessary that every embodiment includes the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment(s). Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0063] It shall be understood that although the terms “first” and “second” or the like may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. For example, a first element could also be termed as a second element, and similarly, a second element could also be termed as a first element, without departing from the scope of embodiments. As used herein, the term “and/or” includes any and all combinations of one or more of the listed terms.

[0064] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of example embodiments. As used herein, the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises”, “comprising”, “has”, “having”, “includes” and/or “including”, when used herein, specify the presence of stated features, elements, and/or components etc., but do not preclude the presence or addition of one or more other features, elements, components and/or combinations thereof.

[0065] Aspects of the present disclosure are described in the context of a wireless communications system.

[0066] Fig. 1 illustrates an example of a wireless communications system 100 that supports logical channel prioritization in accordance with aspects of the present disclosure. The wireless communications system 100 may include one at least one of network entities 102 (also referred to as network equipment (NE)), one or more terminal devices or UEs 104, a core network 106, and a packet data network 108. The wireless communications system 100 may support various radio access technologies. In some implementations, the wireless communications system 100 may be a 4G network, such as an LTE network or an LTE-advanced (LTE-A) network. In some other implementations, the wireless communications system 100 may be a 5G network, such as an NR network. In other implementations, the wireless communications system 100 may be a combination of a 4G network and a 5G network, or other suitable radio access technology including institute of electrical and electronics engineers (IEEE) 802.11 (Wi-Fi), IEEE 802.16 (WiMAX), IEEE 802.20. The wireless communications system 100 may support radio access technologies beyond 5G. Additionally, the wireless communications system 100 may support technologies, such as time division multiple access (TDMA), frequency division multiple access (FDMA), or code division multiple access (CDMA), etc.

[0067] The network entities 102 may be dispersed throughout a geographic region to form the wireless communications system 100. One or more of the network entities 102 described herein may be or include or may be referred to as a network node, a base station (BS), a network element, a radio access network (RAN) node, a base transceiver station, an access point, a NodeB, an eNodeB (eNB), a next-generation NodeB (gNB), or other suitable terminology. A network entity 102 and a UE 104 may communicate via a

communication link 110, which may be a wireless or wired connection. For example, a network entity 102 and a UE 104 may perform wireless communication (e.g., receive signaling, transmit signaling) over a Uu interface. The network entities 102 may be collectively referred to as network entities 102 or individually referred to as a network entity 102. Hereinafter, some implementations of the present disclosure will be described by taking a base station as an example of the network entity 102. Thus, the network entity 102 may be used interchangeably with the base station 102.

[0068] A network entity 102 may provide a geographic coverage area 112 for which the network entity 102 may support services (e.g., voice, video, packet data, messaging, broadcast, etc.) for one or more UEs 104 within the geographic coverage area 112. For example, a network entity 102 and a UE 104 may support wireless communication of signals related to services (e.g., voice, video, packet data, messaging, broadcast, etc.) according to one or multiple radio access technologies. In some implementations, a network entity 102 may be moveable, for example, a satellite associated with a non-terrestrial network. In some implementations, different geographic coverage areas 112 associated with the same or different radio access technologies may overlap, but the different geographic coverage areas 112 may be associated with different network entities 102. Information and signals described herein may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0069] The one or more UEs 104 may be dispersed throughout a geographic region of the wireless communications system 100. A UE 104 may include or may be referred to as a mobile device, a wireless device, a remote device, a remote unit, a handheld device, or a subscriber device, or some other suitable terminology. In some implementations, the UE 104 may be referred to as a unit, a station, a terminal, or a client, among other examples. Additionally, or alternatively, the UE 104 may be referred to as an internet-of-things (IoT) device, an internet-of-everything (IoE) device, or machine-type communication (MTC) device, among other examples. In some implementations, a UE 104 may be stationary in the wireless communications system 100. In some other implementations, a UE 104 may be mobile in the wireless communications system 100.

[0070] The one or more UEs 104 may be devices in different forms or having different capabilities. Some examples of UEs 104 are illustrated in Fig. 1. A UE 104 may be capable of communicating with various types of devices, such as the network entities 102, other UEs 104, or network equipment (e.g., the core network 106, the packet data network 108, a relay device, an integrated access and backhaul (IAB) node, or another network equipment), as shown in Fig. 1. Additionally, or alternatively, a UE 104 may support communication with other network entities 102 or UEs 104, which may act as relays in the wireless communications system 100.

[0071] A UE 104 may also be able to support wireless communication directly with other UEs 104 over a communication link 114. For example, a UE 104 may support wireless communication directly with another UE 104 over a device-to-device (D2D) communication link. In some implementations, such as vehicle-to-vehicle (V2V) deployments, vehicle-to-everything (V2X) deployments, or cellular-V2X deployments, the communication link 114 may be referred to as a sidelink. For example, a UE 104 may support wireless communication directly with another UE 104 over a PC5 interface.

[0072] A network entity 102 may support communications with the core network 106, or with another network entity 102, or both. For example, a network entity 102 may interface with the core network 106 through one or more backhaul links 116 (e.g., via an S1, N2, N2, or another network interface). The network entities 102 may communicate with each other over the backhaul links 116 (e.g., via an X2, Xn, or another network interface). In some implementations, the network entities 102 may communicate with each other directly (e.g., between the network entities 102). In some other implementations, the network entities 102 may communicate with each other or indirectly (e.g., via the core network 106). In some implementations, one or more network entities 102 may include subcomponents, such as an access network entity, which may be an example of an access node controller (ANC). An ANC may communicate with the one or more UEs 104 through one or more other access network transmission entities, which may be referred to as a radio heads, smart radio heads, or transmission-reception points (TRPs).

[0073] In some implementations, a network entity 102 may be configured in a disaggregated architecture, which may be configured to utilize a protocol stack physically or logically distributed among two or more network entities 102, such as an integrated

access backhaul (IAB) network, an open radio access network (O-RAN) (e.g., a network configuration sponsored by the O-RAN Alliance), or a virtualized RAN (vRAN) (e.g., a cloud RAN (C-RAN)). For example, a network entity 102 may include one or more of a central unit (CU), a distributed unit (DU), a radio unit (RU), a RAN intelligent controller (RIC) (e.g., a near-real time RIC (Near-RT RIC), a non-real time RIC (Non-RT RIC)), a service management and orchestration (SMO) system, or any combination thereof.

[0074] An RU may also be referred to as a radio head, a smart radio head, a remote radio head (RRH), a remote radio unit (RRU), or a transmission reception point (TRP). One or more components of the network entities 102 in a disaggregated RAN architecture may be co-located, or one or more components of the network entities 102 may be located in distributed locations (e.g., separate physical locations). In some implementations, one or more network entities 102 of a disaggregated RAN architecture may be implemented as virtual units (e.g., a virtual CU (VCU), a virtual DU (VDU), a virtual RU (VRU)).

[0075] Split of functionality between a CU, a DU, and an RU may be flexible and may support different functionalities depending upon which functions (e.g., network layer functions, protocol layer functions, baseband functions, radio frequency functions, and any combinations thereof) are performed at a CU, a DU, or an RU. For example, a functional split of a protocol stack may be employed between a CU and a DU such that the CU may support one or more layers of the protocol stack and the DU may support one or more different layers of the protocol stack. In some implementations, the CU may host upper protocol layer (e.g., a layer 3 (L3), a layer 2 (L2)) functionality and signaling (e.g., radio resource control (RRC), service data adaptation protocol (SDAP), packet data convergence protocol (PDCP)). The CU may be connected to one or more DUs or RUs, and the one or more DUs or RUs may host lower protocol layers, such as a layer 1 (L1) (e.g., physical (PHY) layer) or an L2 (e.g., radio link control (RLC) layer, medium access control (MAC) layer) functionality and signaling, and may each be at least partially controlled by the CU.

[0076] Additionally, or alternatively, a functional split of the protocol stack may be employed between a DU and an RU such that the DU may support one or more layers of the protocol stack and the RU may support one or more different layers of the protocol stack. The DU may support one or multiple different cells (e.g., via one or more RUs). In some implementations, a functional split between a CU and a DU, or between a DU and

an RU may be within a protocol layer (e.g., some functions for a protocol layer may be performed by one of a CU, a DU, or an RU, while other functions of the protocol layer are performed by a different one of the CU, the DU, or the RU).

[0077] A CU may be functionally split further into CU control plane (CU-CP) and CU user plane (CU-UP) functions. A CU may be connected to one or more DUs via a midhaul communication link (e.g., F1, F1-c, F1-u), and a DU may be connected to one or more RUs via a fronthaul communication link (e.g., open fronthaul (FH) interface). In some implementations, a midhaul communication link or a fronthaul communication link may be implemented in accordance with an interface (e.g., a channel) between layers of a protocol stack supported by respective network entities 102 that are in communication via such communication links.

[0078] The core network 106 may support user authentication, access authorization, tracking, connectivity, and other access, routing, or mobility functions. The core network 106 may be an evolved packet core (EPC), or a 5G core (5GC), which may include a control plane entity that manages access and mobility (e.g., a mobility management entity (MME), an access and mobility management functions (AMF)) and a user plane entity that routes packets or interconnects to external networks (e.g., a serving gateway (S-GW), a packet data network (PDN) gateway (P-GW), or a user plane function (UPF)). In some implementations, the control plane entity may manage non-access stratum (NAS) functions, such as mobility, authentication, and bearer management (e.g., data bearers, signal bearers, etc.) for the one or more UEs 104 served by the one or more network entities 102 associated with the core network 106.

[0079] The core network 106 may communicate with the packet data network 108 over one or more backhaul links 116 (e.g., via an S1, N2, N2, or another network interface). The packet data network 108 may include an application server 118. In some implementations, one or more UEs 104 may communicate with the application server 118. A UE 104 may establish a session (e.g., a protocol data unit (PDU) session, or the like) with the core network 106 via a network entity 102. The core network 106 may route traffic (e.g., control information, data, and the like) between the UE 104 and the application server 118 using the established session (e.g., the established PDU session). The PDU session may be an example of a logical connection between the UE 104 and the core network 106 (e.g., one or more network functions of the core network 106).

[0080] In the wireless communications system 100, the network entities 102 and the UEs 104 may use resources of the wireless communications system 100 (e.g., time resources (e.g., symbols, slots, subframes, frames, or the like) or frequency resources (e.g., subcarriers, carriers)) to perform various operations (e.g., wireless communications). In some implementations, the network entities 102 and the UEs 104 may support different resource structures. For example, the network entities 102 and the UEs 104 may support different frame structures. In some implementations, such as in 4G, the network entities 102 and the UEs 104 may support a single frame structure. In some other implementations, such as in 5G and among other suitable radio access technologies, the network entities 102 and the UEs 104 may support various frame structures (i.e., multiple frame structures). The network entities 102 and the UEs 104 may support various frame structures based on one or more numerologies.

[0081] One or more numerologies may be supported in the wireless communications system 100, and a numerology may include a subcarrier spacing and a cyclic prefix. A first numerology (e.g., $\mu=0$) may be associated with a first subcarrier spacing (e.g., 15 kHz) and a normal cyclic prefix. In some implementations, the first numerology (e.g., $\mu=0$) associated with the first subcarrier spacing (e.g., 15 kHz) may utilize one slot per subframe. A second numerology (e.g., $\mu=1$) may be associated with a second subcarrier spacing (e.g., 30 kHz) and a normal cyclic prefix. A third numerology (e.g., $\mu=2$) may be associated with a third subcarrier spacing (e.g., 60 kHz) and a normal cyclic prefix or an extended cyclic prefix. A fourth numerology (e.g., $\mu=3$) may be associated with a fourth subcarrier spacing (e.g., 120 kHz) and a normal cyclic prefix. A fifth numerology (e.g., $\mu=4$) may be associated with a fifth subcarrier spacing (e.g., 240 kHz) and a normal cyclic prefix.

[0082] A time interval of a resource (e.g., a communication resource) may be organized according to frames (also referred to as radio frames). Each frame may have a duration, for example, a 10 millisecond (ms) duration. In some implementations, each frame may include multiple subframes. For example, each frame may include 10 subframes, and each subframe may have a duration, for example, a 1 ms duration. In some implementations, each frame may have the same duration. In some implementations, each subframe of a frame may have the same duration.

[0083] Additionally or alternatively, a time interval of a resource (e.g., a communication resource) may be organized according to slots. For example, a subframe may include a number (e.g., quantity) of slots. The number of slots in each subframe may also depend on the one or more numerologies supported in the wireless communications system 100. For instance, the first, second, third, fourth, and fifth numerologies (i.e., $\mu=0$, $\mu=1$, $\mu=2$, $\mu=3$, $\mu=4$) associated with respective subcarrier spacings of 15 kHz, 30 kHz, 60 kHz, 120 kHz, and 240 kHz may utilize a single slot per subframe, two slots per subframe, four slots per subframe, eight slots per subframe, and 16 slots per subframe, respectively. Each slot may include a number (e.g., quantity) of symbols (e.g., OFDM symbols). In some implementations, the number (e.g., quantity) of slots for a subframe may depend on a numerology. For a normal cyclic prefix, a slot may include 14 symbols. For an extended cyclic prefix (e.g., applicable for 60 kHz subcarrier spacing), a slot may include 12 symbols. The relationship between the number of symbols per slot, the number of slots per subframe, and the number of slots per frame for a normal cyclic prefix and an extended cyclic prefix may depend on a numerology. It should be understood that reference to a first numerology (e.g., $\mu=0$) associated with a first subcarrier spacing (e.g., 15 kHz) may be used interchangeably between subframes and slots.

[0084] In the wireless communications system 100, an electromagnetic (EM) spectrum may be split, based on frequency or wavelength, into various classes, frequency bands, frequency channels, etc. By way of example, the wireless communications system 100 may support one or multiple operating frequency bands, such as frequency range designations FR1 (410 MHz – 7.125 GHz), FR2 (24.25 GHz – 52.6 GHz), FR3 (7.125 GHz – 24.25 GHz), FR4 (52.6 GHz – 114.25 GHz), FR4a or FR4-1 (52.6 GHz – 71 GHz), and FR5 (114.25 GHz – 300 GHz). In some implementations, the network entities 102 and the UEs 104 may perform wireless communications over one or more of the operating frequency bands. In some implementations, FR1 may be used by the network entities 102 and the UEs 104, among other equipment or devices for cellular communications traffic (e.g., control information, data). In some implementations, FR2 may be used by the network entities 102 and the UEs 104, among other equipment or devices for short-range, high data rate capabilities.

[0085] FR1 may be associated with one or multiple numerologies (e.g., at least three numerologies). For example, FR1 may be associated with a first numerology (e.g., $\mu=0$), which includes 15 kHz subcarrier spacing; a second numerology (e.g., $\mu=1$), which

includes 30 kHz subcarrier spacing; and a third numerology (e.g., $\mu=2$), which includes 60 kHz subcarrier spacing. FR2 may be associated with one or multiple numerologies (e.g., at least 2 numerologies). For example, FR2 may be associated with a third numerology (e.g., $\mu=2$), which includes 60 kHz subcarrier spacing; and a fourth numerology (e.g., $\mu=3$), which includes 120 kHz subcarrier spacing.

[0086] As described above, logical channel prioritization (LCP) procedure does not consider delay status of the buffered data but a priority of a logical channel. The delay status of the buffered data may comprise remaining time of the buffered data. The delay critical data may not be multiplexed to a MAC PDU for a UL grant during the MAC PDU assembling procedure, and the delay critical data may be discarded. Thus, the capacity is impacted. This will be described with reference to Fig. 2.

[0087] Fig. 2 illustrates an example of a legacy LCP. In the example of Fig. 2, a priority of a logical channel (LCH) #1 is represented by P1, a priority of an LCH #2 is represented by P2, and P1 is higher than P2. Remaining time of data of the LCH #1 is equal to 10ms, and remaining time of data of the LCH #2 is equal to 3ms. A value which is maintained for the LCH #1 (represented by B1) is equal to Prioritized Bit Rate (PBR) $1 \cdot T$, and a bucket size for the LCH #1 (represented by bucket size 1) is equal to PBR $1 \cdot$ Bucket Size Duration (BSD). A value which is maintained for the LCH #2 (represented by B2) is equal to PBR $2 \cdot T$.

[0088] Because P1 is higher than P2, a UE may first allocate resources for the data of the LCH #1 for a UL grant. In other words, the data of the LCH #1 is multiplexed to a MAC PDU for the UL grant first. If the UL grant is exhausted after the data of the LCH #1 was multiplexed, the data of the LCH #2 will not be multiplexed to the MAC PDU for the UL grant. If the remaining time of data of the LCH #2 is equal to or less than a threshold the data of the LCH #2 is not timely multiplexed to a MAC PDU for transmission, the data of the LCH #2 may be discarded.

[0089] Fig. 3 illustrates a flowchart of a process 300 for multiplexing a MAC PDU of a logical channel in accordance with aspects of the present disclosure.

[0090] In the process 300, each LCH j has a token bucket (also referred to as “bucket”) and a value which is maintained for the LCH j . The value which is maintained for the LCH j is presented by B_j .

[0091] A bucket size maximum capacity of the token bucket 305 is equal to a product $PBR \times BSD$. The bucket size of the token bucket 305 is also referred to as a maximum capacity of the token bucket 305.

[0092] B_j may represent the number of tokens in the token bucket for the LCH j . B_j is initialized to zero when the LCH j is established. For each LCH j , the UE 104 shall increment B_j by the product $PBR \times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented. If the value of B_j is greater than the bucket size (i.e., $PBR \times BSD$), the UE 104 sets B_j to the bucket size.

[0093] As shown in Fig. 3, at 310, the UE 104 inject $PBR \times T$ tokens to the token bucket 305 at every instance of an LCP procedure.

[0094] At 320, the UE 104 increments B_j by the product $PBR \times T$, where T is the time elapsed since B_j was last incremented.

[0095] At 330, the UE 104 determines whether B_j is greater than zero.

[0096] If B_j is greater than zero, the UE 104 decrements B_j by the total size of MAC SDUs served to logical channel j at 340. The total size of MAC SDUs served to logical channel j is represented by T_{sdu} .

[0097] At 350, the UE 104 multiplex an SDU 315 in a MAC PDU.

[0098] At 360, the UE 104 determines whether PBR is met.

[0099] If PBR is met, the UE 104 processes the next LCH at 370.

[0100] If PBR is not met, the process 300 proceeds to block 395. At 395, the UE 104 receives packets from upper layer.

[0101] If the UE 104 determines B_j is not greater than zero at 330, the UE 104 determines, at 380, there are no available tokens in the token bucket 305 and the SDU 315 will not be multiplexed in the MAC PDU.

[0102] At 390, the UE 104 determines the processing of this LCH is completed, and then the next logical channel with lower priority will be processed.

[0103] In view of the above, the present disclosure provides a solution that supports logical channel prioritization. In this solution, a UE determines first delay status of data of a first LCH. In turn, the UE prioritizes transmission of the data of the first LCH based

on the first delay status of the data. In this way, logical channel prioritization based on delay awareness may be achieved.

[0104] Hereinafter, principle of the present disclosure will be described with reference to Figs. 4 to 10.

[0105] Fig. 4 illustrates a signaling chart illustrating an example process 400 that supports logical channel prioritization in accordance with aspects of the present disclosure. For the purpose of discussion, the process 400 will be described with reference to Fig. 1. The process 400 may involve the UE 104 and the base station 102 in Fig. 1.

[0106] As shown in Fig. 4, the UE 104 determines 410 first delay status of data of a first LCH.

[0107] In some implementations, delay status of data of an LCH may comprise remaining time of a discard timer of the data available for transmission on the LCH. Hereinafter, “remaining time of a discard timer of data available for transmission on an LCH” as “remaining time of data of an LCH” for brevity.

[0108] In some implementations, the remaining time of data of an LCH may be less than a threshold. Hereinafter, the threshold is also referred to as a remaining time threshold.

[0109] In some implementations, the remaining time of data of an LCH may be the smallest remaining time value of the PDCP discard timers among service data units (SDUs) buffered for the LCH.

[0110] In some implementations, the remaining time of data of an LCH may be the smallest remaining time value of the PDCP discard timers among SDUs buffered for a logical channel group (LCG) including the LCH.

[0111] Additionally or alternatively, in some implementations, the delay status of the data of the LCH may comprise a total amount of the data buffered for the LCH, for which the remaining time till the discard timer expiry is less than a threshold.

[0112] In some implementations, the data of the LCH may comprise at least one of the following:

- MAC SDUs that have not yet been multiplexed to a MAC sub-PDU;
- MAC sub-PDU that have not been multiplexed in a MAC PDU;
- MAC sub-PDU that have been multiplexed in a MAC PDU;

- RLC SDUs and RLC SDU segments that have not yet been included in an RLC data PDU;
- RLC data PDUs pending for initial transmission, and containing a RLC SDU or a RLC SDU segment;
- RLC data PDUs that are pending for retransmission (RLC AM);
- PDCP SDUs for which no PDCP Data PDUs have been constructed;
- PDCP Data PDUs that contain the PDCP SDUs and have not been submitted to lower layers;
- PDCP Control PDUs;
- for AM DRBs, the PDCP SDUs to be retransmitted; or
- for AM DRBs, the PDCP Data PDUs to be retransmitted.

[0113] The UE 104 prioritizes 420 transmission of the data of the first LCH based on the first delay status of the data.

[0114] In some implementations, the data of the first LCH may comprise a first type of data of the first LCH. The first delay status may comprise first remaining time of the first type of data, and the first remaining time of the first type of data is below a remaining time threshold. For example, the first remaining time of the first type of data is equal to or less than the remaining time threshold. In such implementations, the UE 104 may prioritize transmission of the first type of data of the first LCH. Hereinafter, the first type of data is also referred to as delay critical data for brevity.

[0115] In some implementations, if *pdu-SetDiscard* is not configured, a data for which the remaining time till *discardTimer* expiry is equal to or less than a remaining time threshold may be determined as delay critical data.

[0116] In some implementations, if *pdu-SetDiscard* is configured, a data belonging to a PDU Set of which at least one data has the remaining time till *discardTimer* expiry equal to or less than a remaining time threshold may be determined as delay critical data.

[0117] With the process 400, logical channel prioritization based on delay awareness may be achieved.

[0118] Fig. 5 illustrates a signaling chart illustrating an example process 500 that supports logical channel prioritization in accordance with aspects of the present disclosure. The process 500 may be considered as an example implementation of the process 400.

For the purpose of discussion, the process 500 will be described with reference to Fig. 1. The process 500 may involve the UE 104 and the base station 102 in Fig. 1.

[0119] As shown in Fig. 5, the UE 104 determines 510 first delay status of data of a first LCH. The action 510 is similar to the action 410 in Fig. 4. Details of this action is omitted for brevity.

[0120] The UE 104 may receive 520 a first indication from the base station 102. The first indication may indicate whether to prioritize transmission of data of one or more LCHs based on delay status of the data. The one or more LCHs may comprise the first LCH.

[0121] In some implementations, the UE 104 may receive the first indication via a Layer 1 signaling.

[0122] In such implementations, the UE 104 may receive the first indication via Downlink Control Information (DCI).

[0123] For example, the first indication may be included in a dedicated DCI format.

[0124] For another example, the first indication may be included in an existing or legacy DCI format. For example, the existing or legacy DCI format may comprise one of the following: DCI format 0-0, DCI format 1-0, DCI format 0-1 or DCI format 1-1, DCI format 2-0, DCI format 2-1, DCI format 2-2, DCI format 2-3, DCI format 2-4, DCI format 2-5, or DCI format 2-6.

[0125] In some implementations, the UE 104 may receive the first indication together with a UL grant. In such implementations, if the first indication indicates to prioritize the transmission of the data of the first LCH based on the first delay status of the data, the UE 104 may prioritize the transmission of the data of the first LCH for the UL grant. For example, the first indication and the UL grant may be included in an existing or legacy DCI format. For example, the existing or legacy DCI format may comprise one of the following: DCI format 0-0 or DCI format 0-1. Alternatively, the first indication and the UL grant may be included in a dedicated DCI format.

[0126] Alternatively, in some implementations, the UE 104 may receive the first indication via a Layer 2 signaling. For example, the first indication may be included in a MAC CE. For example, the first indication may be included in one of the following: RLC control PDU, PDCP control PDU, or SDAP control PDU.

[0127] Alternatively, in some implementations, the UE 104 may receive the first indication via a Layer 3 signaling. For example, the first indication may be included in an RRC message.

[0128] In some implementations, the UE 104 may receive an LCP configuration from the base station 102. The LCP configuration may comprise the first indication.

[0129] In some implementations, an RRC entity of the UE 104 may control the scheduling of uplink data based on the LCP configuration by signalling at least one of the following for each logical channel per MAC entity:

- *priority* where an increasing priority value indicates a lower priority level;
- *prioritisedBitRate* which sets the PBR; or
- *bucketSizeDuration* which sets the BSD.

[0130] In some implementations, the first indication may be configured per LCH. In other words, the first indication may indicate whether to prioritize transmission of data of an LCH based on delay status of the data. For example, the first indication may indicate whether to prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0131] In some implementations, the first indication may indicate to prioritize transmission of all data of the first LCH based on the first delay status of the first LCH.

[0132] Alternatively, in some implementations, the first indication may indicate to prioritize transmission of the first type of data of the first LCH based on the first delay status of the first LCH.

[0133] In some implementations, the first indication may indicate a remaining time threshold for the first LCH. If the first indication does not indicate the remaining time threshold, the UE 104 may use a delay threshold (or a remaining time threshold) configured for delay status report (DSR) triggered for a logical channel group (LCG) including the first LCH.

[0134] Alternatively, in some implementations, the first indication may be configured per LCG. In other words, the first indication may indicate whether to prioritize transmission of data of an LCG based on delay status of the data. The LCG may comprise the first LCH.

[0135] In some implementations, the first indication may indicate to prioritize transmission of all data of all LCHs in the LCG based on delay status of the data.

[0136] Alternatively, in some implementations, the first indication may indicate to prioritize transmission of the first type of data of all LCHs in the LCG based on delay status of the data. The LCG may comprise the first LCH.

[0137] In some implementations, the first indication may indicate a remaining time threshold for the LCG. If the first indication does not indicate the remaining time threshold, the UE 104 may use a delay threshold (or a remaining time threshold) configured for DSR triggered for the LCG. The LCG may comprise the first LCH. In some implementations, if the UE 104 may use a delay threshold (or a remaining time threshold) configured for DSR triggered for an LCG including the first LCH, the UE prioritizes transmission of the first type of data of all LCHs in the LCG associated with triggered delay status.

[0138] With continued reference to Fig. 5, the UE 104 may further receive a second indication from the base station 102. The second indication indicates to activate prioritizing of transmission of data of one or more LCHs based on delay status of the data. The one or more LCHs may comprise the first LCH.

[0139] For example, the one or more LCHs may be configured to allow to prioritize transmission of data of one or more LCHs based on delay status of the data. Alternatively, the one or more LCHs may be configured with a respectively remaining time threshold.

[0140] In some implementations, the second indication may comprise one bit to indicate the UE 104 to activate or trigger prioritizing of transmission of data of the one or more LCHs.

[0141] In some implementations, the second indication may comprise a bitmap to indicate the UE 104 to activate or trigger prioritizing of transmission of data of the one or more LCHs. Each bit in the bitmap may be associated with one of the one or more LCHs.

[0142] In turn, the UE 104 may prioritize transmission of the data of the first LCH based on the first delay status of the data. For example, the UE 104 may prioritize transmission of the data of the first LCH based on the first delay status of the data based on the second indication.

[0143] Then, in some implementations, the UE 104 may further receive, from the base station 102, the second indication which indicates to deactivate prioritizing of transmission of data of one or more LCHs based on delay status of the data. In such embodiments, the UE 104 may allocate resources to the LCHs selected for the UL grant with B_j at least for delay critical data of the LCHs in descending order of the configured priorities.

[0144] In some implementations, the UE 104 may prioritize transmission of the data of the first LCH over data of a second LCH. In such implementations, the UE 104 may allocate resources for the data of the first LCH and the data of the second LCH in a decreasing order of priority levels for the first LCH and the second LCH, where a priority level for the first LCH is higher than a priority level for the second LCH. In other words, the UE 104 may allocate resources for the data of the first LCH before allocating resources for the data of the second LCH.

[0145] In some implementations, a priority level for an LCH may indicate a priority level for allocating resources for data of the LCH. Hereinafter, the term “priority level” may be used interchangeably with the term “priority”. An increasing value of a priority may indicate a lower priority level. Alternatively, an increasing value of a priority may indicate a higher priority level.

[0146] Alternatively, in some implementations, the UE 104 may prioritize transmission of the first type of data of the first LCH over the data of the second LCH. In such implementations, the UE 104 may allocate resources for the first type of data of the first LCH and the data of the second LCH in a decreasing order of a first priority level for the first type of data and a priority level for the second LCH. In other words, the UE 104 may allocate resources for the first type of data of the first LCH before allocating resources for the data of the second LCH.

[0147] Alternatively, in some implementations, the UE 104 may prioritize transmission of the first type of data of the first LCH over a second type of data of the first LCH. The first delay status of the data of the first LCH may comprise second remaining time of the second type of data. The second remaining time of the second type of data is equal to or greater than the remaining time threshold. Hereinafter, the second type of data is also referred to as non-delay critical data, or the second type of data is also referred to as data not associated with a triggered delay status report. In such

implementations, the UE 104 may allocate resources for the first type of data of the first LCH and the second type of data of the first LCH in a decreasing order of the first priority level for the first type of data and a second priority level for the second type of data. In other words, the UE 104 may allocate resources for the first type of data of the first LCH before allocating resources for the second type of data of the first LCH.

[0148] In some implementations, the buffered data of the second LCH may be not associated with a triggered DSR. In such implementations, the second LCH may be an LCH without delay critical data. In some implementations, the second LCH may not be configured with a delay threshold (or a remaining time threshold) to determine the delay status of data. In some implementations, the second LCH is not allowed to trigger DSR.

[0149] Alternatively, the second LCH may be associated with a triggered DSR and remaining time of the data of the second LCH may be equal to or greater than a remaining time threshold. In such implementations, the second LCH may be an LCH with non-delay critical data. That is to say, the second LCH has buffered data with remaining time below a remaining time threshold and with remaining time equal to or greater than a remaining time threshold.

[0150] In some implementations, the UE 104 may prioritize the transmission of the data of the first LCH by increasing the first priority level for the first type of data of the first LCH to a target priority level.

[0151] In some implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH during the first round of resource allocation procedure. For example, the UE 104 may first increase the priority level for first type of the data of the first LCH, before the UE 104 may allocate resources to the logical channels selected for the UL grant with $B_j > 0$ in decreasing order of priority. Alternatively, the UE 104 may increase the first priority level for the first type of data of the first LCH during the second round of resource allocation procedure. For example, after the UE 104 may allocate resources to the logical channels selected for the UL grant with $B_j > 0$ in decreasing order of priority, the UE 104 may first increase the priority level for first type of data of the first LCH. In some implementations, during the first round of resource allocation procedure, the UE 104 allocates resources for each LCH j based on B_j .

[0152] In some implementations, during the second round of resource allocation procedure, the UE 104 allocates resources for each LCH j regardless of B_j .

[0153] In some implementations, the UE 104 may first increase the priority level for the first type of data of the first LCH, the UE 104 may first allocate resources to the logical channels with delay critical data for the UL grant with $B_j > 0$ for the delay critical data in decreasing order of priority, decrement B_j by the total size of MAC SDUs served to the logical channel j . And further if any resources remain, the UE 104 may first allocate resources to the logical channels with non-delay critical data for the UL grant with $B_j > 0$ for the non-delay critical data in decreasing order of priority, decrement B_j by the total size of MAC SDUs served to the logical channel j with non-delay critical data. In some implementations, the UE 104 may allocate resources to the logical channels selected for the UL grant with $B_j > 0$ in decreasing order of priority, and decrement B_j by the total size of MAC SDUs served to logical channel j . If any resources remain, the UE 104 may increase the priority level for the first type of data of the first LCH, the logical channels selected are served in a strict order of that with delay critical data and that without delay critical data (regardless of the value of B_j) until either the data for that logical channel or the UL grant is exhausted, whichever comes first. If there is more than one LCH with delay critical data, the logical channels selected with delay critical data are served in a strict decreasing order of priority or in a strict increasing order of remaining time value.

[0154] In some implementations, an increasing priority value may indicate a lower priority level. In such implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH by decreasing a priority value for the first type of data of the first LCH.

[0155] Alternatively, an increasing priority value may indicate a higher priority level. In such implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH by increasing a priority value for the first type of data of the first LCH.

[0156] In some implementations, the UE 104 may only increase the first priority level for the first type of data of the first LCH to the target priority level and keep a priority level for the second type of data of the first LCH unchanged.

[0157] Consider a first example. In the first example, LCH#1 has a priority level of 1 (represented by priority 1), LCH#2 has a priority level of 2 (represented by priority 2), LCH#3 has a priority level of 3 (represented by priority 3), LCH#4 has a priority level of 4 (represented by priority 4). Priority 1 is higher than priority 2, priority 2 is higher than

priority 3, and priority 3 is higher than priority 4. In other words, a value of priority 1 < a value of priority 2 < a value of priority 3 < a value of priority 4.

[0158] In the first example, LCH#2 has delay critical data and non-delay critical data. LCH#3 has delay critical data and non-delay critical data. LCH#1 and LCH#4 has not delay critical data. That is, LCH#2 and LCH#3 are LCHs with delay critical data, LCH#2 and LCH#3 are also LCHs with non-delay critical data, LCH#1 and LCH#4 are LCHs without delay critical data, LCH#1 and LCH#4 are LCHs with non-delay critical data.

[0159] In order to prioritize transmissions of the delay critical data of LCH#2 and LCH#3, the UE 104 may increase priority levels for the delay critical data of LCH#2 and LCH#3 and keep priority levels for the non-delay critical data of LCH#2 and LCH#3 unchanged. Thus, a priority level for the non-delay critical data of LCH#2 is still equal to priority 2, and a priority level for the non-delay critical data of LCH#3 is still equal to priority 3.

[0160] In turn, the UE 104 may allocate resources for the delay critical data of LCH#2 and LCH#3 first. Then, the UE 104 may allocate resources for data of LCH#1, for the non-delay critical data of LCH#2, for the non-delay critical data of LCH#3 and for data of LCH#4 in a decreasing order of priority 1, priority 2, priority 3 and priority 4.

[0161] In the first example, the UE 104 may perform the procedure as shown in Table 1 below.

Table 1

The MAC entity of the UE 104 shall, when a new transmission is performed: 1>allocate resources to the logical channels as follows: 2>logical channels with delay critical data selected in clause 5.4.3.1.2 for the UL grant with $B_j > 0$ are allocated resourcesfor the delay critical data in decreasing order of priority. If the PBR of a logical channel is set to <i>infinity</i>, the MAC entity shall allocate resources for all the data that is available for transmission on the logical channel before meeting the PBR of the lower priority logical channel(s); 2>decrement B_j by the total size of MAC SDUs served to logical channel j above;
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2> logical channels (**with non-delay critical data**) selected in clause 5.4.3.1.2 for the UL grant with $B_j > 0$ are allocated resources for the non-delay critical data **in decreasing order of priority**. If the PBR of a logical channel is set to *infinity*, the MAC entity shall allocate resources for all the data that is available for transmission on the logical channel before meeting the PBR of the lower priority logical channel(s);

2> decrement B_j by the total size of MAC SDUs served to logical channel j above;

2> if any resources remain, all the logical channels selected in clause 5.4.3.1.2 are served in a strict decreasing priority order (regardless of the value of B_j) until either the data for that logical channel or the UL grant is exhausted, whichever comes first. Logical channels configured with equal priority should be served equally.

[0162] In some implementations, the UE 104 may prioritize the transmission of the data of the first LCH by increasing a priority level for the data of the first LCH to the target priority level. In other words, the UE 104 may prioritize the transmission of the data of the first LCH by increasing a priority level for all the data of the first LCH to the target priority level. That is, if the first LCH has delay critical data and non-delay critical data, priority levels for both delay critical data and non-delay critical data may be increased.

[0163] In some implementations, the UE 104 may increase the priority level for all the data of the first LCH during the first round of resource allocation procedure. For example, the UE 104 may first increase the priority level for all the data of the first LCH, then, the UE 104 may allocate resources to the logical channels selected for the UL grant with $B_j > 0$ in decreasing order of priority. Alternatively, the UE 104 may increase the priority level for all the data of the first LCH during the second round of resource allocation procedure. For example, after the UE 104 may allocate resources to the logical channels selected for the UL grant with $B_j > 0$ in decreasing order of priority, the UE 104 may first increase the priority level for all the data of the first LCH. In some implementations, the UE 104 may first increase the priority level for all the data of the

first LCH, then, the UE 104 may allocate resources to the logical channels selected for the UL grant with $B_j > 0$ in decreasing order of priority.

[0164] In some implementations, the UE 104 may allocate resources to the logical channels selected for the UL grant with $B_j > 0$ in decreasing order of priority, and decrement B_j by the total size of MAC SDUs served to logical channel j , and the UE 104 may increase the priority level for all the data of the first LCH. If any resources remain, all the logical channels selected are served in a strict decreasing priority order (regardless of the value of B_j) until either the data for that logical channel or the UL grant is exhausted, whichever comes first. The UE 104 may increase the priority level for all the data of the first LCH after the first round of resource allocation.

[0165] Consider a second example. In the second example, LCH#1 has a priority level of 1 (represented by priority 1), LCH#2 has a priority level of 2 (represented by priority 2), LCH#3 has a priority level of 3 (represented by priority 3), LCH#4 has a priority level of 4 (represented by priority 4). Priority 1 is higher than priority 2, priority 2 is higher than priority 3, and priority 3 is higher than priority 4. In other words, a value of priority 1 < a value of priority 2 < a value of priority 3 < a value of priority 4.

[0166] In the second example, LCH#2 has delay critical data and non-delay critical data. LCH#3 has delay critical data and non-delay critical data. LCH#1 and LCH#4 has not delay critical data. That is, LCH#2 and LCH#3 are LCHs with delay critical data, LCH#1 and LCH#4 are LCHs without delay critical data, LCH#1 and LCH#4 are LCHs with non- delay critical data.

[0167] The second example is different from the first example in that, in order to prioritize transmissions of data of LCH#2 and LCH#3, the UE 104 may increase priority levels for all the data of LCH#2 and LCH#3 so that the priority levels for all the data of LCH#2 and LCH#3 are higher than the priority levels for all the data of LCH#1 and LCH#4.

[0168] In turn, the UE 104 may allocate resources for all the data of LCH#2 and LCH#3 first. Then, the UE 104 may allocate resources for data of LCH#1 and for data of LCH#4 in a decreasing order of priority 1 and priority 4. In other words, the UE 104 may divide LCH#2 and LCH#3 into a first group of LCHs with delay critical data, and divide LCH#1 and LCH#4 into a second group of LCHs without delay critical data. The UE 104

may allocate resources for the data in an order of the first group of LCHs with delay critical data and the second group of LCHs without delay critical data.

[0169] In the second example, the UE 104 may perform the procedure as shown in Table 2 below.

Table 2

The MAC entity of the UE 104 shall, when a new transmission is performed: 1> allocate resources to the logical channels as follows: 2> logical channels selected in clause 5.4.3.1.2 for the UL grant with $B_j > 0$ are allocated resources in order of that LCHs with delay critical data and LCHs without delay critical data. If the PBR of a logical channel is set to <i>infinity</i>, the MAC entity shall allocate resources for all the data that is available for transmission on the logical channel before meeting the PBR of the lower priority logical channel(s); 2> decrement B_j by the total size of MAC SDUs served to logical channel j above; 2> if any resources remain, all the logical channels selected in clause 5.4.3.1.2 are served in a strict decreasing priority order (regardless of the value of B_j) until either the data for that logical channel or the UL grant is exhausted, whichever comes first. Logical channels configured with equal priority should be served equally.

[0170] In some implementations, if multiple LCHs have delay critical data with $B_j > 0$, the UE 104 may prioritize transmissions of data of one or more LCHs among the multiple LCHs further based on the target logical channel priorities of the multiple LCHs.

[0171] In some implementations, if multiple LCHs have delay critical data with $B_j > 0$, the UE 104 may prioritize transmissions of data of one or more LCHs among the multiple LCHs further based on the original logical channel priorities of the multiple LCHs.

[0172] For example, both the first LCH and a fifth LCH have delay critical data with $B_j > 0$. The UE 104 may prioritize transmissions of the data of the first LCH and the data of the fifth LCH in a decreasing order of a priority level for the first LCH and a priority level for the fifth LCH.

- [0173] If the priority level for the first LCH is higher than the priority level for the fifth LCH, the UE 104 may prioritize the transmission of the data of the first LCH. If the priority level for the first LCH is lower than the priority level for the fifth LCH, the UE 104 may prioritize the transmission of the data of the fifth LCH. The priority levels for the first LCH and the fifth LCH may be the original logical channel priorities or increased logical channel priorities.
- [0174] Consider a third example. In the third example, LCH#1 has a priority level of 1 (represented by priority 1), LCH#2 has a priority level of 2 (represented by priority 2), LCH#3 has a priority level of 3 (represented by priority 3), LCH#4 has a priority level of 4 (represented by priority 4). Priority 1 is higher than priority 2, priority 2 is higher than priority 3, and priority 3 is higher than priority 4. In other words, a value of priority 1 < a value of priority 2 < a value of priority 3 < a value of priority 4.
- [0175] In the third example, LCH#2 has delay critical data, and LCH#3 has delay critical data. LCH#1 and LCH#4 has not delay critical data. That is, LCH#2 and LCH#3 are LCHs with delay critical data, LCH#1 and LCH#4 are LCHs without delay critical data.
- [0176] In order to prioritize transmissions of data of LCH#2 and LCH#3, the UE 104 may increase priority levels for all the data of LCH#2 and LCH#3.
- [0177] In turn, the UE 104 may allocate resources for all the data of LCH#2 and LCH#3 first. Because the original logical channel priority for LCH#2 (i.e., priority 2) is higher than the original logical channel priority for LCH#3 (i.e., priority 3), the UE 104 may allocate resources for all the data of LCH#2 and LCH#3 in an decreasing order of priority 2 and priority 3. That is, the UE 104 may allocate resources for all the data of LCH#2 first and then allocate resources for all the data of LCH#3.
- [0178] Then, the UE 104 may allocate resources for data of LCH#1 and for data of LCH#4 in a decreasing order of priority 1 and priority 4.
- [0179] In the third example, the UE 104 may perform the procedure as shown in Table 3 below.

Table 3

The MAC entity shall, when a new transmission is performed:

1> allocate resources to the logical channels as follows:

2> logical channels **with delay critical data** selected in clause 5.4.3.1.2 for the UL grant with $B_j > 0$ are allocated resources **in decreasing order of priority**. If the PBR of a logical channel is set to *infinity*, the MAC entity shall allocate resources for all the data that is available for transmission on the logical channel before meeting the PBR of the lower priority logical channel(s);

2> logical channels **without delay critical data** selected in clause 5.4.3.1.2 for the UL grant with $B_j > 0$ are allocated resources **in decreasing order of priority**. If the PBR of a logical channel is set to *infinity*, the MAC entity shall allocate resources for all the data that is available for transmission on the logical channel before meeting the PBR of the lower priority logical channel(s);

2> decrement B_j by the total size of MAC SDUs served to logical channel j above;

2> if any resources remain, all the logical channels selected in clause 5.4.3.1.2 are served in a strict decreasing priority order (regardless of the value of B_j) until either the data for that logical channel or the UL grant is exhausted, whichever comes first. Logical channels configured with equal priority should be served equally.

[0180] In some implementations, if multiple LCHs have delay critical data with $B_j > 0$, the UE 104 may prioritize transmissions of data of one or more LCHs among the multiple LCHs further based on remaining time of data of the multiple LCHs.

[0181] For example, both the first LCH and a fifth LCH have delay critical data with $B_j > 0$. The UE 104 may prioritize transmissions of the data of the first LCH and the data of the fifth LCH in an increasing order of remaining time of data of the first LCH and remaining time of data of the fifth LCH. For example, remaining time of data of the first LCH is equal to 2ms, and remaining time of data of the first LCH is equal to 4ms. The UE 104 may prioritize the transmission of the data of the first LCH.

[0182] In some implementations, if multiple LCHs have delay critical data with $B_j > 0$, the UE 104 may prioritize transmissions of data of one or more LCHs among the multiple LCHs further based on remaining time of data of the multiple LCHs and the original logical channel priorities of the multiple LCHs.

[0183] For example, the UE 104 may prioritize transmissions of data of the one or more LCHs in a decreasing order of priority levels for the one or more LCHs first, and then prioritize transmissions of data of the one or more LCHs in an increasing order of remaining time of data of the one or more LCHs.

[0184] Alternatively, the UE 104 may prioritize transmissions of data of the one or more LCHs in an increasing order of remaining time of data of the one or more LCHs first, and then prioritize transmissions of data of the one or more LCHs in a decreasing order of priority levels for the one or more LCHs.

[0185] As described above, in some implementations, the UE 104 may prioritize the transmission of the data of the first LCH by increasing the first priority level for the first type of data of the first LCH to a target priority level.

[0186] In some implementations, the target priority level is higher than one or more priority levels for a group of one or more LCHs.

[0187] In some implementations, each of the one or more LCHs in the group may be not associated with a triggered DSR. In such implementations, each of the one or more LCHs in the group may be an LCH without delay critical data.

[0188] Alternatively, each of the one or more LCHs in the group may be associated with a triggered DSR and remaining time of data of each of the one or more LCHs in the group may be equal to or greater than a remaining time threshold. In such implementations, each of the one or more LCHs in the group may be an LCH with non-delay critical data.

[0189] In some implementations, the target priority level is higher than or equal to a third priority level for a third LCH, and the group of one or more LCHs excludes the third LCH. In such implementations, even if the increased priority level (i.e., the target priority level) for the delay critical data of the first LCH is equal to or higher than an original priority for the third LCH which is configured or indicated by the base station 102, the UE 104 may still consider the original priority for the third LCH is higher than the target

priority level for the delay critical data. Thus, the UE 104 will not prioritize transmission of the delay critical data of the first LCH over data or singling of the third LCH.

[0190] In some implementations, the third LCH may comprise an LCH having at least one signaling radio bearer (SRB). The at least one SRB may comprise at least one of the following: SRB0, SRB1, SRB2, SRB3, or SRB4.

[0191] In some implementations, the third LCH may be configured or indicated by the base station 102 or predefined.

[0192] In some implementations, the target priority level is lower than a fourth priority level for a fourth LCH. In some implementations, the fourth LCH may not have delay critical data but have important data.

[0193] For example, LCH#1 is configured with a priority 1 by the base station 102, LCH#2 is configured with a priority 2 by the base station 102, where priority 1 > priority 2. LCH#1 has very important data. For example, LCH#1 has some RRC signaling but has no delay critical data. LCH#2 has delay critical data. Thus, an original priority level for the data of LCH#2 is equal to priority 2. Even if LCH#2 has delay critical data and LCH#1 has no delay critical data, the UE 104 may not increase the priority level (i.e., priority 2) for the data of LCH#2 to a target priority level which is higher than the priority (i.e., priority 1) for LCH#1. Therefore, the increased priority level is restricted to some range.

[0194] In some implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on an absolute priority value. In such implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH to the absolute priority value. For example, the absolute priority value may be an absolute priority value for the first type of data.

[0195] In some implementations, the absolute priority may be configured by the base station 102 or predefined.

[0196] Alternatively or additionally, in some implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on a priority offset value. In such implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of

the first LCH by the priority offset value. For example, the priority offset value may be a priority offset value for the first type of data.

[0197] In some implementations, the priority offset value may be configured by the base station 102 or predefined.

[0198] Alternatively or additionally, in some implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on a factor. For example, the UE 104 may determine a target priority level based on the following: floor (factor * the first priority level), where “floor” represents a rounding down operation. The factor may be a factor for the first type of data.

[0199] Alternatively or additionally, in some implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on mapping between the factor and remaining time of the first type of data. The mapping between the factor and remaining time may be configured by the base station 102.

[0200] In some implementations, the UE 104 may receive a Layer 1, Layer 2 or Layer 3 signaling which comprises at least one of the following: the absolute priority value, the priority offset value, or the factor.

[0201] In some implementations, as shown in Fig. 5, the UE 104 may determine 540 a value which is maintained for the first LCH. In turn, the UE 104 may prioritize the transmission of the data of the first LCH based on the delay status of the data and the value which is maintained for the first LCH. As used herein, a value which is maintained for an LCH j is represented by B_j .

[0202] Hereinafter, some implementations of determination of the value which is maintained for the first LCH will be described by taking determination of B_j for an LCH j for example.

[0203] In some implementations, the UE 104 may determine B_j based on at least one LCP configuration for LCH j .

[0204] In some implementations, the at least one LCP configuration comprises a dedicated or new LCP configuration, and the dedicated LCP configuration comprises at least one of the following: a second PBR or a second BSD.

[0205] In some implementations, the at least one LCP configuration further comprises a first or legacy LCP configuration, and the first LCP configuration comprises a first PBR and a first BSD. The first PBR is separate from the second PBR, and the first BSD is separate from the second BSD.

[0206] In some implementations, the UE 104 may determine B_j according to the first or legacy LCP configuration comprising the first PBR and the first BSD. For example, the UE 104 increments B_j by the $\text{PBR} \times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented. The UE 104 determines B_j based on a bucket size, where the bucket size = first PBR $\times$ first BSD. If the value of B_j is greater than the bucket size (i.e., $\text{PBR} \times \text{BSD}$), the UE 104 sets B_j to the bucket size.

[0207] Alternatively, in some implementations, the UE 104 may determine B_j according to the dedicated or new LCP configuration. For example, the UE 104 increments B_j by the second PBR $\times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented. The PBR may be the first PBR or the second PBR. The UE determines B_j based on the bucket size, where the bucket size = second PBR $\times$ second BSD. If the value of B_j is greater than the bucket size (i.e., $\text{PBR} \times \text{BSD}$), the UE 104 sets B_j to the bucket size.

[0208] Alternatively, in some implementations, the UE 104 may determine B_j according to the dedicated LCP configuration and the first LCP configuration. For example, the UE 104 increments B_j by the second PBR $\times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented. The PBR may be the first PBR or the second PBR. The UE 104 determines the bucket size. For example, the bucket size = first PBR $\times$ second BSD, or the bucket size = second PBR $\times$ first BSD.

[0209] Table 4 gives some examples of determinations of B_j and the bucket size.

Table 4

	B_j	Bucket Size
1	First PBR $\times T$	First PBR, second BSD
2	First PBR $\times T$	second PBR, First BSD
3	First PBR $\times T$	second PBR, second BSD
4	second PBR $\times T$	First PBR, second BSD
5	second PBR $\times T$	second PBR, First BSD

6	second PBR *T	second PBR, second BSD
7	second PBR *T	First PBR, First BSD

[0210] Alternatively, in some implementations, the UE 104 may determine B_j based on a size of delay critical data of LCH j .

[0211] In some implementations, if B_j is less than the size of delay critical data, the UE 104 may determine B_j as the size of delay critical data. In other words, the UE 104 may increase B_j to the size of delay critical data. For example, the UE 104 may perform the procedure as shown in Table 5.

Table 5

For each logical channel j , the MAC entity shall: 1>increment B_j by the product $PBR \times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented; 1> if the value of B_j is smaller than size of the delay critical data: 2>set B_j to the size. 1> if the value of B_j is greater than the bucket size (i.e. $PBR \times BSD$): 2> set B_j to the bucket size.
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[0212] In some implementations, if the size of delay critical data is greater than a bucket size associated with LCH j , the UE 104 may determine the bucket size as the size of delay critical data. In turn, the UE 104 may determine B_j based on the bucket size. In such implementations, the UE 104 may increase bucket size to the size of delay critical data. For example, the UE 104 may perform the procedure as shown in Table 6.

Table 6

For each logical channel j , the MAC entity shall: 1>increment B_j by the product $PBR \times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented; 1> if the size of the delay critical data is greater than bucket size: 2>set the bucket size to the size. 1> if the value of B_j is greater than the bucket size: 2> set B_j to the bucket size.
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[0213] In some implementations, if B_j is less than the size of delay critical data and a bucket size associated with LCH j is less than the size of delay critical data, the UE 104 may determine B_j as the size of delay critical data and determine the bucket size as the size of delay critical data. For example, the UE 104 may perform the procedure as shown in Table 7.

Table 7

For each logical channel j , the MAC entity shall: 1> increment B_j by the product $PBR \times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented; 1> if the value of B_j is smaller than size of the data with the delay is lower than a delay threshold: 2> set B_j to the size. 1> if the size of the data with the remaining delay is lower than a delay threshold is greater than bucket size: 2> set the bucket size to the size. 1> if the value of B_j is greater than the bucket size: 2> set B_j to the bucket size.

[0214] In some implementations, the UE 104 may receive, from the base station 102, a configuration for a bucket size associated with LCH j . In turn, the UE 104 may determine B_j based on the bucket size. In such implementations, the bucket size is also referred to as a separate bucket size.

[0215] In some implementations, the UE 104 may receive, from the base station 102, an LCP configuration which comprises the separate bucket size.

[0216] In some implementations, the separate bucket size may be configured per LCH, DRB or QoS flow. The UE 104 may determine B_j based on the separate bucket size.

[0217] In some implementations, the separate bucket size may be configured for an LCH. For example, the LCH carries data in a PDU set or data burst.

[0218] In some implementations, the separate bucket size may be configured separately for high importance PDU set and low importance PDU set.

[0219] For example, the MAC entity of the UE 104 shall initialize B_j of an LCH to the separate bucket size when the LCH is established.

[0220] For another example, for each LCH j , the MAC entity shall increment B_j by the product $PBR \times T$ before every instance of the LCP procedure, where T is the time elapsed since B_j was last incremented. If B_j is greater than the separate bucket size, and optionally if there is delay critical data of the LCH j , the MAC entity sets B_j to the separate bucket size.

[0221] In some implementations, the UE 104 may determine a bucket size based on a first size of a PDU Set comprising delay critical data or a second size of a data burst comprising delay critical data. In turn, the UE 104 may determine B_j based on the first size and the second size. For example, if LCH j has delay critical data, the UE 104 may determine B_j based on the first size of the PDU Set or the second size of the data burst.

[0222] In some implementations, if the first size of the PDU Set or the second size of the data burst is greater than a bucket size, the UE 104 may set the bucket size to the first size of the PDU Set or the second size of the data burst.

[0223] In some implementations, if PDU set discard is configured for a data radio bearer (DRB) of the data of the first LCH, the UE 104 may prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0224] In some implementations, if the PDU set discard is activated for the DRB of the data of the first LCH, the UE 104 may prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0225] In some implementations, if the PDU set discard is deactivated for the DRB of the data of the first LCH, the UE 104 may prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0226] In some implementations, if the first type of data of the first LCH has high importance, the UE 104 may prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0227] In some implementations, if PDU set importance (PSI) based discard is configured for the DRB of the data of the first LCH, the UE 104 may prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0228] In some implementations, if the PSI based discard is activated for the DRB of the data of the first LCH, the UE 104 may prioritize the transmission of the data of the first LCH based on the first delay status of the data.

[0229] In some implementations, if the PSI based discard is deactivated for the DRB of the data of the first LCH.

[0230] In some implementations, the UE 104 may prioritize the transmission of the data of the first LCH based on the first delay status of the data regardless of a value which is maintained for the first LCH. In such implementations, during the second round of resource allocation procedure, the UE 104 may increase a first priority level for the first type of data of the first LCH to a target priority level or increase a priority level for the data of the first LCH to a target priority level. Then, the UE 104 may allocate resources to the logical channels selected for the UL grant in a decreasing priority order. During which round of resource allocation procedure to increase the priority, it may be configured by the base station 102. The implementations of increasing the first priority level for the first type of data or priority level for the data of the first LCH as described above may be applied to such implementations.

[0231] In some implementations, regardless that the UE 104 increases the priority level for at least the data with remaining time lower than remaining time threshold or not, the UE 104 may maximize the transmission for at least the delay critical data during the UE 104 allocates resources to the logical channels selected for the UL grant. This enhancement of such implementations may be configured by the base station 102.

[0232] In some implementations, based on B_j , the UE 104 allocates resources to the logical channels selected for the UL grant in a decreasing priority order. Some implementations of determining B_j have been described as above.

[0233] In some implementations, the UE 104 may prioritize the transmission of at least delay critical data over non-delay critical data as possible during the UE 104 allocates resources to the logical channels selected for the UL grant if the delay critical data fits into the resources of the associated MAC entity. This enhancement of such implementations may be configured by the base station 102.

[0234] In some implementations, during the first resource allocation round for the LCHs with B_j , if there is delay critical data of an LCH, the UE 104 shall allocate resources for at least the delay critical data that is available for transmission on the logical channel before meeting the PBR of the lower priority logical channel(s), i.e., regardless of B_j of the LCH, the UE 104 allocates the resource for all delay critical data of the LCH or for

all data of the LCH having the delay critical data as possible. For example, the UE 104 may perform the procedure as shown in Table 8.

Table 8

The UE shall also follow the rules below during the scheduling procedures above: - the UE should prioritize the transmission of at least delay critical data over non-delay critical data as possible if the delay critical data fits into the resources of the associated MAC entity and UE is configured to prioritize based on delay status. - the UE should not segment an RLC SDU (or partially transmitted SDU or retransmitted RLC PDU) if the whole SDU (or partially transmitted SDU or retransmitted RLC PDU) fits into the remaining resources of the associated MAC entity; - if the UE segments an RLC SDU from the logical channel, it shall maximize the size of the segment to fill the grant of the associated MAC entity as much as possible; - the UE should maximise the transmission of data; - if the MAC entity is given a UL grant size that is equal to or larger than 8 bytes (when eLCID is not used) or 10 bytes (when eLCID is used) while having data available and allowed (according to clause 5.4.3.1) for transmission, the MAC entity shall not transmit only padding BSR and/or padding.
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[0235] Fig. 6 illustrates a signaling chart illustrating an example process 600 that supports logical channel prioritization in accordance with aspects of the present disclosure. For the purpose of discussion, the process 600 will be described with reference to Fig. 1. The process 600 may involve the UE 104 and the base station 102 in Fig. 1.

[0236] As shown in Fig. 6, the UE 104 receives 610, from the base station 102, a command indicating to prioritize transmission of data of a first LCH.

[0237] In some implementations, the UE 104 may receive the command via a Layer 1, Layer 2 or Layer 3 signaling.

[0238] The UE 104 prioritizes 620 transmission of the data of the first LCH based on the command.

[0239] In some implementations, the command may indicate to prioritize the transmission of the data of the first LCH by indicating to increase a first priority level for a first type of data of the first LCH to a target priority level. First remaining time of the first type of data is below a remaining time threshold. In such implementations, the command may indicate to increase the first priority level for delay critical data of the first LCH to the target priority level. In such implementations, the UE 104 may determine the first remaining time of the first type of data.

[0240] In some implementations, the command may indicate to prioritize the transmission of the data of the first LCH by indicating to increase a priority level for the data of the first LCH to a target priority level. In such implementations, the command may indicate to increase the priority level for all the data of the first LCH to the target priority level.

[0241] In some implementations, the command may indicate information to determine the target priority level.

[0242] In some implementations, the command may indicate the target priority level.

[0243] In some implementations, the command may indicate the target priority level by indicating an absolute priority value. In some implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on the absolute priority value. In such implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH to the absolute priority value. For example, the absolute priority value may be an absolute priority value for the first type of data.

[0244] Alternatively or additionally, in some implementations, the command may indicate the target priority level by indicating a priority offset value. In such implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on the priority offset value. In such implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH by the priority offset value. For example, the priority offset value may be a priority offset value for the first type of data.

[0245] Alternatively or additionally, in some implementations, the command may indicate the target priority level by indicating a factor. In such implementations, the UE

104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on the factor. For example, the UE 104 may determine a target priority level based on the following: floor (factor * the first priority level), where “floor” represents a rounding down operation. The factor may be a factor for the first type of data.

[0246] Alternatively or additionally, in some implementations, the UE 104 may increase the first priority level for the first type of data of the first LCH or for the data of the first LCH based on mapping between the factor and remaining time of the first type of data. The mapping between the factor and remaining time may be configured by the base station 102.

[0247] It shall be noted that the implementations as described with reference to Figs. 1 to 5 are also applicable to the process 600. Details of the implementations are omitted for brevity.

[0248] Fig. 7 illustrates an example of a device 700 that supports logical channel prioritization in accordance with aspects of the present disclosure. The device 700 may be an example of a network entity 102 or a UE 104 as described herein. The device 700 may support wireless communication with one or more network entities 102, UEs 104, or any combination thereof. The device 700 may include components for bi-directional communications including components for transmitting and receiving communications, such as a processor 702, a memory 704, a transceiver 706, and, optionally, an I/O controller 708. These components may be in electronic communication or otherwise coupled (e.g., operatively, communicatively, functionally, electronically, electrically) via one or more interfaces (e.g., buses).

[0249] The processor 702, the memory 704, the transceiver 706, or various combinations thereof or various components thereof may be examples of means for performing various aspects of the present disclosure as described herein. For example, the processor 702, the memory 704, the transceiver 706, or various combinations or components thereof may support a method for performing one or more of the operations described herein.

[0250] In some implementations, the processor 702, the memory 704, the transceiver 706, or various combinations or components thereof may be implemented in hardware (e.g., in communications management circuitry). The hardware may include a processor,

a digital signal processor (DSP), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA) or other programmable logic device, a discrete gate or transistor logic, discrete hardware components, or any combination thereof configured as or otherwise supporting a means for performing the functions described in the present disclosure. In some implementations, the processor 702 and the memory 704 coupled with the processor 702 may be configured to perform one or more of the functions described herein (e.g., executing, by the processor 702, instructions stored in the memory 704).

[0251] For example, the processor 702 may support wireless communication at the device 700 in accordance with examples as disclosed herein. The processor 702 may be configured to operable to support a means for performing the following: determining first delay status of data of a first LCH; and prioritizing transmission of the data of the first LCH based on the first delay status of the data.

[0252] Alternatively, in some implementations, the processor 702 may be configured to operable to support a means for performing the following: receiving, from a base station, a command indicating to prioritize transmission of data of a first LCH; and prioritizing the transmission of the data of the first LCH based on the command.

[0253] The processor 702 may include an intelligent hardware device (e.g., a general-purpose processor, a DSP, a CPU, a microcontroller, an ASIC, an FPGA, a programmable logic device, a discrete gate or transistor logic component, a discrete hardware component, or any combination thereof). In some implementations, the processor 702 may be configured to operate a memory array using a memory controller. In some other implementations, a memory controller may be integrated into the processor 702. The processor 702 may be configured to execute computer-readable instructions stored in a memory (e.g., the memory 704) to cause the device 700 to perform various functions of the present disclosure.

[0254] The memory 704 may include random access memory (RAM) and read-only memory (ROM). The memory 704 may store computer-readable, computer-executable code including instructions that, when executed by the processor 702 cause the device 700 to perform various functions described herein. The code may be stored in a non-transitory computer-readable medium such as system memory or another type of memory. In some implementations, the code may not be directly executable by the processor 702 but may cause a computer (e.g., when compiled and executed) to perform functions

described herein. In some implementations, the memory 704 may include, among other things, a basic I/O system (BIOS) which may control basic hardware or software operation such as the interaction with peripheral components or devices.

[0255] The I/O controller 708 may manage input and output signals for the device 700. The I/O controller 708 may also manage peripherals not integrated into the device M02. In some implementations, the I/O controller 708 may represent a physical connection or port to an external peripheral. In some implementations, the I/O controller 708 may utilize an operating system such as iOS®, ANDROID®, MS-WINDOWS®, OS/2®, UNIX®, LINUX®, or another known operating system. In some implementations, the I/O controller 708 may be implemented as part of a processor, such as the processor 706. In some implementations, a user may interact with the device 700 via the I/O controller 708 or via hardware components controlled by the I/O controller 708.

[0256] In some implementations, the device 700 may include a single antenna 710. However, in some other implementations, the device 700 may have more than one antenna 710 (i.e., multiple antennas), including multiple antenna panels or antenna arrays, which may be capable of concurrently transmitting or receiving multiple wireless transmissions. The transceiver 706 may communicate bi-directionally, via the one or more antennas 710, wired, or wireless links as described herein. For example, the transceiver 706 may represent a wireless transceiver and may communicate bi-directionally with another wireless transceiver. The transceiver 706 may also include a modem to modulate the packets, to provide the modulated packets to one or more antennas 710 for transmission, and to demodulate packets received from the one or more antennas 710. The transceiver 706 may include one or more transmit chains, one or more receive chains, or a combination thereof.

[0257] A transmit chain may be configured to generate and transmit signals (e.g., control information, data, packets). The transmit chain may include at least one modulator for modulating data onto a carrier signal, preparing the signal for transmission over a wireless medium. The at least one modulator may be configured to support one or more techniques such as amplitude modulation (AM), frequency modulation (FM), or digital modulation schemes like phase-shift keying (PSK) or quadrature amplitude modulation (QAM). The transmit chain may also include at least one power amplifier configured to

amplify the modulated signal to an appropriate power level suitable for transmission over the wireless medium. The transmit chain may also include one or more antennas 710 for transmitting the amplified signal into the air or wireless medium.

[0258] A receive chain may be configured to receive signals (e.g., control information, data, packets) over a wireless medium. For example, the receive chain may include one or more antennas 710 for receive the signal over the air or wireless medium. The receive chain may include at least one amplifier (e.g., a low-noise amplifier (LNA)) configured to amplify the received signal. The receive chain may include at least one demodulator configured to demodulate the receive signal and obtain the transmitted data by reversing the modulation technique applied during transmission of the signal. The receive chain may include at least one decoder for decoding the processing the demodulated signal to receive the transmitted data.

[0259] Fig. 8 illustrates an example of a processor 800 that supports logical channel prioritization in accordance with aspects of the present disclosure. The processor 800 may be an example of a processor configured to perform various operations in accordance with examples as described herein. The processor 800 may include a controller 802 configured to perform various operations in accordance with examples as described herein. The processor 800 may optionally include at least one memory 804, such as L1/L2/L3 cache. Additionally, or alternatively, the processor 800 may optionally include one or more arithmetic-logic units (ALUs) 806. One or more of these components may be in electronic communication or otherwise coupled (e.g., operatively, communicatively, functionally, electronically, electrically) via one or more interfaces (e.g., buses).

[0260] The processor 800 may be a processor chipset and include a protocol stack (e.g., a software stack) executed by the processor chipset to perform various operations (e.g., receiving, obtaining, retrieving, transmitting, outputting, forwarding, storing, determining, identifying, accessing, writing, reading) in accordance with examples as described herein. The processor chipset may include one or more cores, one or more caches (e.g., memory local to or included in the processor chipset (e.g., the processor 800) or other memory (e.g., random access memory (RAM), read-only memory (ROM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), static RAM (SRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, phase change memory (PCM), and others).

[0261] The controller 802 may be configured to manage and coordinate various operations (e.g., signaling, receiving, obtaining, retrieving, transmitting, outputting, forwarding, storing, determining, identifying, accessing, writing, reading) of the processor 800 to cause the processor 800 to support various operations in accordance with examples as described herein. For example, the controller 802 may operate as a control unit of the processor 800, generating control signals that manage the operation of various components of the processor 800. These control signals include enabling or disabling functional units, selecting data paths, initiating memory access, and coordinating timing of operations.

[0262] The controller 802 may be configured to fetch (e.g., obtain, retrieve, receive) instructions from the memory 804 and determine subsequent instruction(s) to be executed to cause the processor 800 to support various operations in accordance with examples as described herein. The controller 802 may be configured to track memory address of instructions associated with the memory 804. The controller 802 may be configured to decode instructions to determine the operation to be performed and the operands involved. For example, the controller 802 may be configured to interpret the instruction and determine control signals to be output to other components of the processor 800 to cause the processor 800 to support various operations in accordance with examples as described herein. Additionally, or alternatively, the controller 802 may be configured to manage flow of data within the processor 800. The controller 802 may be configured to control transfer of data between registers, arithmetic logic units (ALUs), and other functional units of the processor 800.

[0263] The memory 804 may include one or more caches (e.g., memory local to or included in the processor 800 or other memory, such RAM, ROM, DRAM, SDRAM, SRAM, MRAM, flash memory, etc. In some implementation, the memory 804 may reside within or on a processor chipset (e.g., local to the processor 800). In some other implementations, the memory 804 may reside external to the processor chipset (e.g., remote to the processor 800).

[0264] The memory 804 may store computer-readable, computer-executable code including instructions that, when executed by the processor 800, cause the processor 800 to perform various functions described herein. The code may be stored in a non-transitory computer-readable medium such as system memory or another type of memory. The

controller 802 and/or the processor 800 may be configured to execute computer-readable instructions stored in the memory 804 to cause the processor 800 to perform various functions. For example, the processor 800 and/or the controller 802 may be coupled with or to the memory 804, the processor 800, the controller 802, and the memory 804 may be configured to perform various functions described herein. In some examples, the processor 800 may include multiple processors and the memory 804 may include multiple memories. One or more of the multiple processors may be coupled with one or more of the multiple memories, which may, individually or collectively, be configured to perform various functions herein.

[0265] The one or more ALUs 806 may be configured to support various operations in accordance with examples as described herein. In some implementation, the one or more ALUs 806 may reside within or on a processor chipset (e.g., the processor 800). In some other implementations, the one or more ALUs 806 may reside external to the processor chipset (e.g., the processor 800). One or more ALUs 806 may perform one or more computations such as addition, subtraction, multiplication, and division on data. For example, one or more ALUs 806 may receive input operands and an operation code, which determines an operation to be executed. One or more ALUs 806 be configured with a variety of logical and arithmetic circuits, including adders, subtractors, shifters, and logic gates, to process and manipulate the data according to the operation. Additionally, or alternatively, the one or more ALUs 806 may support logical operations such as AND, OR, exclusive-OR (XOR), not-OR (NOR), and not-AND (NAND), enabling the one or more ALUs 806 to handle conditional operations, comparisons, and bitwise operations.

[0266] The processor 800 may support wireless communication in accordance with examples as disclosed herein. The processor 800 may be configured to operable to support a means for performing the following: determining first delay status of data of a first LCH; and prioritizing transmission of the data of the first LCH based on the first delay status of the data.

[0267] Alternatively, in some implementations, the processor 800 may be configured to operable to support a means for performing the following: receiving, from a base station, a command indicating to prioritize transmission of data of a first LCH; and prioritizing the transmission of the data of the first LCH based on the command.

[0268] Fig. 9 illustrates a flowchart of a method 900 that supports logical channel prioritization in accordance with aspects of the present disclosure. The operations of the method 900 may be implemented by a device or its components as described herein. For example, the operations of the method 900 may be performed by the UE 104 as described herein. In some implementations, the device may execute a set of instructions to control the function elements of the device to perform the described functions. Additionally, or alternatively, the device may perform aspects of the described functions using special-purpose hardware.

[0269] At 910, the method may include determining first delay status of data of a first LCH. The operations of 910 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 910 may be performed by a device as described with reference to Fig. 1.

[0270] At 920, the method may include prioritizing transmission of the data of the first LCH based on the first delay status of the data. The operations of 920 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 920 may be performed by a device as described with reference to Fig. 1.

[0271] Fig. 10 illustrates a flowchart of a method 1000 that supports logical channel prioritization in accordance with aspects of the present disclosure. The operations of the method 1000 may be implemented by a device or its components as described herein. For example, the operations of the method 1000 may be performed by the UE 104 as described herein. In some implementations, the device may execute a set of instructions to control the function elements of the device to perform the described functions. Additionally, or alternatively, the device may perform aspects of the described functions using special-purpose hardware.

[0272] At 1010, the method may include receiving, from a base station, a command indicating to prioritize transmission of data of a first LCH. The operations of 1010 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 1010 may be performed by a device as described with reference to Fig. 1.

[0273] At 1020, the method may include prioritizing the transmission of the data of the first LCH based on the command. The operations of 1020 may be performed in

accordance with examples as described herein. In some implementations, aspects of the operations of 1020 may be performed by a device as described with reference to Fig. 1.

[0274] It shall be noted that implementations of the present disclosure which have been described with reference to Figs. 1 to 6 are also applicable to the device 700, the processor 800 and the methods 900, 1000.

[0275] It should be noted that the methods described herein describes possible implementations, and that the operations and the steps may be rearranged or otherwise modified and that other implementations are possible. Further, aspects from two or more of the methods may be combined.

[0276] The various illustrative blocks and components described in connection with the disclosure herein may be implemented or performed with a general-purpose processor, a DSP, an ASIC, a CPU, an FPGA or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices (e.g., a combination of a DSP and a microprocessor, multiple microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0277] The functions described herein may be implemented in hardware, software executed by a processor, firmware, or any combination thereof. If implemented in software executed by a processor, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Other examples and implementations are within the scope of the disclosure and appended claims. For example, due to the nature of software, functions described herein may be implemented using software executed by a processor, hardware, firmware, hardwiring, or combinations of any of these. Features implementing functions may also be physically located at various positions, including being distributed such that portions of functions are implemented at different physical locations.

[0278] Computer-readable media includes both non-transitory computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A non-transitory storage medium may be

any available medium that may be accessed by a general-purpose or special-purpose computer. By way of example, non-transitory computer-readable media may include RAM, ROM, electrically erasable programmable ROM (EEPROM), flash memory, compact disk (CD) ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other non-transitory medium that may be used to carry or store desired program code means in the form of instructions or data structures and that may be accessed by a general-purpose or special-purpose computer, or a general-purpose or special-purpose processor.

[0279] As used herein, including in the claims, an article “a” before an element is unrestricted and understood to refer to “at least one” of those elements or “one or more” of those elements. The terms “a,” “at least one,” “one or more,” and “at least one of one or more” may be interchangeable. As used herein, including in the claims, “or” as used in a list of items (e.g., a list of items prefaced by a phrase such as “at least one of” or “one or more of” or “one or both of”) indicates an inclusive list such that, for example, a list of at least one of A, B, or C means A or B or C or AB or AC or BC or ABC (i.e., A and B and C). Also, as used herein, the phrase “based on” shall not be construed as a reference to a closed set of conditions. For example, an example step that is described as “based on condition A” may be based on both a condition A and a condition B without departing from the scope of the present disclosure. In other words, as used herein, the phrase “based on” shall be construed in the same manner as the phrase “based at least in part on. Further, as used herein, including in the claims, a “set” may include one or more elements.

[0280] The description herein is provided to enable a person having ordinary skill in the art to make or use the disclosure. Various modifications to the disclosure will be apparent to a person having ordinary skill in the art, and the generic principles defined herein may be applied to other variations without departing from the scope of the disclosure. Thus, the disclosure is not limited to the examples and designs described herein but is to be accorded the broadest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

1. A user equipment (UE), comprising:
a processor; and
a transceiver coupled to the processor,
wherein the processor is configured to:
determine first delay status of data of a first logical channel (LCH); and
prioritize transmission of the data of the first LCH based on the first delay status of the data.
2. The UE of claim 1, wherein the processor is configured prioritize transmission of the data of the first LCH based on the first delay status of the data by:
prioritize transmission of a first type of data of the first LCH, wherein the first delay status comprises first remaining time of the first type of data, the first remaining time of the first type of data is below a remaining time threshold.
3. The UE of claim 1 or 2, wherein the processor is configured prioritize transmission of the data of the first LCH based on the first delay status of the data by one of the following:
prioritizing transmission of the data of the first LCH over data of a second LCH,
or
prioritizing transmission of the first type of data of the first LCH over the data of the second LCH, or
prioritizing transmission of the first type of data of the first LCH over a second type of data of the first LCH, wherein the first delay status comprises second remaining time of the second type of data, the second remaining time of the second type of data is above the remaining time threshold.
4. The UE of claim 3, wherein the processor is configured prioritize transmission of the data of the first LCH based on the first delay status of the data by one of the following:
allocating resources for the data of the first LCH and the data of the second LCH in a decreasing order of priority levels of the first LCH and the second LCH; or

allocating resources for the first type of data of the first LCH and the data of the second LCH in a decreasing order of a first priority level for the first type of data and a priority level for the second LCH; or

allocating resources for the first type of data of the first LCH and the second type of data of the first LCH in a decreasing order of the first priority level for the first type of data and a second priority level for the second type of data.

5. The UE of claim 2, wherein the processor is configured to prioritize the transmission of the data of the first LCH by:

increasing a first priority level for the first type of data of the first LCH to a target priority level.

6. The UE of claim 1, wherein the processor is configured to prioritize the transmission of the data of the first LCH by:

increasing a priority level for the data of the first LCH to a target priority level.

7. The UE of claim 5 or 6, wherein the target priority level is higher than or equal to a third priority level for a third LCH, and a group of one or more LCHs excludes the third LCH.

8. The UE of claim 1 or 2, wherein:

the processor is further configured to:

determine second delay status of data of a fifth LCH, wherein the data of the fifth LCH comprises at least the first type of data, the second delay status comprises third remaining time of the first type of data of the fifth LCH, the third remaining time of the first type of data is below the remaining time threshold; and

the processor is configured to prioritize the transmission of the data of the first LCH by:

prioritizing the transmission of the data of the first LCH based on determining that a first priority level for the first LCH is higher than a fifth priority level for the fifth LCH.

9. The UE of claim 1, wherein the processor is configured to prioritize the transmission of the data of the first LCH by:

prioritizing the transmission of the data of the first LCH based on the delay status of the data and a value which is maintained for the first LCH.

10. The UE of claim 1, wherein the processor is configured to prioritize the transmission of the data of the first LCH based on the first delay status of the data based on determining one of the following:

protocol data unit (PDU) set discard is configured for a data radio bearer (DRB) of the data of the first LCH;

the PDU set discard is activated for the DRB of the data of the first LCH;

the PDU set discard is deactivated for the DRB of the data of the first LCH;

a first type of data of the first LCH has high importance;

PDU set importance (PSI) based discard is configured for the DRB of the data of the first LCH;

the PSI based discard is activated for the DRB of the data of the first LCH; or

the PSI based discard is deactivated for the DRB of the data of the first LCH.

11. The UE of claim 1, wherein the processor is configured to prioritize the transmission of the data of the first LCH based on the first delay status of the data regardless of a value which is maintained for the first LCH.

12. The UE of claim 11, wherein the data of the first LCH is a first type of data of the first LCH, wherein the first delay status comprises first remaining time of the first type of data, the first remaining time of the first type of data is below a remaining time threshold.

13. The UE of claim 1, wherein the processor is further configured to:

receive, via the transceiver from a base station, a first indication indicating whether to prioritize the transmission of the data of the first LCH based on the first delay status of the data.

14. A user equipment (UE), comprising:

a processor; and

a transceiver coupled to the processor,

wherein the processor is configured to:

receive, via the transceiver from a base station, a command indicating to prioritize transmission of data of a first logical channel (LCH); and
prioritize the transmission of the data of the first LCH based on the command.

15. The UE of claim 14, wherein the command indicates to prioritize the transmission of the data of the first LCH by indicating to increase a first priority level for a first type of data of the first LCH to a target priority level, wherein first remaining time of the first type of data is below a remaining time threshold.

16. The UE of claim 15, wherein the processor is further configured to:
determine the first remaining time of the first type of data.

17. The UE of claim 14, wherein the command indicates to prioritize the transmission of the data of the first LCH by indicating to increase a priority level for the data of the first LCH to a target priority level.

18. The UE of claim 15 or 17, wherein the command indicates information to determine the target priority level.

19. The UE of claim 18, wherein the command indicates the target priority level.

20. A base station, comprising:
a processor; and
a transceiver coupled to the processor,
wherein the processor is configured to:
receive, via the transceiver from a user equipment (UE), capability indicating whether to prioritize transmission of data of one or more logical channels (LCHs) based on delay status of the data; and
transmit, via the transceiver to the UE, an indication indicating whether to prioritize the transmission of the data of the one or more LCHs based on the delay status of the data.