METHODS FOR FABRICATING INTEGRATED CIRCUITS WITH RUTHENIUM-LINED COPPER

ABSTRACT

Methods for fabricating integrated circuits are provided. In an embodiment, a method for fabricating an integrated circuit includes depositing a dielectric layer defining a plane. In the method, the dielectric layer is etched to form trenches. Then, a ruthenium-containing liner layer is deposited overlying the dielectric layer. The trenches are filled with copper-containing metal. The method includes recessing the copper-containing metal in each trench to form a space between the copper-containing metal and the plane. The space is filled with a capping layer. The layers are then planarized to at least the plane.

Fig. 5