

The present invention relates to a power supply of the switched-mode AC/DC converter type, that is to say a power supply which, from a voltage delivered by an alternating mains, will supply a DC output voltage by using for that purpose an input rectifier circuit and, between this circuit and its output, switching means controlled as a function of the output voltage of the power supply in order to regulate this output voltage; moreover, this power supply must consume, from the mains, a sinusoidal current in phase with the voltage so as to optimize the power factor of the power supply, that is to say so that the ratio of the active power necessary over the apparent power consumed from the mains is substantially equal to 1.

Such power supplies exist and will be described with the aid of the attached Figure 1. In these known power supplies, which are said to be anharmonic switched-mode power supplies with forced switching, the switching is caused to occur at the moment when currents flow in the switching means; this results in switching losses, interference in the form of current spikes which are prejudicial to good working conditions for the components of the power supply, and interference by radiation. Moreover, these power supplies, which operate at maximum switching frequencies of the order of 200 kHz, are relatively bulky.

The object of the present invention is to avoid or, at least, to reduce these drawbacks.

A switched-mode power supply is known from the document JP-A-58,136,265, consisting of a four-pole network including, in series between its first input and its first output, a first inductor, a first switch, a first terminal of a first capacitor, a first terminal of a unidirectional conductor, a second switch, a second inductor and the first terminal of a second capacitor, the second terminals of the first and second switches and of the unidirectional conductor being coupled to the second input and the second output of the four-pole network, the two switches being, by means of a control

circuit, switched alternately.

The subject of the present invention is a power supply including switching means which are arranged and controlled at very high frequencies in such a way that the current which passes through them is zero at the moment when they are opened and that their volume is small, this power supply being such as defined by Claim 1.

Other subjects and other characteristics will become apparent with the aid of the description below, and of the figures relating thereto which represent:

- Figure 1, a simplified diagram of a power supply according to the prior art,

- Figure 2, a diagram of a power supply according to the invention.

Figure 1 is the simplified diagram of a power supply of the switched-mode AC/DC converter type according to the prior art.

A rectifier bridge P supplies, between its output terminals B1, B2, and from an alternating input voltage, v, a voltage formed by arches of rectified sinusoids. The terminal B1 is coupled by an inductor L followed by a diode D to one of the two output terminals S1, S2 of the power supply; a load R depicted by a resistor is branched between the terminals S1 S2; the diode is arranged to be conducting for the current rectified by the bridge P. The terminal B2 is linked to the terminal S2 via a resistor r. A capacitor Cs is branched between the terminals S1 S2. An electronic switch, T, depicted by a contact, is mounted between the point common to the inductor L and to the diode D, and the terminal S2. This switch is controlled by a first comparator 12, the "+" input of which is linked to the output of a multiplier circuit 11, and the "-" input of which is linked to the terminal S2. A second comparator 10 has its "+" input linked to the terminal S1 and its "-" input linked to a DC reference voltage V; the output of the comparator 10 is linked to one of the two inputs of the multiplier 11, the other input of which is linked to the terminal B1.

The comparator 12 compares the current which is flowing in the inductor L and thus in the resistor r, with a datum signal which is a rectified sinusoid of the same frequency as that of the mains and of amplitude proportional to the power to be transmitted; this datum signal is obtained by multiplying the value of the rectified voltage supplied by the rectifier bridge P, by the result of the comparison performed by the comparator 10 between the output voltage of the power supply and the reference voltage V.

As it is shown, the switch T opens and closes at a rate of 100 to 200 kHz; the value of this rate is determined on the basis of the value given to the inductor L; and the control of the switch T is set so that the envelope of the current in the inductor L is a rectified sinusoid.

With the layout according to Figure 1, the opening and closing of the switch T, which are forced by the state of the output of the comparator 12 and which occur although currents are flowing respectively in the switch T and in the diode D, entail switching losses and interference in the switch.

Figure 2 is the diagram of a switched-mode AC/DC converter type power supply, according to the invention.

A rectifier bridge P supplies, between its output terminals B1, B2, and from an alternating input voltage v, of 117 V and 400 Hz, delivered by a mains, a voltage formed by arches of rectified sinusoids. The terminal B1 is coupled by an inductor L_e to a first input terminal A1 of a four-pole network, the other input terminal of which bears the reference A2, and the output terminals the references A3 and A4. The terminal B2 is linked to the terminal A2 and is coupled to the terminal A1 via a capacitor C_e.

The terminal A1 is linked to the terminal A3 by a first unidirectional switch T1, followed by an inductor L1, followed by a second unidirectional switch T2, followed by an inductor L2. The unidirectional switches T1 and T2 are transistors controlled respectively by the

direct Q and inverted $\bar{Q}$ outputs of a monostable latch 3; they have been represented in Figure 2 by a contact in series with a diode: d1 for T1, d2 for T2.

5 The four-pole network has its input terminal A2 linked to the output terminal A4; these two terminals are coupled by a capacitor C1, a diode D1 and a capacitor C2 in parallel with a diode D2, respectively to the common point of the inductor L1 and of the switch T2, to the common point of the switch T2 and of the inductor L2 and
10 to the terminal A3.

The terminal A3 of the four-pole network is coupled to one, S1, of the two output terminals of the power supply via an inductor Ls. The terminal A4 of the four-pole network is linked to the terminal S2 of the
15 power supply and is coupled by a capacitor Cs to the terminal S1 of the power supply. A load R, depicted by a resistor, is branched between the terminals of the power supply. The inductor Ls, with the capacitor Cs, forms a low-pass filter which is arranged at the output of the
20 power supply.

A comparator 1 has its "+" input linked to the output terminal S1 of the power supply and its "-" input linked to a DC reference voltage source V.

The output of the comparator 1 is linked to the
25 control input of an oscillator circuit 2 which, as a function of its control signal, delivers pulses at a frequency capable of varying from 0 to 1 MHz. These pulses control the latching of the latch 3.

The monostable latch 3 has a duration of its
30 quasi-stable state which is fixed at 280 ns. For the duration of its quasi-stable state, it controls the closing of the switch T1 and the opening of the switch T2, and conversely when it is not in its quasi-stable state.

35 The current which flows in the switch T1 is a half-sinusoid of high frequency, the duration of which is determined by the resonance frequency of the oscillating circuit constituted by the elements L1, C1, and the amplitude of which is proportional to the instantaneous

value of the alternating input voltage, v . The envelope of the current thus follows, in phase, the rectified sinusoid of the input voltage.

5 The high-frequency input filter, constituted by the elements L_e , C_e makes it possible, by eliminating the high-frequency components of the current flowing in the switch T_1 , to keep only the sinusoidal envelope of the input current at the frequency, F , of the mains.

10 When the switch T_1 is closed, the capacitor C_1 charges sinusoidally, through the inductor L_1 up to twice the input voltage. This charging takes place at high frequency, the oscillating circuit L_1 - C_1 having a resonance frequency of 2 MHz. The charging of the capacitor C_1 is done over the duration of the quasi-stable state of
15 the latch 3 and this duration, equal to 280 ns, is greater than the half-period of the oscillating circuit L_1 - C_1 , that is to say than 250 ns; hence the capacitor C_1 has finished being charged at the moment when the switch T_1 is opened, that is to say that no current flows in
20 this switch at the moment when it is opened.

The role of the diode d_1 is to avoid the capacitor C_1 discharging, by preventing the current in the inductor L_1 being reversed.

25 Upon opening T_1 , the capacitor C_1 is charged; upon closing T_2 , which is simultaneous with the opening of T_1 , the energy stored in the capacitor C_1 is transferred, sinusoidally at high frequency, through the inductor L_2 , into the output load R and into the capacitor C_2 .

30 The diode d_2 prevents the current which flows in the inductor L_2 being reversed and thus recharging the capacitor C_1 .

35 The diode D_1 , by tapping off through it the current from the inductor L_2 , prevents the capacitor C_1 being discharged down to a negative voltage.

Likewise the diode D_2 , by tapping off through it the current from the inductor L_s , prevents the capacitor C_2 being charged negatively.

As long as, during a switching cycle, that is to

say over the duration of one consecutive closing and opening of the switch T1, the energy stored in the capacitor C1 remains less than that consumed by the load R, the capacitor C2 cannot be charged, as all the energy stored in the capacitor C1 is entirely consumed by the load R.

When, during one switching cycle, the energy stored in the capacitor C1 is greater than that consumed by the load R, the capacitor C2 is charged, storing the difference between these two energies and this energy stored in the capacitor C2 is consumed by the load R before any new charging of the capacitor C1, that is to say before a new switching cycle commences.

This way of regulating the output voltage from the power supply is achieved with the aid of the oscillating circuit 2, the frequency of which is controlled by the output voltage from the comparator 1 which plays the role of error amplifier by comparing the output voltage from the power supply with the reference voltage V; and, as was seen above, the pulses which the oscillating circuit 2 delivers control the closing of the switch T1 for 280 ns and the opening of the switch T2 for the same length of time.

It should be noted that the comparator 1 includes a low-pass filter on its "+" input, so as not to take account of the slight residual ripple at the frequency of the mains which the output of the power supply exhibits.

The present invention is not limited to the example described, thus, in particular, a linking transformer may be inserted into the four-pole network, downstream from the switch T1. Likewise, the unidirectional switches T1 and T2 may consist of two separate elements: a bidirectional switch and a semiconductor element, and, in this case, in Figure 2, the places occupied by the elements d1 and L1 may be exchanged.

Likewise, in the example described, the resonance frequency of the oscillating circuit L1-C1 has been chosen to have a very high value, with respect to that of

the alternating means, since there is a ratio of 5,000 between the two frequencies; the ratio between these two frequencies may be less high, while remaining higher than 1,000, on condition of reducing consequentially the maximum frequency which the oscillator circuit 2 can reach, and of setting the duration of the quasi-stable state of the monostable latch 3 in such a way that it remains at least equal to or just a little greater than the half-period of the oscillating circuit L1, C1.

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10 However, it should be noted that the power transmitted to the load will be commensurately all the higher as the number of times per second when the capacitor C1 is charged and discharged is high; this therefore leads, for a maximum switching frequency of the circuit 2 and for

15 the maximum desired power, to defining the values of L1 and C1.

CLAIMS

1. Power supply of the switched-mode AC/DC converter type, with a full-wave rectifier circuit (P), followed by a high-frequency filter (Le, Ce) coupled by a four-pole network to a low-frequency filter (Ls, Cs) delivering an output voltage, the four-pole network including, in series between its first input (A1) and its first output (A3), a first unidirectional switch (T1), a first inductor (L1), a first terminal of a first capacitor (C1), a second unidirectional switch (T2), a first terminal of a first unidirectional conductor (D1), a second inductor (L2) and a first terminal of a second capacitor (C2) and of a second unidirectional conductor (D2), the second terminals of the first and second capacitors and of the first and second unidirectional conductors being coupled to the second input (A2) and to the second output (A4) of the four-pole network, and the power supply including a monostable circuit (3) the quasi-stable state of which has a duration slightly longer than the inverse of the resonance frequency of the oscillating circuit (L1, C1) constituted by the first inductor and the first capacitor, for controlling the closing of the first switch and the opening of the second switch during its quasi-stable state and conversely outside its quasi-stable state and an oscillator circuit (2), controlled as a function of the output voltage, for supplying pulses for triggering the monostable circuit.

2. Power supply according to Claim 1, in which the rectifier circuit (P) is connected to mains supplying an alternating voltage of a given frequency, characterized in that the resonance frequency of the oscillating circuit (L1, C1) is more than a thousand times higher than the given frequency.

