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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Transistors and Methods of Making Same

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to transistors and methods of making the same and more particularly to transistors and methods of making the same in or on a semiconductor substrate.

The present invention is a transistor comprising an integral or integrated body of semiconductor material containing a semiconductor substrate, a monocrystalline collector region of one conductivity type in or on one face of said substrate, a diffused monocrystalline base region of opposite conductivity type contiguous with said collector region to form therewith a first P-N junction extending to one surface of said body and there defining a first enclosed area and a diffused monocrystalline emitter region of said one conductivity type contiguous with said base region to form therewith a second P-N junction extending to said one surface and there defining a second enclosed area surrounded by said first enclosed area, and ohmic connections to said collector, base and emitter regions.

The present invention is also a method of fabricating a transistor contained in an integral or integrated body of single crystal semiconductor material comprising the steps of: forming a collector region of one conductivity type in or on a semiconductor substrate, forming a base region of opposite conductivity type contiguous with said collector region to form therewith a P-N junction extending to one surface of said body and there defining a first enclosed area by diffusing a conductivity type producing ingredient into said collector region adapted to give said base region said opposite conductivity type, forming an emitter region of said one conductivity type contiguous with said base region to form therewith a second P-N junction extending to said one surface and there defining a second enclosed area surrounded by said first enclosed area by diffusing a conductivity type producing ingredient into said base region adapted to give said emitter region said one conductivity type, and providing ohmic connections to said collector, base and emitter regions.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawing, in which:—

Figs. 1 and 2 illustrate semiconductor devices embodying transistors according to the invention.

The transistors illustrated in Figs. 1 and 2 may be part of a semiconductor body containing other circuit elements as described in parent British Patent Application No. 16071/60 (Serial No. 958,242) from which the present application is divided.

The semiconductor device embodying the invention comprises a body of semiconductor material of single crystal structure which may be composed of any suitable semiconductor material such as germanium, silicon, intermetallic alloys such as gallium arsenide, aluminium antimonide, indium antimonide, as well as others.

Referring to Fig. 1, there is illustrated a semiconductor device embodying an NPN transistor including N-type collector region 18, P-type base region 20 and N-type-emitter regions 22 and 24. The device illustrated is a multi-emitter transistor; however, it

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actually includes one NPN transistor plus an integral diode formed by the additional emitter region.

The collector region 18 may be mounted or secured on a semiconductor substrate 10, for example, by solder glass. The semiconductor substrate 10 may be composed of intrinsic semiconductor material having a relatively high order of resistivity.

Ohmic contacts are made to the regions by metal contacts 33, 26, 28 and 30. The contacts 26, 28 and 30 may be plated or evaporated onto their respective regions. The collector contact 33 may be soldered or alloyed to substrate 10 and extends beneath the collector region 18 to make ohmic contact therewith.

The device may be constructed by providing an N-type wafer, diffusing a P-type conductivity producing ingredient into one surface of said wafer, selectively etching the semiconductor material to produce the shape illustrated in Fig. 1, selectively diffusing an N-type conductivity producing ingredient into the P region to form the N-type emitter regions, and securing the collector region 18 on the semiconductor substrate 10.

The semiconductor device illustrated in Fig. 2 is similar to that illustrated in Fig. 1. Referring to Fig. 2, there is disclosed a body of single crystal semiconductor material which includes the transistor regions and the substrate 10 as the same physical piece of semiconductor material. The entire unit is formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the region occupied by collector region 18 and thereafter the device is constructed as the Fig. 1 device. In the device of Fig. 2, the ohmic contact 33 is made to the top surface of the collector region 18 in a similar manner as contacts 26, 28 and 30.

In each embodiment described, the collector-base P-N junction extends to one surface of the body and there defines an enclosed area and each emitter-base P-N junction extends to said one surface and there defines another enclosed area surrounded by said first-mentioned enclosed area.

It must be emphasized that only two embodiments of the invention has been described and that other variations and modifications may be made without departing from the scope of the invention as defined in the appended claims.

Reference is additionally made to our copending patent applications nos. 23279/63; 46086/63; 46088/63; 46089/63, and 46090/63, (Serial nos. 958244; 958245; 958247; 958248 and 958249) also divided from said parent application no. 16071/60. (Serial no. 958242).

Terms indicative of position, such as "on", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A transistor comprising an integral or integrated body of semiconductor material containing a semiconductor substrate, a monocrystalline collector region of one conductivity type in or on one face of said substrate, a diffused monocrystalline base region of opposite conductivity type contiguous with said collector region to form therewith a first P-N junction extending to one surface of said body and there defining a first enclosed area and a diffused monocrystalline emitter region of said one conductivity type contiguous with said base region to form therewith a second P-N junction extending to said one surface and there defining a second enclosed area surrounded by said first enclosed area, and ohmic connections to said collector, base and emitter regions.

2. A transistor according to claim 1, wherein said collector region is a diffused region.

3. A method of fabricating a transistor contained in an integral or integrated body of single crystal semiconductor material comprising the steps of: forming a collector region of one conductivity type in or on a semiconductor substrate, forming a base region of opposite conductivity type contiguous with said collector region to form therewith a P-N junction extending to one surface of said body and there defining a first encosed area by diffusing a conductivity type producing ingredient into said collector region adapted to give said base region said opposite conductivity type forming an emitter region of said one conductivity type contiguous with said base region to form therewith a second P-N junction extending to said one surface and there defining a second enclosed area surrounded by said first enclosed area by diffusing a conductivity type producing ingredient into said base region adapted to give said emitter region said one conductivity type, and providing ohmic connections to said collector, base and emitter regions.

4. A method of fabricating a transistor according to claim 3, wherein said collector region is formed in said semiconductor substrate including the step of diffusing a conductivity type producing ingredient into said semiconductor substrate adapted to give said collector region said one conductivity type.

5. A transistor according to claim 1 or 2, included as part of a semiconductor network wherein said body includes one or

actually includes one NPN transistor plus an integral diode formed by the additional emitter region.

The collector region 18 may be mounted or secured on a semiconductor substrate 10, for example, by solder glass. The semiconductor substrate 10 may be composed of intrinsic semiconductor material having a relatively high order of resistivity.

Ohmic contacts are made to the regions by metal contacts 33, 26, 28 and 30. The contacts 26, 28 and 30 may be plated or evaporated onto their respective regions. The collector contact 33 may be soldered or alloyed to substrate 10 and extends beneath the collector region 18 to make ohmic contact therewith.

The device may be constructed by providing an N-type wafer, diffusing a P-type conductivity producing ingredient into one surface of said wafer, selectively etching the semiconductor material to produce the shape illustrated in Fig. 1, selectively diffusing an N-type conductivity producing ingredient into the P region to form the N-type emitter regions, and securing the collector region 18 on the semiconductor substrate 10.

The semiconductor device illustrated in Fig. 2 is similar to that illustrated in Fig. 1. Referring to Fig. 2, there is disclosed a body of single crystal semiconductor material which includes the transistor regions and the substrate 10 as the same physical piece of semiconductor material. The entire unit is formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the region occupied by collector region 18 and thereafter the device is constructed as the Fig. 1 device. In the device of Fig. 2, the ohmic contact 33 is made to the top surface of the collector region 18 in a similar manner as contacts 26, 28 and 30.

In each embodiment described, the collector-base P-N junction extends to one surface of the body and there defines an enclosed area and each emitter-base P-N junction extends to said one surface and there defines another enclosed area surrounded by said first-mentioned enclosed area.

It must be emphasized that only two embodiments of the invention has been described and that other variations and modifications may be made without departing from the scope of the invention as defined in the appended claims.

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WHAT WE CLAIM IS:—

1. A transistor comprising an integral or integrated body of semiconductor material containing a semiconductor substrate, a monocrystalline collector region of one conductivity type in or on one face of said substrate, a diffused monocrystalline base region of opposite conductivity type contiguous with said collector region to form therewith a first P-N junction extending to one surface of said body and there defining a first enclosed area and a diffused monocrystalline emitter region of said one conductivity type contiguous with said base region to form therewith a second P-N junction extending to said one surface and there defining a second enclosed area surrounded by said first enclosed area, and ohmic connections to said collector, base and emitter regions.

2. A transistor according to claim 1, wherein said collector region is a diffused region.

3. A method of fabricating a transistor contained in an integral or integrated body of single crystal semiconductor material comprising the steps of: forming a collector region of one conductivity type in or on a semiconductor substrate, forming a base region of opposite conductivity type contiguous with said collector region to form therewith a P-N junction extending to one surface of said body and there defining a first encosed area by diffusing a conductivity type producing ingredient into said collector region adapted to give said base region said opposite conductivity type forming an emitter region of said one conductivity type contiguous with said base region to form therewith a second P-N junction extending to said one surface and there defining a second enclosed area surrounded by said first enclosed area by diffusing a conductivity type producing ingredient into said base region adapted to give said emitter region said one conductivity type, and providing ohmic connections to said collector, base and emitter regions.

4. A method of fabricating a transistor according to claim 3, wherein said collector region is formed in said semiconductor substrate including the step of diffusing a conductivity type producing ingredient into said semiconductor substrate adapted to give said collector region said one conductivity type.

5. A transistor according to claim 1 or 2, included as part of a semiconductor network wherein said body includes one or

* C L M S *

more other circuit elements.

6. A method of fabricating a transistor according to claim 3 or 4, including the step of forming one or more other circuit elements in said body.

7. A transistor when produced by the method of claim 3, 4 or 6.

H. D. FITZPATRICK & CO.,
Chartered Patent Agents,
3 Gray's Inn Square, London, W.C.1,
and
94 Hope Street, Glasgow, C.2.

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