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(54) Title: INTERLEAVED MIRRORED MEMORY SYSTEMS

(57) **Abstract:** In some embodiments, a system includes a first memory assembly coupled to a first channel and a second memory assembly coupled to a second channel. The system includes a memory controller to write first and second primary data sections to the first and second memory assemblies, respectively, and write first and second redundant data sections to the second and first memory assemblies, respectively, wherein the first and second redundant data sections are redundant with respect to the first and second primary data sections, respectively. Other embodiments are described and claimed.

