

FABRICATION OF QUBIT WITH SELF DEFINED JOSEPHSON JUNCTION

BACKGROUND

[0001] The currently claimed embodiments of the present invention relate to superconducting qubits, and more specifically, to a method of making a Josephson junction in a superconducting qubit and the superconducting qubit device.

[0002] Quantum computation is based on the reliable control of quantum bits (referred to herein throughout as qubits). The fundamental operations required to realize quantum algorithms are a set of single-qubit operations and two-qubit operations which establish correlations between two separate quantum bits. The realization of high fidelity two-qubit operations may be desirable both for reaching the error threshold for quantum computation and for reaching reliable quantum simulations.

[0003] The superconducting quantum processor (having one or more superconducting qubits) includes superconducting metals (e.g., Al, Nb, etc.) on an insulating substrate (e.g., Si or high resistivity Si, Al_2O_3 , etc.). The superconducting quantum processor is typically a planar two-dimensional lattice structure of individual qubits linked by a coupler in various lattice symmetry (for example, square, hexagonal, etc.), and a readout structure located on a flip-chip. The couplers can be made of a capacitor, a resonator, a coil or any microwave component that provides a coupling between qubits.

[0004] Conventional methods of fabricating superconducting qubits are based on the standard Josephson junction fabrication using the Dolan or Manhattan methods to form bridges. The above methods require many steps including many lithographic steps and the resulting qubit may be relatively bulky and thus may be sensitive to far field and/or near field coupling to the external environment.

SUMMARY

[0005] An aspect of the present invention is to provide a method of making a Josephson junction in a superconducting qubit. The method includes providing a substrate having a convex structure, the convex structure having a first face and a second face meeting

at an edge; and depositing a first layer of superconducting material on the first face of the substrate material. The method further includes oxidizing the first layer of superconducting material to form a layer of oxide material on a surface of the first layer of superconducting material; and depositing a second layer of the superconducting material on the second face of the substrate material. A portion of the second layer is in contact with a portion of the layer of oxide material at or in the vicinity of the edge such that the portion of the layer of oxide material is sandwiched between a portion of the first layer of superconducting material and the portion of the second layer of superconducting material to define a Josephson junction at or in the vicinity of the edge.

[0006] Another aspect of the present invention is to provide a qubit device. The qubit device includes a substrate having a convex structure, the convex structure having a first face and second face meeting at an edge and forming an angle therebetween. The qubit device further includes a first layer of superconducting material deposited on the first face of the substrate material; and a layer of oxide material on a surface of the first layer of superconducting material. The qubit device also includes a second layer of the superconducting material on the second face of the substrate material. A portion of the second layer is in contact with a portion of the layer of oxide material at or in the vicinity of the edge such that the portion of the layer of oxide material is sandwiched between a portion of the first layer of superconducting material and a portion of the second layer of superconducting material to define a Josephson junction at or in the vicinity of the edge.

[0007] Yet another aspect of the present invention is to provide a method of making a Josephson junction in a superconducting qubit. The method includes providing a substrate; depositing superconducting material on a surface of the substrate; and depositing a sacrificial material layer on the superconducting material. The method further includes removing a portion of the sacrificial material layer to uncover a portion of the surface of the substrate to define a qubit pocket; and etching the portion of the surface of the substrate to form a convex shape in the substrate, the convex shape having a first face and a second face meeting at an edge. The method also includes forming a Josephson Junction at or in the vicinity of the edge without applying electron beam or optical beam lithography to connect capacitor pads connected to the Josephson Junction to a plurality of buses.

[0008] In an embodiment, forming the Josephson Junction includes depositing a first layer of superconducting material on the first face of the convex shape in the substrate

material; oxidizing the first layer of superconducting material to form a layer of oxide material on a surface of the first layer of superconducting material; and depositing a second layer of the superconducting material on the second face of the convex shape in the substrate material. A portion of the second layer is in contact with a portion of the layer of oxide material at or in the vicinity of the edge such that the portion of the layer of oxide material is sandwiched between a portion of the first layer of superconducting material and the portion of the second layer of superconducting material to define the Josephson junction at or in the vicinity of the edge.

[0009] In an embodiment, the method further includes defining the plurality of buses and a plurality of readout resonators using lithography; and removing portions of the superconducting material to form the plurality of buses and readout resonators on the substrate. In an embodiment, removing a portion of the sacrificial material layer includes applying a single lithography step.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present disclosure, as well as the methods of operation and functions of the related elements of structure and the combination of parts and economies of manufacture, will become more apparent upon consideration of the following description and the appended claims with reference to the accompanying drawings, all of which form a part of this specification, wherein like reference numerals designate corresponding parts in the various figures. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only and are not intended as a definition of the limits of the invention.

[0011] FIG. 1 is a schematic lateral view of a substrate on which is deposited a layer superconducting material, according to an embodiment of the present invention;

[0012] FIG. 2A shows a schematic top view of the substrate with the layer of superconducting material deposited thereon and having some portions of the layer of superconducting material removed, according to an embodiment of the present invention;

[0013] FIG. 2B is a cross-section view, along line 2B-2B shown in FIG. 2A, of the substrate with the layer of superconducting material deposited thereon, according to an embodiment of the present invention;

[0014] FIG. 3A shows a schematic top view of the substrate having deposited thereon the layer of superconducting material and a layer of sacrificial material layer with a portion of the sacrificial material layer being removed to uncover a portion of a surface of the substrate 100 to define a qubit pocket, according to an embodiment of the present invention;

[0015] FIG. 3B is a cross-section view, along line 3B-3B shown in FIG. 3A, of the substrate having deposited thereon the layer of superconducting material and the layer of sacrificial material layer with a portion of the sacrificial material layer being removed to uncover a portion of the surface of the substrate to define the qubit pocket, according to an embodiment of the present invention;

[0016] FIG. 4A shows a schematic top view of the substrate with the uncovered portion of the surface of the substrate defining the qubit pocket and the extent of undercut when etching the uncovered portion, according to an embodiment of the present invention;

[0017] FIG. 4B is a cross-section view, along line 4B-4B shown in FIG. 4A, of the substrate with the uncovered portion of the surface of the substrate defining the qubit pocket and the extent of the undercut when etching the uncovered portion, according to an embodiment of the present invention;

[0018] FIG. 4C is a cross-section view, along line 4C-4C shown in FIG. 4A, of the substrate with the uncovered portion of the surface of the substrate defining the qubit pocket and the extent of undercut when etching the uncovered portion, according to an embodiment of the present invention;

[0019] FIG. 5 is a cross-section view of the substrate showing a wedge shape structure, according to an embodiment of the present invention;

[0020] FIG. 6A is a top view of a formed qubit device including a Josephson junction (JJ) and buses and resonators, according to an embodiment of the present invention;

[0021] FIG. 6B is a cross-section view of the formed qubit device, along line 6B-6B shown in FIG. 6A, according to an embodiment of the present invention; and

[0022] FIG. 6C is a cross-section view of the formed qubit device, along line 6C-6C shown in FIG. 6A, according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0023] In an embodiment, a method of making a Josephson junction for a superconducting qubit device is provided herein. In an embodiment, the method includes providing a substrate 100 and depositing a layer of superconducting material 102 on a surface 100S of the substrate 100. FIG. 1 is a schematic lateral view of the substrate 100 on which is deposited the layer superconducting material 102, according to an embodiment of the present invention. In an embodiment, the substrate 100 can be any non-conductor material including, but not limited to, Silicon (Si) and Sapphire. In an embodiment, the superconducting material 102 can be any superconducting material including, but not limited to, Niobium (Nb), Aluminum (Al), etc.

[0024] The method further includes removing portions the superconducting material 102 to uncover a first portion 100A of the surface 100S of the substrate 100 to form a plurality of buses 202 and readout resonators 204 on the substrate. In an embodiment, removal of portions of the layer of superconducting material 102 can be performed by etching (for example, using chemical etching such as acid etching) the portions of the layer of superconducting material 102.

[0025] FIG. 2A shows a schematic top view of the substrate 100 with the layer of superconducting material 102 deposited thereon and having some portions of the layer of superconducting material 102 removed, according to an embodiment of the present invention. FIG. 2B is a cross-section view, along line 2B-2B shown in FIG. 2A, of the substrate with the layer of superconducting material 102 deposited thereon, according to an embodiment of the present invention.

[0026] The method further includes depositing a sacrificial material layer 302 on the layer of superconducting material 102 and on the uncovered portion 100A of the surface 100S of the substrate 100. The method also includes applying electron beam or optical beam lithography to expose a portion of the sacrificial material layer 302; and removing the exposed portion of the sacrificial material layer 302 to uncover a portion 100B of the surface 100S of the substrate 100 to define a qubit pocket 304. In an embodiment, removing the exposed portion of the sacrificial material layer 302 comprises applying a single lithography step.

[0027] FIG. 3A shows a schematic top view of the substrate 100 having deposited thereon the layer of superconducting material 102 and the layer of sacrificial material layer

302 with a portion of the sacrificial material layer 302 being removed to uncover the portion 100B of the surface 100S of the substrate 100 to define the qubit pocket 304, according to an embodiment of the present invention. FIG. 3B is a cross-section view, along line 3B-3B shown in FIG. 3A, of the substrate 100 having deposited thereon the layer of superconducting material 102 and the layer of sacrificial material layer 302 with a portion of the sacrificial material layer 302 being removed to uncover the portion 100B of the surface 100S of the substrate 100 to define the qubit pocket 304, according to an embodiment of the present invention.

[0028] In an embodiment, depositing the sacrificial material layer 302 on the layer of superconducting material 102 and on the uncovered portion 100B of the substrate 100 includes depositing Germanium (Ge) on the superconducting material layer 102 and on the uncovered portion 100B of the substrate 100.

[0029] As shown in FIG. 3A, in an embodiment, the uncovered portion 102B of the surface 100S of the substrate 100 defining the pocket 304 has two mirror symmetric shapes 304A and 304B. As shown in FIG. 3A, the uncovered portion 100B of the surface 100S of the substrate 100 has an H-like shape. The two mirror symmetric shapes 304A and 304B face each other to form a relatively narrower strip 304C of the sacrificial material layer 302 at a median of the two mirror symmetric shapes 304A and 304B.

[0030] In an embodiment, the method further includes etching the portion 100B of the surface 100S of the substrate 100 to form a convex structure 402 in the substrate 100 (shown in FIGS. 4C and 5). In an embodiment, etching the portion 100B includes etching using potassium hydroxide (KOH) or Tetramethylammonium hydroxide (TMAH).

[0031] FIG. 4A shows a schematic top view of the substrate 100 with the uncovered portion 100B of the surface 100S of the substrate 100 defining the qubit pocket 304 and the extent of undercut 404 when etching the uncovered portion 100B, according to an embodiment of the present invention. In an embodiment, the extent of the undercut 404 created by the etching of the portion 100B is delimited by the dotted lines, as shown in FIG. 4A.

[0032] FIG. 4B is a cross-section view, along line 4B-4B shown in FIG. 4A, of the substrate 100 with the uncovered portion 100B of the surface 100S of the substrate 100 defining the qubit pocket 304 and the extent of undercut 404 when etching the uncovered portion 100B, according to an embodiment of the present invention. Along the 4B-4B cross-

section shown in FIG. 4B, the sacrificial material layer 302 forms a bridge structure 406 that runs on top of the surface 100S of the substrate 100 and crosses a void 408 formed after etching the portion 100B of the surface 100S of the substrate 100.

[0033] FIG. 4C is a cross-section view, along line 4C-4C shown in FIG. 4A, of the substrate 100 with the uncovered portion 100B of the surface 100S of the substrate 100 defining the qubit pocket 304 and the extent of undercut 404 when etching the uncovered portion 100B, according to an embodiment of the present invention. Along the 4C-4C cross-section shown in FIG. 4C, the sacrificial material layer 302 forms the bridge structure 406 that runs on top of the surface 100S of the substrate 100 and on top of the formed convex structure 402 after etching the portion 100B of the surface 100S of the substrate 100.

[0034] In an embodiment, the convex structure 402 can have for example a wedge shape or a triangular prism shape. In general, the convex structure 402 has a first face 402A and a second face 402B meeting at an edge 402C. The two faces 402A and 402B define an angle (e.g., an acute angle less than 90 deg.) at the edge 402C. In an embodiment, as shown in FIG. 4C, a cross-section of the convex structure along the line 4C-4C has a triangular shape. In an embodiment, the first face 402A and the second face 402B are formed in a (111) crystal plane of the substrate 100.

[0035] FIG. 5 is a cross-section view of the substrate showing the wedge shape structure, according to an embodiment of the present invention. In an embodiment, the method further includes depositing a first layer of superconducting material 502 on the first face 402A of the convex structure 402 in the substrate 100. In an embodiment, the first layer of superconducting material 502 can be deposited by using a first evaporation, as illustrated for example in FIG. 5. In an embodiment, the first layer of superconducting material 502 is also deposited in a first trench 510 and second trench 512 formed during the etching of the substrate 100.

[0036] The method further includes, after depositing the first layer of superconducting material 502, oxidizing the first layer of superconducting material 502 to form a layer of oxide material 504 on a surface of the first layer of superconducting material 502. The layer of oxide material 504 forms where the first layer of superconducting material 502 is not in contact with the substrate 100. In particular, an end portion 502A of the first layer of superconducting material 502 near the edge 402C is also oxidized and a portion 504A of the oxide layer 504 forms on the end portion 502A of the first layer of

superconducting material 502. In addition, the oxide layer 504 also forms at the bottom of the trenches 510 and 512 on top of the first layer of superconducting material 502.

[0037] The method also includes depositing a second layer of the superconducting material 506 on the second face 402B of the convex structure 402. In an embodiment, the second layer of superconducting material 506 can be deposited by using a second evaporation, as illustrated for example in FIG. 5. A portion 506A of the second layer of superconducting material 506 is deposited in contact with the portion 504A of the layer of oxide material 504 at or in the vicinity of the edge 402C such that the portion of the layer of oxide material 504A is sandwiched between the portion 502A of the first layer of superconducting material 502 and the portion 506A of the second layer of superconducting material 506 to define a Josephson junction (JJ) at or in the vicinity of the edge 402C. In an embodiment, the oxide material layer 504 is selected from the group consisting of Aluminum oxide and Niobium oxide. In an embodiment, the second layer of superconducting material 506 is also deposited inside the trenches 510 and 512 on top of the oxide layer 504.

[0038] In an embodiment, the first layer of superconducting material 502 and the second layer of superconducting material 506 can be from a same or a different superconducting material. For example, in one embodiment, the first layer of superconducting material 502 and the second layer of superconducting material 506 can be both Aluminum layers. In another embodiment, the first layer of superconducting material 502 can be an Aluminum layer and the second layer of superconducting material can be a Niobium layer. In addition, the first layer of superconducting material 502 and/or the second layer of superconducting material 506 can be the same or different from the layer of superconducting material 102.

[0039] The method further includes removing remaining sacrificial material layer (e.g., Germanium) 302 to form the Josephson Junction (JJ) and the qubit device 600. FIG. 6A is a top view of the formed qubit device 600 including the Josephson junction (JJ) and the buses and resonators 202 and 204, according to an embodiment of the present invention. FIG. 6B is a cross-section view of the formed qubit device 600, along line 6B-6B shown in FIG. 6A, according to an embodiment of the present invention. FIG. 6C is a cross-section view of the formed qubit device 600, along line 6C-6C shown in FIG. 6A, according to an embodiment of the present invention.

[0040] As shown in FIGS. 6A-6C, the qubit device 600 includes the substrate 100 having the convex structure 402, the convex structure 402 having the first face 402A and the second face 402B meeting at the edge 402C and forming an angle therebetween. The qubit device 600 also includes the first layer of superconducting material 502 deposited on the first face 402A of the convex structure 402 of the substrate material 100. The qubit device 600 also includes a layer of oxide material 504 on the surface of the first layer of superconducting material 502. The qubit device 600 also includes the second layer of the superconducting material 506 on the second face of the substrate material 402B. The portion 506A of the second layer of superconducting material 506 is deposited in contact with the portion 504A of the layer of oxide material 504 at or in the vicinity of the edge 402C such that the portion of the layer of oxide material 504A is sandwiched between the portion 502A of the first layer of superconducting material 502 and the portion 506A of the second layer of superconducting material 506 to define a Josephson junction (JJ) at or in the vicinity of the edge 402C.

[0041] In an embodiment, the first layer of superconducting material 502 and the second layer of superconducting material 506 that are also deposited in the first trench 510 define the first capacitor pad 602 to electrically connect to the Josephson junction (JJ), as shown in FIGS. 6A and 6B. The first layer of superconducting material 502 and the second layer of superconducting material 506 that are also deposited in the second trench 512 define the second capacitor pad 604 to electrically connect to the Josephson junction (JJ), as shown in FIGS. 6A and 6B. In an embodiment, the Josephson junction (JJ) is formed at or in the vicinity of the edge 402C without applying electron beam or optical beam lithography to connect capacitor pads 602 and 604 to the Josephson junction (JJ) and to the plurality of buses 202 and/or the plurality of readout resonators 204. As described in the above paragraphs, the plurality of buses 202 and the plurality of readout resonators 204 are defined using lithography and portions of the superconducting material layer 102 are removed to form the plurality of buses and readout resonators 202 and 204 on the substrate 100. Gaps between the first capacitor pad 602 and the plurality of buses 202 and readout resonators 204 and gaps between the second capacitor pad 604 and the plurality of buses 202 and readout resonators 204 define the coupling capacitors to couple microwave energy to the Josephson junction (JJ).

[0042] In conventional methods, ion milling is used to open up naturally formed oxide on capacitor pad material so as to connect the Josephson junction to the capacitor pad

material. In conventional methods, this ion milling step is typically performed before junction metal evaporation and *in situ*. In contrast, in some embodiments of the present invention, the capacitor pads 602 and 604 and the Josephson junction (JJ) of the qubit are formed in a same step. As a result, the use of ion milling to open up the naturally formed oxide on capacitor pad material to connect the Josephson junction to the capacitor pads is not needed. Indeed, the ion milling step can damage the substrate 100 (e.g., silicon) in exposed regions and thus can negatively affect coherence. Therefore, by using the methods according to some embodiments of the present invention, this problem can be avoided and thus this challenge can be overcome.

[0043] In addition, the methods according to some embodiments of the present invention allow for the fabrication of a qubit device 600 that substantially reduces far field and near field coupling to the external environment. In addition, the overall size of the resulting qubit device 600 is also reduced thus providing a compact qubit device which thereby reduce losses and allows for the assembly of 2D lattices of qubits with symmetry.

[0044] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.