that case, the unselected Local I/O lines remain undisturbed by the Global I/O lines and can be precharged in advance allowing very fast cycle times.

According to a second solution, a decoder, that can be as simple as for instance a NOR or a NAND gate, can be added between a CoLumn Select line and the row decode signal φ_{PCH}. With this second solution, the content of the half-selected sense amplifiers remains unaffected by the Local I/O lines. The load along the CoLumn Select lines can also be reduced (the decoder being used as a local signal booster) while the cycle time may be improved. This second solution is in particular described in the French patent application n° 1152256 filed by the Applicant on March 18, 2011 and not yet published.

Both first and second solutions can be applied simultaneously which afford for very good performances but may not be optimal on the layout point of view. Indeed, the only possible location for these decoders is immediately next to the sense amplifiers (or even into the sense amplifier layout) which introduces an "irregular" layout in a very sensitive region.

Summary of the invention

Embodiments of the invention aim at providing a semiconductor memory that may not suffer from the above mentioned drawbacks, and in particular a semiconductor memory wherein the sense amplifiers are introduced without particular layout constraint and without area penalty.

According to a first aspect of the present invention, there is provided a sense amplifier for sensing and amplifying data stored in a memory cell, the sense amplifier being connected between a bit line and a reference bit line complementary to the first bit line and comprising:

- a sense circuit capable of providing an output indicative of the data stored in the memory cell; and
- a precharge and decode circuit comprising a pair of dual gate transistors for precharging the first and second bit lines during a precharge operation and for transferring the output provided by the sense circuit to a data line during a read operation, wherein each dual gate transistor of the precharge and decode circuit has a first gate and a second gate, the first gates of the dual gate transistors being both controlled by a decoding control signal and the second gates of the dual gate transistors being both controlled by a precharge control signal.

Other preferred, although non limitative, embodiments are as follows:

CLAIMS

1. A sense amplifier for sensing and amplifying data stored in a memory cell, the sense amplifier being connected between a bit line (BL) and a reference bit line ($\overline{BL}$) complementary to the first bit line and comprising:

- a sense circuit (SC) capable of providing an output indicative of the data stored in the memory cell; and
- a precharge and decode circuit (PDC) comprising a pair of dual gate transistors (T5, T6) for precharging the first and second bit lines during a precharge operation and for transferring the output provided by the sense circuit to a data line during a read operation, wherein each dual gate transistor of the precharge and decode circuit has a first gate and a second gate, the first gates of the dual gate transistors being both controlled by a decoding control signal and the second gates of the dual gate transistors being both controlled by a precharge control signal.

~~2. The sense amplifier of claim 1, wherein each dual gate transistor of the precharge and decode circuit has a first gate and a second gate, the first gates of the dual gate transistors being both controlled by a decoding control signal and the second gates of the dual gate transistors being both controlled by a precharge control signal.~~

~~3.~~2. The sense amplifier of claim 1~~2~~, wherein each dual gate transistor is capable of working in either depletion or enhancement mode with respect to the state of the first gate of the transistor controlled by the decoding control signal depending on the state of the second gate of the transistor controlled precharge control signal.

~~4.~~3. The sense amplifier of claim 2~~3~~, wherein each dual gate transistor is capable of working in depletion mode when the precharge control signal is at a ON state, and capable of working in enhancement mode when the precharge control signal is at a OFF state.

5.4. The sense amplifier according to any one of claims 1-3 ~~1-4~~ made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a substrate by an insulating layer, wherein the dual gate transistors each comprise a first and a second gate, one of which is a back gate formed in the substrate below the insulating layer.

6.5. The sense amplifier of claim ~~4~~5, wherein the second gate of each dual gate transistor is a back gate formed in the substrate below the insulating layer.

7.6. The sense amplifier according to any one of claims 1-3~~1-4~~, wherein each dual gate transistor is a Fin-type independent double gate transistor.

8.7. The sense amplifier according to any one of claims 1-3~~1-4~~, wherein each dual gate transistor is made of two single gate transistors arranged in parallel.

9.8. The sense amplifier according to any one of claims 1-7~~1-8~~, wherein the precharge and decode circuit (PDC) comprises a single pair of dual gate transistors (T5, T6).

10.9. The sense amplifier according to any one of claims 1-8~~1-9~~, wherein each dual gate transistor is arranged in series between one of the bit line and the reference bit line and a corresponding one of a first and a second data lines.

11.10. The sense amplifier of claim 9~~10~~ made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a substrate by an insulating layer, wherein the sense circuit comprises a pair of cross-coupled inverters arranged between the first and second bit lines, and wherein the cross-coupled inverters comprises dual gate transistors each having a first and a second gate, one of which is a back gate formed in the substrate below the insulating layer.

~~12.~~11. The sense amplifier of claim 10~~11~~, wherein the sense circuit consists in the pair of cross-coupled inverters and in a further equalization transistor.

~~13.~~12. A semiconductor memory comprising at least one array of memory cells arranged in rows and columns and at least one sense amplifier according to any one of claim 1-11~~1-12~~.

~~14.~~13. The semiconductor memory of claim 12~~13~~, wherein the first gates of the dual gate transistors are connected to a decoding line on which runs the decoding control signal and the second gates of the dual gate transistors are connected to a precharge line on which runs the precharge control signal, and wherein the decoding line and the precharge line are arranged perpendicular to each other, with for instance the decoding line arranged in the bit line direction of the memory cells array and the precharge line arranged in the direction perpendicular to the bit line direction.

~~15.~~14. A method of operating a sense amplifier according to claim ~~4~~3 comprising the steps of:

- setting the precharge control signal at the ON state to perform the precharge operation;
- setting the precharge control signal at the OFF state and sensing the data stored in the memory cell with the sense circuit;
- setting the decoding control signal at the high state to perform the read operation.