

SEMICONDUCTOR DEVICE

This invention relates to a semiconductor device, and more particularly to a power transistor which is contained in a high-output semiconductor integrated circuit (hereinbelow, called "power IC").

5 In a power transistor in the power IC of an audio output circuit or the like, a plurality of emitter regions are arranged within a single base region in order to derive a high output current. In such a power transistor, ballast resistances are inserted between the respective
10 emitter regions and the corresponding emitter input terminals so that emitter currents may flow uniformly through the respective emitter regions. In order to make the area occupied by the whole power transistor small, it has been considered to form the ballast resistance of a
15 diffused resistance region one end of which is continuous with the original emitter region and the other end of which is connected to an emitter input electrode.

The power transistor of the above structure, however, has had the disadvantage that current concentrates locally
20 in the part of the ballast resistance proximate to the input electrode, resulting in the breakdown of the transistor. Upon studying the breakdown, the inventor has found it ascribable to the fact that the ballast resistance region proximate to the input electrode also effects a
25 transistor operation. That is, it has been revealed that current is liable to concentrate on a parasitic transistor whose emitter is the ballast resistance region and that local current concentration occurs in a part of the region, with the result that the transistor breaks down.

30 It is therefore desirable to increase the breakdown strength of a power transistor which uses a part of an emitter region as an emitter ballast resistance.

According to the present invention there is provided a semiconductor device having a first semi-

conductor region of a first conductivity type in one principal surface of a semiconductor body, a second semiconductor region of a second conductivity type within and surrounded by the first semiconductor region, and a third semiconductor region of the first conductivity type within and surrounded by the second semiconductor region, the first, second, and third semiconductor regions forming a collector region, a base region, and an emitter region respectively; wherein the third semiconductor region includes an emitter operation portion, an electrode contact portion, and an emitter ballast resistance portion located between the emitter operation portion and the electrode contact portion, the part of the first semiconductor region located in the vicinity of the emitter ballast resistance portion is such as to determine the lateral width of the part of the second semiconductor region surrounding the emitter ballast resistance portion, and said lateral width is less than the lateral width of the part of the second semiconductor region surrounding the electrode portion.

Preferably, there is a fourth semiconductor region of the first conductivity type, forming an emitter region, within the second semiconductor region so as to be spaced from the third semiconductor region, the fourth semiconductor region including a transistor operation portion, an electrode connection portion, and a ballast resistance portion located between the transistor operation portion and the electrode connection portion.

There may be a plurality of discrete base regions in the collector region (first semiconductor region) and each base region may have a plurality of emitter regions. Each emitter region then has a ballast resistance portion with each base region having a reduced lateral width where it surrounds the corresponding ballast resistance portion. Preferably all the emitter regions have a common electrode.

Preferred embodiments of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

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Figure 1 is a plan view of a power transistor portion in a power IC embodying this invention,

Figure 2 is an enlarged plan view of essential parts in Figure 1,

Figure 3 is a sectional view taken along line III-III in Figure 1 and Figure 2,

5 Figure 4 is a sectional view taken along line IV-IV in Figure 2,

Figure 5 is an equivalent circuit diagram in the case where two power transistors are formed with a single base region, and

10 Figure 6 is an enlarged plan view similar to Figure 2, showing a power transistor portion in another embodiment.

Figure 1 is a plan view showing the structure of a power transistor of this invention formed in a power IC. The power transistor is formed in a part of a silicon semiconductor wafer 20 which consists of a P-type semiconductor substrate, and an N⁻-type epitaxial layer 2 formed thereon by epitaxial growth. In particular, the power transistor is surrounded by a P⁺-type isolation region 3 and is electrically isolated from circuit elements (not shown) formed in the rest of the wafer 20.

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As shown in Figure 3, an annular N⁺-type diffused region 5 which is deep enough to reach an N⁺-type buried layer 4 and which serves to lead out a collector electrode is formed within the N⁻-type epitaxial layer 2 which is surrounded with the isolation region 3. Within the N⁺-type epitaxial layer 2 and surrounded by the N⁺-type diffused region 5, P-type base regions 6 are formed by the well-known diffusion technique. As illustrated in Figure 1, four such base regions 6 are formed in the single island region 2. Adjacent pairs of base regions are surrounded by the N⁺-type region 5. Within each base region 6, two N⁺-type emitter regions 7 are formed by the well-known diffusion technique. As will be better understood from Figure 2, each emitter region 7 is composed of an emitter portion 7a which is formed for the main transistor operation, a resistance portion 7b which acts as a ballast resistance,

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and an electrode lead-out portion 7c. A section taken along line IV-IV in Figure 2 is shown in Figure 4. As seen from Figure 3, a metal electrode 8 of aluminum or the like is held in ohmic contact with the electrode lead-out portion 7c through a contact hole 18 provided in a silicon oxide film 10. As indicated by a two-dot chain line in Figure 1, the electrode 8 is connected in common to the emitter regions through the corresponding contact holes 18 and forms an emitter input terminal. An emitter electrode 9 made of a metal such as aluminum is held in ohmic contact with the emitter portion 7a of the transistor operation portion through a contact hole 17. A base electrode 14 made of a metal such as aluminum is held in ohmic contact with the part of the base region 6 between the pair of emitter regions 7a, through a contact hole 16. The contact hole 16 does not extend alongside the resistance portions 7b. As indicated by a two-dot chain line in Figure 1, the base electrode 14 is disposed so as to connect the base contact regions in common and thus forms a base input terminal. As indicated by a further two-dot chain line in Figure 1, a common collector electrode 15 is led out from the collector lead-out regions 5 through contact holes 13.

Figure 5 is an equivalent circuit diagram of transistors which are formed with a single base region 6 of the above power transistor. Tr_1 indicates the originally required transistor which is formed by the emitter portion 7a. Tr_2 indicates the unfavorable parasitic transistor which is formed by the electrode lead-out portion 7c held in ohmic contact with the emitter electrode 8. In addition, letter R indicates the ballast resistance which is formed by the resistance portion 7b.

Important here is that, as illustrated in Figures 1 and 2, the base region 6 is formed on the surface of the semiconductor body so as to be relatively narrow along the emitter ballast resistance portion 7b. That is, the width W_{B1} of the base region part surrounding the emitter ballast resistance portion 7b is smaller than the width W_{B2} of the

base region part surrounding the emitter electrode lead-out portion 7c.

The base resistance indicated by R_b can be regarded as including in parallel the resistance component of the base region directly below the emitter region (7b,7c) and the resistance component existing in the side surfaces of the emitter region (7b,7c). Now that the base region extending along the emitter region (7b,7c) is narrow, only the base resistance directly below the region 7b may be considered. Since the impurity concentration of the base region underlying this emitter region is low, the base resistance R_b can be made very great. This resistance acts as the base resistance of the parasitic transistor. As a result, the base-emitter voltage V_{BE} of the parasitic transistor can be reduced because of the voltage drop across the base resistance R_b during the operation of the power transistor. Normal operation can therefore be achieved by bringing only the main transistor Tr_1 into the "on" state and without allowing the parasitic transistor to turn into the "on" state. That is, current can be effectively poured onto the main transistor side during the operation of the power transistor by substantially preventing the parasitic transistor from operating. Moreover, a uniform operation can be effected since current concentration can be prevented by means of the ballast resistance R .

In order to operate the power transistor normally and to substantially prevent the parasitic transistor from operating as described above, the ballast resistance R needs to be designed in relation to the parasitic transistor so as to satisfy the formula

$$R < \frac{R_b}{h_{FE}} \quad (h_{FE}: \text{current gain}).$$

Usually, R is about 1Ω to 2Ω . Assuming h_{FE} to be approximately 200, therefore, it may be established that $R_b > 200 - 400\Omega$. Since, however, that base region directly

under the region 7c which determines the base resistance Rb has a high resistance ($10 \text{ k}\Omega/\square$) to the same extent as a pinch resistance, the base resistance Rb can be increased so as to satisfy the above formula by appropriately laying out the peripheral shape of the base region. By way of example, the width of the base region 6 extending along the regions 7b and 7c may be approximately $5\mu\text{m}$. The width of the base region 6 can be made smaller to a high precision by using some of the base region-forming windows for the formation of the emitter regions. The base width needs to be made $1 - 2 \mu\text{m}$ or greater in order to prevent punch-through between the N^+ -type region 7 and the N^- -type region 2.

As is apparent from the foregoing description, one feature of the invention is that the lateral width of the base regions where it surrounds the ballast resistance portion of the emitter region is less than its lateral width where it surrounds the electrode contact portion. Therefore, current concentration in the parasitic transistor can be prevented as described before, and current can be uniformly poured into the main transistor by the ballast resistance, so that the breakdown strength of the power transistor can be enhanced and the action of the ballast resistance can be effectively demonstrated.

Figure 6 shows another embodiment of this invention, and illustrates the plan configuration of a power transistor.

In this example, an emitter region 7 which consists of two emitter operation portions 7a, 7a' and emitter ballast resistance portions 7b, 7b' having substantially equal widths and an electrode lead-out portion 7c is formed within a single base region 6. An aluminum electrode as an emitter input terminal is led out from the electrode lead-out portion 7c. The base region 6 surrounds the emitter ballast resistance portions 7b, 7b' and the emitter electrode lead-out portion 7c, and is given an effectively smaller width in the vicinity of the portions 7b, 7b', as follows. No base

region exists between the pair of resistance portions 7b and 7b' and between a base contact hole 16 and the electrode lead-out portion 7c, and the N⁻-type epitaxial layer 2 is directly exposed to the substrate surface in that area. This signifies that, as in the foregoing embodiment, the width W_{B1} of the base region part surrounding the emitter ballast resistance portions 7b and 7b' is made smaller than the width W_{B2} of the base region part surrounding the emitter electrode lead-out portion 7c.

With such a construction, as in the preceding embodiment, the base resistance R_b of the parasitic transistor can be made large, so as to sharply reduce the supply of current thereto, and the main transistor can be operated normally. Moreover, a common emitter input terminal can be provided.

While this invention has been exemplified above, the examples can be further modified on the basis of the technical idea of this invention. For instance, the plan configuration of the base region extending along the ballast resistance portion may be altered variously, and the positions of the base contacts are not restricted to those in the foregoing examples. It is also possible, unlike the foregoing examples, for only one emitter region to be formed in a single base region, the base region having only a small width where it surrounds the emitter region on the front surface side. This invention is also applicable to a PNP-type transistor in which the conductivity types of the respective semiconductor regions above described are inverted.

As set forth above, the base region is made narrow along the emitter ballast resistance portion. Therefore, the base resistance of the parasitic transistor can be made great to reduce current flowing thereto, and current can be effectively poured to the main transistor portion. Moreover, current concentration can be prevented by the function of the emitter ballast resistance portion. It is accordingly

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possible to increase the breakdown strength of the transistor and to provide a semiconductor device which is useful especially as a power transistor.

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CLAIMS:

1. A semiconductor device having a first semiconductor region of a first conductivity type in one principal surface of a semiconductor body, a second semiconductor region of a second conductivity type within and surrounded by the first semiconductor region, and a third semiconductor region of the first conductivity type within and surrounded by the second semiconductor region, the first, second, and third semiconductor regions forming a collector region, a base region, and an emitter region respectively; wherein the third semiconductor region includes an emitter operation portion, an electrode contact portion, and an emitter ballast resistance portion located between the emitter operation portion and the electrode contact portion, the part of the first semiconductor region located in the vicinity of the emitter ballast resistance portion is such as to determine the lateral width of the part of the second semiconductor region surrounding the emitter ballast resistance portion, and said lateral width is less than the lateral width of the part of the second semiconductor region surrounding the electrode contact portion.
2. A semiconductor device according to claim 1, having electrodes on surfaces of the emitter operation portion and the electrode contact portion respectively.
3. A semiconductor device according to claim 1 or claim 2, wherein there is a fourth semiconductor region of the first conductivity type forming an emitter region within the second semiconductor region so as to be spaced from the third semiconductor region; the fourth semiconductor region including an emitter operation portion, an electrode connection portion, and a ballast resistance portion located between the emitter operation portion and the electrode connection portion.
4. A semiconductor device according to claim 3, having an electrode on a surface of the second semiconductor



region between the **emitter** operation portions of the third and fourth semiconductor regions.

5. A semiconductor device according to any one of the preceding claims, having a plurality of discrete base regions in the collector region, and a plurality of emitter regions in each base region, the emitter regions having a common electrode, and each emitter region having a ballast resistance portion with each base region having a reduced lateral width where it surrounds the corresponding ballast resistance portion.
 6. A semiconductor device according to any one of the preceding claims, wherein the second semiconductor region includes a first base contact portion adjacent the emitter operation portion of the third semiconductor region and a second base portion adjacent the ballast resistance portion of the third semiconductor region.
 7. A semiconductor device substantially as herein described with reference to and as illustrated in the accompanying drawings.
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