"METHOD OF MAKING A BIPOLAR TRANSISTOR"

The present invention relates to a method of making a bipolar transistor and to a semiconductor device with bipolar transistors integrated at a part of or the entire region of a substrate.

The construction of a prior bipolar transistor is shown in the accompanying Figure 1. The transistor of Figure 1 comprises a substrate 201 which is provided with a collector 202, a base 204 and an emitter 205. The base 204 and the collector 202 are directly connected to respective electrodes constituted by metal wiring members 210, while the emitter 205 is connected to its electrode 210 by way of polycrystalline silicon material 209. The transistor is provided with insulation films 207, 200 and with a device isolation area 203.

In order both to enhance the speed of a transistor and to improve the current amplification factor, it is necessary to shorten the travel time of the carriers within the base by lowering the impurity concentration of the base or by reducing the base length. Such a change in the construction, however, increases the base resistance, so that an improvement of the performance can hardly be expected. In particular, in the construction of the prior bipolar transistor shown in Figure 1 in which there is a considerable distance between the metal electrode 210 of the base 204 and the emitter 205, this disadvantage is very marked.

According to the present invention, there is therefore provided a method of making a bipolar transistor comprising a silicon substrate having a base

region and an emitter region which are respectively electrically connected to first and second conductive or semi-conductive material, the method comprising forming a metal layer on the silicon substrate, reacting the metal layer with the silicon substrate so as to produce a metal silicide which constitutes the first material and which is in electrical connection with the base region of the substrate; removing a portion of the first material in a region aligned with the emitter region of the substrate; forming an annular insulation film in the aligned region; and thereafter forming the second material radially inwardly of the annular insulation film so as to be in electrical connection with the emitter region, the annular insulation film electrically isolating the first and second materials from each other.

The metal of the metal silicide may be W, Mo, Ti or Ta.

Preferably, after the formation of the first material, a first insulation film is formed thereon; a portion of both the first material and the first insulation film is removed in the aligned region; a second insulation film is formed on the first insulation film so as to fill the aligned region; and a central portion of the second insulation film in the aligned region is removed so as to form the annular insulation film.

Preferably, the annular insulation film is a side wall insulator which has been produced by dry etching without masking the second insulation film.

Preferably, the second insulation film is completely removed except for the part thereof which

forms the annular insulation film.

The invention also comprises a bipolar transistor when made by the method set forth above.

The present invention enables the base resistance to be reduced and the performance of the transistor to be improved.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a sectional view of a prior bipolar transistor;

Figure 2 is a sectional view of an embodiment of a bipolar transistor in accordance with the present invention; and

Figures 3(A), 3(B) and 3(C) are sectional views of successive stages in the formation of the embodiment shown in Figure 2.

An embodiment of the present invention is shown in Figure 2, which is a sectional view. In this embodiment, a metal silicide layer 410 is provided on a base 409 formed in a silicon substrate 401. A first insulation film 406 and an annular side wall insulation film 407 are used for isolating the metal silicide layer 410 and a semiconductor material 411 from each other. A collector 402, a device isolation area 403, metal wirings or electrode terminals 404, 412 and 413, and an outer insulation layer 405 have the same construction as in a known device and the present invention is not restricted to the particular form of these elements shown in Figure 2.

The manufacturing process for producing the embodiment shown in Figure 2 will be explained with reference to Figure 3.

In Figure 3, only the elements essential for explaining the present invention are shown. A device

isolation area 502 and a base 503 are first formed in a substrate 501. Thereafter, the entire surface is covered with a metal layer 504. By annealing, a portion 505 of the metal layer 504 is reacted with silicon in the underlayer, thereby becoming a metal silicide, the metal silicide portion 505 being formed over the base 503 and over a region 501 aligned with an emitter region (not shown in Figure 3 but corresponding to the emitter 408 of Figure 2). Only the metal of the layer 504 which has not been turned into a metal silicide is etched by an appropriate solution while leaving the metal silicide portion 505. A first insulation film 506 is next provided over the entire surface, and a portion of the first insulation film 506, together with the part of the metal silicide portion 505 in the region 110, is removed by photolithography and etching. Thereafter, a second insulation film 507 is provided over the entire surface of the first insulation film 506 as shown in Figure 3(B) so as to fill the region 510.

By etching away other parts of the second insulation film 507, a portion thereof, which forms an annular side wall portion 509, is formed in the region 510, as shown in Figure 3(C).

Through processes such as the formation of an emitter 408 and an emitter electrode 412 and wiring thereafter by ordinary methods, the construction shown in Figure 2 is obtained. The metal layer 504 for obtaining a metal silicide, may for example, be a Ti, W, Mo or Ta layer. As a solvent for etching only the metal of the layer 504 while leaving the metal silicide, a mixed solution of ammonia and hydrogen peroxide, for example, is suitable.

In the construction shown in Figure 2, since the resistance of a metal silicide is much lower than the

impurity diffusion resistance of a conventional base, it is possible to greatly reduce the base resistance. Furthermore, since it is possible to reduce the distance between the metal silicide layer 410 and the emitter 408 to a greater extent than the distance between the electrode 210 and the emitter 205 shown in Figure 1, the base resistance is further reduced. In addition, since it is possible to control the distance between the metal silicide and the emitter by controlling the thickness of the insulation film 507 shown in Figure 3, the optimum distance between the metal silicide layer 410 and the emitter 408 can be set to take account of the sideways spread of the emitter diffusion layer 408.

Thus, the present invention enables a transistor to be produced which is capable of reducing the base resistance and has a high speed and a high current amplification factor.

CLAIMS

1. A method of making a bipolar transistor comprising a silicon substrate having a base region and an emitter region which are respectively electrically connected to first and second conductive or semi-conductive material, the said method comprising forming a metal layer on the silicon substrate, reacting the metal layer with the silicon substrate so as to produce a metal silicide which constitutes the said first material and which is in electrical connection with the base region of the substrate; removing a portion of the said first material in a region aligned with the emitter region of the substrate; forming an annular insulation film in said aligned region; and thereafter forming the said second material radially inwardly of the annular insulation film so as to be in electrical connection with the emitter region, the annular insulation film electrically isolating the said first and second materials from each other.

2. A method as claimed in claim 1 in which the metal of the metal silicide is W, Mo, Ti or Ta.

3. A method as claimed in claim 1 or 2 in which, after the formation of the first material, a first insulation film is formed thereon; a portion of both the first material and the first insulation film is removed in the said aligned region; a second insulation film is formed on the first insulation film so as to fill the aligned region; and a central portion of the second insulation film in the aligned region is removed so as to form the annular insulation film.

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4. A method as claimed in claim 3 in which the annular insulation film is a side wall insulator which has been produced by dry etching without mask of the second insulation film.

5. A method as claimed in claim 3 or 4 in which the second insulation film is completely removed except for the part thereof which forms the annular insulation film.

6. A method of making a bipolar transistor substantially as hereinbefore described with reference to Figures 2 and 3 of the accompanying drawings.

7. A bipolar transistor when made by the method of any preceding claim.

8. A semiconductor device composed of a bipolar transistor as claimed in claim 7 when appended to claim 1 and provided at a part of or the entire region of said substrate, comprising said first material consisting of a metal silicide which is electrically connected directly to the base region, said second material consisting of a semiconductor material which is electrically connected directly to the emitter region, a first insulator, a part of or all of which is directly on the first material, and said annular insulation film produced by dry-etching without masking a second insulator deposited on the substrate, in order to electrically isolate the first and second materials.

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