

Technical Field

The present invention relates to the field of packaging semiconductor chips, and more specifically relates to a chip packaging box.

Background Art

A chip packaging tray is usually used in relation to electronic products and electronic components, and more specifically used for carrying chips by enterprises that perform closed test for semiconductors.

Nowadays, in a common chip packaging tray having grid units, a bottom surface of each grid unit supporting a chip is usually a smooth surface that entirely contacts the smooth bottom surface of the chip. This structure has the following disadvantages: Since the smooth bottom surface of the chip entirely contacts the supporting surface of the corresponding grid unit, and the chip to be carried has a light weight and a small size, vacuum and electrostatic adherences may occur easily resulting in adherence of the chip with the grid unit that carries the chip.

In view of the above, structural improvements of the existing chip packaging tray is urgently required to prevent adherence of the chip with the grid unit.

Disclosure of the Invention

The technical problem to be solved by the present invention is the adherence of the chip with the grid unit that carries the chip.

A chip packaging box, comprising a body, grid units provided on the body, and a positioning frame extending downwardly around an outer periphery of the body; a bottom surface of each of the grid units is provided with intersecting grooves; side walls of each of the grid units incline towards a center of the corresponding grid unit from top to bottom.

In a preferred embodiment, the body has a square shape; the grid units are arranged in array; a height of each grid unit is greater than a thickness of the chip to be placed inside.

In a preferred embodiment, outer surfaces of the positioning frame are vertical surfaces; inner surfaces of the positioning frame are inclined surfaces that are inclined towards a center of the positioning frame from bottom to top.

In a preferred embodiment, each of the grid units has a square shape; the intersecting grooves cross one another perpendicularly; the bottom surface of each grid unit is formed as having multiple raised platforms of square or rhombus shapes mutually separated by the intersecting grooves.

In a preferred embodiment, the body is made of PE material.

In a preferred embodiment, protruding portions are provided around outer peripheral surfaces of the positioning frame; the inner surfaces of the positioning frame are provided with vertical sliding grooves matching with the protruding portions; when stacking two chip packaging boxes, the protruding portions of the positioning frame of a bottom one of the two chip packaging

boxes slide along the sliding grooves of the positioning frame of an upper one of the two chip packaging boxes and are then locked at top ends of the sliding grooves.

Compared with prior art, the present invention is used for storage and transportation of chips. Identical grid units are provided on the surface of the present invention. Intersecting grooves are provided on the supporting surface that supports a chip at the bottom surface of each grid unit, such that the supporting surface of each grid unit does not entirely contact the bottom surface of the corresponding chip placed inside. Therefore, the influences of vacuum adherence and static electricity are reduced, thereby preventing the chip from adhering with its corresponding grid unit due to electrostatic adherence. Hence, the chip is being better protected.

Brief Description of Drawings

FIG. 1 is the structural view of the present invention.

FIG. 2 is an enlarged view of portion A shown in FIG. 1.

FIG. 3 is a structural view showing how a chip is supported according to the present invention.

Best Mode for Carrying out the Invention

A chip packaging box is provided, which reduces influences of vacuum and electrostatic adherences, thereby preventing the chip from adhering a grid unit due to electrostatic adherence. Accordingly, the chip is protected more effectively. The present invention is also easy and convenient to use. The present invention will be further described in detail below with reference to an embodiment and the accompanying drawings.

As shown in FIG. 1, a chip packaging box comprises a body 10, grid units 12 provided on the body 10, and a positioning frame 11 extending downwardly around an outer periphery of the body 10; a bottom surface of each of the grid units 12 is provided with intersecting grooves 121; side walls 123 of each of the grid units 12 incline towards a center of the corresponding grid unit 12 from top to bottom.

The present invention is used for storage and transportation of chips 20; the grid units 12 provided on the chip packaging box are the same; the bottom surface of each of the grid units 12 is a supporting surface that supports a chip 20 and is provided with intersecting grooves 121; the intersecting grooves 121 render the supporting surface as a netted surface such that the supporting surface of each grid unit does not entirely contact a bottom surface of a corresponding chip, thereby reducing a contact surface area between the supporting surface of each grid unit and the bottom surface of the corresponding chip 20. When the chip 20 is taken out from the corresponding grid unit, air enters between the supporting surface of the corresponding grid unit and the bottom surface of the chip 20 through the intersecting grooves 121 to eliminate vacuum adherence and reduce the influences by vacuum adherence and static electricity. Accordingly, the chip 20 is prevented from adhering to the corresponding grid unit due to electrostatic adherence, and the chip 20 is thus being better protected.

The body 10 has a square shape; the grid units 12 are arranged in array. A height of each grid unit is greater than a thickness of the chip 20 to be placed inside. Square shaped body

facilitates transportation and stacking for generally convenient use. The height of each grid unit 12 is configured to prevent the chip 20 inside from falling out.

As shown in FIG. 3, outer surfaces of the positioning frame 11 are vertical surfaces; inner surfaces of the positioning frame 11 are inclined surfaces that are inclined towards a center of the positioning frame 11 from bottom to top. These structures facilitate stacking of multiple chip packaging boxes according to the present invention such that whenever an upper chip packaging box is stacked on a bottom chip packaging box of the same kind, self-alignment is achieved when the upper chip packaging box rests on the bottom chip packaging box by means of gravity force, thereby preventing jamming and misalignment when stacking up the chip packaging boxes.

As shown in FIG. 2, each of the grid units 12 has a square shape. The intersecting grooves 121 cross one another perpendicularly. The bottom surface of each grid unit 12 is formed as having multiple raised platforms 122 of square or rhombus shapes mutually separated by the intersecting grooves 121. Each of the grid units 12 may also have a circular shape. The intersecting grooves 121 and the raised platforms 122 can be configured to have a circular shape of other shapes based on practical needs.

The body 10 is made of PE material, which has a light weight and a low cost. The body 10 can be directly made as a one whole piece by means of for example injection molding.

Protruding portions are provided around outer peripheral surfaces of the positioning frame 11. The inner surfaces of the positioning frame 11 are provided with vertical sliding grooves matching with the protruding portions. In case of stacking of two chip packaging boxes according to the present invention, the protruding portions of the positioning frame 11 of a bottom one of the two chip packaging boxes slide along the sliding grooves of the positioning frame 11 of an upper one of the two chip packaging boxes and are then locked at the top ends of the sliding grooves. The protruding portions and the sliding grooves according to the present invention allow the protruding portions of the bottom one of the two chip packaging boxes to be placed within the sliding grooves of the upper one of the two chip packaging boxes, slide upwardly therein till the top ends of the sliding grooves, to achieve stacking through automatic alignment.

The present invention is used for storage and transportation of chips. Identical grid units are provided on the surface of the present invention. Intersecting grooves are provided on the supporting surface that supports a chip at the bottom surface of each grid unit, such that the supporting surface of each grid unit does not entirely contact the bottom surface of the corresponding chip placed inside. Therefore, the influences of vacuum adherence and static electricity are reduced, thereby preventing the chip from adhering with its corresponding grid unit due to electrostatic adherence. Hence, the chip is being better protected.

The present invention should not be limited to the most preferred embodiment described above. Any person skilled in this field of art should note that the same or similar technical solution as a result of structural changes in light of the teachings of the present invention should also fall within the scope of protection of the present invention.

CLAIMS

1. A chip packaging box, comprising a body, grid units provided on the body, and a positioning frame extending downwardly around an outer periphery of the body; a bottom surface of each of the grid units is provided with intersecting grooves; side walls of each of the grid units incline towards a center of the corresponding grid unit from top to bottom; each of the grid units has a square shape; the intersecting grooves cross one another perpendicularly; the bottom surface of each of the grid units is formed as having multiple raised platforms of square or rhombus shapes mutually separated by the intersecting grooves.
2. The chip packaging box of claim 1, wherein the body has a square shape; the grid units are arranged in array; a height of each grid unit is greater than a thickness of a chip to be placed inside.
3. The chip packaging box of claim 1, wherein outer surfaces of the positioning frame are vertical surfaces; inner surfaces of the positioning frame are inclined surfaces that are inclined towards a center of the positioning frame from bottom to top.
4. The chip packaging box of claim 1, wherein the body is made of PE material.
5. The chip packaging box of claim 1, wherein protruding portions are provided around outer peripheral surfaces of the positioning frame; inner surfaces of the positioning frame are provided with vertical sliding grooves matching with the protruding portions; when stacking two chip packaging boxes, the protruding portions of the positioning frame of a bottom one of the two chip packaging boxes slide along the sliding grooves of the positioning frame of an upper one of the two chip packaging boxes and are then locked at top ends of the sliding grooves.