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SEMICONDUCTOR DEVICE AND METHOD OF PRODUCING SUCH A DEVICE

The present invention relates to a semiconductor device in which a conductive layer is separated by an insulating layer from a semiconductor substrate e.g. an insulated gate field effect transistor.

It is known to use insulated gate field effect transistors in read-only memories. Some of such memories (hereinafter referred to as EPROMs) permit data to be re-written into the memory by the use of ultraviolet light.

One known memory cell for storing data in an EPROM consists of a field effect transistor having a conductive layer forming a floating gate disposed on a semiconductor substrate via an insulating layer and a control gate disposed on the floating gate via another insulating layer. Generally, both floating and control gates consist of polycrystalline silicon. (Refer, for example, to the magazine "Nikkei Electronics", January 5, 1981, pp.181-201).

Data in such a memory cell takes the form of electric charge stored in the floating gate. For good data retention it is necessary to prevent leakage of this charge; this has been found to occur between the edge of the floating gate and adjacent parts of the control gate and source drain region.

The inventors of the present invention have found

that charge leakage may be reduced if there is a second insulating layer covering sides of the insulating layer between the floating gate and the substrate. Therefore the present invention proposes a semiconductor device having:

a first conductive layer separated by a first insulating layer from a semiconductor substrate;

a second insulating layer adjacent and covering sides of the first insulating layer, the second insulating layer being a dense insulating layer sufficiently dense substantially to prevent charge leakage from the first conductive layer;

a second conductive layer separated by a third insulating layer from the first conductive layer;

two semiconductor regions in the substrate at the sides of the first conductive layer, the two semiconductor regions being of the same conductivity type and of opposite conductivity type to the part of the substrate adjacent the first conductive layer, whereby there is field effect transistor with the part of the substrate adjacent the first conductive layer being a channel of that transistor, the first conductive layer being a floating gate of the transistor, the second conductive layer being a control gate of the transistor, and the first insulating layer being the gate oxide layer of the transistor; and

further semiconductor regions having the same conductivity type as, but a lower impurity concentration than, the two semiconductor regions, and being respectively

between the part of the substrate being the channel of the transistor and each of the two semiconductor regions.

Thermal oxidation is a conventional means for forming, for example, silicon oxide to form the insulating layers. However, this is undesirable if the memory is to be miniaturised for the following reasons.

When an EPROM is miniaturised the memory cell reliability and the operating speed drop in the data write and read modes. Heat-treatment for an extended period of time is usually necessary in order to obtain the desired film thickness of the compact silicon oxide layer. The speed of formation of the silicon oxide layer between the floating gate and the control gate is higher than the speed of formation of the silicon oxide layer between the floating gate and the semiconductor substrate. Moreover, the speed of formation of the silicon oxide layer is higher at the edges of the surfaces of the floating and control gates than on the main surface of the semiconductor substrate. Accordingly, lift-up of the conductive layers may occur, particularly at the edge of the control gate. This means that the parasitic capacitance of the latter is bigger than that of the former. Thus, the potential of the floating gate drops with the result that the efficiency as well as reliability drops in the write mode of data to the memory cell. In the data read mode from the memory cell, on the other hand, the quantity of current that flows through the channel region between the source and drain

regions becomes smaller. This makes it difficult rapidly to discharge a data line, and causes a drop in operating speed. The shorter the channel length, the more significant this phenomenon, because the proportion of the capacitance drop becomes greater. This creates a problem for the miniaturisation of the memory cell.

The source or drain regions of the field effect transistor which serves as the memory cell may be formed in the following way. An impurity for forming the region is introduced by ion implantation into the main surface of the semiconductor substrate on both sids of the floating and control gates using these gates as a mask. Thereafter, the second insulating layer, e.g. a compact silicon oxide layer, is formed and the impurity is subjected to drive-inA diffusion. In this case, since heat-treatment for a long period is necessary as described above, the effective channel length between the source and drain regions becomes shorter because drive-in diffusion is excessive. This induces a short channel effect, invites a drop in reliability of the EPROM in the data read and write modes, and is unsuitable for the scale-down of the memory cell.

A preferred feature of the invention solves this difficulty by avoiding the use of lengthy thermal oxidation in forming the second insulating layer. This is achieved, for example, by using deposition methods such as chemical vapour deposition, plasma chemical vapour deposition, and sputtering. The second insulating layer of, for example,

silicon dioxide formed in this way may then be baked to densify the layer. Another possibility within the scope of the invention is the use of a glass layer, for example a layer of a low concentration phosphosilicate glass.

The second insulating layer of the invention may cover edges of some or all of the other insulating and conductive layers, and may extend on the substrate over the semiconductor regions. In this case the thickness of the second insulating layer of the invention may be substantially equal to or greater than that of the thinnest of the first and additional insulating layers.

The first semiconductor layer is preferably of polycrystalline silicon, and the second conductive layer may be of: polycrystalline silicon, a metal having a high melting point, a compound of silicon and a metal having a high melting point, or a polycrystalline silicon layer and a silicide layer of a metal having a high melting point thereon.

Preferably, the semiconductor regions are As ion impurity regions in the substrate, and the further semiconductor regions are P ion impurity regions in the substrate.

The invention may be used with many types of semiconductor and integrated circuit devices; EPROMs as mentioned above, field effect transistors and other semiconductor devices having a conductive layer separated from a semiconductor substrate by an insulating layer.

The invention also provides a method of producing a semiconductor device comprising:

forming a first conductive layer on a first insulating layer which separates the first conductive layer from the substrate;

forming a second insulating layer adjacent and covering sides of the first insulating layer, the second insulating layer being a dense insulating layer of sufficient density substantially to prevent charge leakage from the first conductive layer;

forming a third insulating layer on the first conductive layer;

forming a second conductive layer on the third insulating layer;

forming two semiconductor regions of a first conductivity type in the substrate; that part of the substrate between the two regions being of a second conductivity type opposite to the first, the two semiconductor regions being source and drain regions of a field effect transistor with that part of the substrate therebetween forming the channel of the field effect transistor, the first conductive layer forming a floating gate of the field effect transistor, the second conductive layer forming a control gate of the field effect transistor, and the first insulating layer being the gate insulating layer of the field effect transistor; and

forming further semiconductor regions of the same

conductivity type as, but a lower impurity concentration than the two semiconductor regions, the further semiconductor regions being respectively between the part of the substrate forming the channel of the transistor and each of the two semiconductor regions.

The method of forming the second insulating region may comprise:

(i) forming a silicon oxide layer covering the or each conductive layer, removing selectively the silicon oxide layer at parts other than both sides of each conductive layer, and then baking the silicon oxide layer for densification;

(ii) forming a silicon oxide layer to cover each conductive layer, baking the silicon oxide layer for densification, and thereafter removing selectively the silicon oxide layer at parts other than at both sides of the or each conductive layer;

(iii) depositing a silicon oxide layer and baking the silicon oxide layer to densify the silicon oxide layer, and the step of forming the pair of semiconductor regions includes introducing impurity ions into the semiconductor substrate, and wherein said depositing and baking are performed prior to the introduction of impurity ions; and

(iv) deposition of material for forming the second insulating layer and baking for densification thereof, and is performed prior to the step of forming the pair of semiconductor regions, including introduction of impurity

ions into the semiconductor substrate, whereby the extent of diffusion of the impurity ions to a region of the semiconductor substrate beneath the conductive layers is limited.

Preferably the step of forming the two semiconductor regions is performed after the step of forming the second insulating layer.

Embodiments of the invention will now be described by way of example, with reference to the drawings, in which:

Figure 1 is a circuit diagram showing parts of an EPROM, useful in understanding the present invention;

Figure 2 is a plan view of parts of the EPROM of Fig. 1;

Figure 3 is a sectional view taken along line III-III of Figure 2;

Figure 4 is a sectional view taken along line IV-IV of Figure 2;

Figure 5 is a diagram showing the dependence of the holding characteristics of data in the form of charge relative to the film thickness of an insulating layer, of the present invention;

Figures 6(A) to 6(C) are sectional views of parts of an EPROM in which the film thickness of an insulating layer is changed;

Figures 7(A) to 7(K) are sectional views of parts of the EPROM of Fig. 1 during production steps thereof,

Figure 8(A) is a sectional view taken along line

VIIIA-VIIIA in Figure 7(B);

Figure 8(B) is a sectional view taken along line VIIIB-VIIIB in Figure 7(C);

Figure 8(C) is a sectional view taken along line VIIIC-VIIIC in Figure 7(J);

Figures 9(A) to 9(J) are sectional views showing parts of a peripheral circuit of the EPROM of Fig. 1 during production steps thereof;

Figures 10(A) to 10(D) are sectional views showing parts of an EPROM produced by another method useful in understanding the present invention;

Figure 11 is a sectional view showing parts of an EPROM according to an embodiment of the present invention;

Figure 12 is a sectional view taken along line XII-XII in Figure 11;

Figure 13 is a sectional view of the EPROM of Fig. 11 during production thereof;

The same reference numerals are used throughout all the drawings to identify the corresponding parts and repeated explanation will be omitted.

The present invention will be described with reference to an EPROM using a field effect transistor having a floating gate and a control gate as a memory cell. However, the invention is not limited thereto and can be applied to any floating gate field effect device; or to any MISFET, or other field effect device, having gate electrodes; or, generally, to semiconductor devices having

conductive layers above a semiconductor substrate and isolated therefrom.

In the EPROM shown in Fig. 1, being a semiconductor device useful in understanding the present invention, an X decoder 1 selects a predetermined word line to be later described, and turns "ON" a memory cell connected to the selected word line. A Y decoder 2 selects a predetermined data line (which will be described in detail later) and applies data in the form of a voltage to the selected data line. A write circuit 3 selects a predetermined word line (to be described later) and writes the data in a predetermined memory cell connected to the selected word line. A sense amplifier 4 selects a predetermined data line (to be described later) and reads the data from a predetermined memory cell connected to the selected data line.

Each of the symbols WL_1, WL_2, ..., WL_m represents a word line, one end of which is connected to the X decoder 1 and the other end of which is connected to the write circuit 3. A plurality of these word lines, disposed in the Y direction so as to extend laterally in the X direction, turn "ON" the memory cells connected to them and write the data. Symbols DL_1, DL_2, ..., DL_n represent data lines each of which have

one end connected to the Y decoder 2 and the other end connected to the sense amplifier 4, and a plurality of data lines are disposed in the X direction so as to extend in the Y direction. They transmit the data of the memory cells M_{11}, M_{12}, ..., M_{nm}, disposed at the points of inter section between the word lines WL and the data lines DL. Each memory cell M has a floating gate and a control gate connected to the predetermined word line WL. Each memory cell consists of a field effect transistor Q. One of the ends of the transistor Q is connected to the predetermined data line DL with the other end being earthed. A plurality of memory cells in a matrix form a memory cell array.

Next, the construction of this device will be described in more detail with reference to Figs. 2 to 4. Inter-layer insulating layers to be disposed between conductive layers are not shown in Figure 2 for ease of illustration.

In Figures 2 to 4, a field insulating layer 6 is disposed between regions where semiconductor devices are to be formed, on one main surface of a p^--type semiconductor substrate 5 consisting of, e.g. silicon

single crystal. This field insulating layer 6 is to electrically isolate the semiconductor devices from one another. A p-type channel stopper region 7 is disposed on the main surface of the semiconductor substrate 5 below the field insulating layer 6 in order to further isolate electrically the semiconductor devices from one another.

Reference numerals 8 and 8A represent insulating layers that are disposed on the main surface of the semiconductor substrate 5 in the regions where the semiconductor devices are to be formed. The insulating layer 8 primarily forms the gate insulating layer of a field effect transistor. A conductive layer 9 is disposed at a predetermined portion on the insulating layer 8 so as to constitute the floating gate (FG) of a memory cell of an EPROM. Reference numeral 10 represents an insulating layer which is disposed so as to cover the upper portion of the conductive layer 9. This layer 10 primarily isolates electrically the conductive layer 9 from another to be disposed on the conductive layer 9. Reference numeral 11 represents a plurality of conductive layers arranged in the Y direction and disposed on a plurality of conductive layers 9 that are arranged in the X direction via the insulating layer 10. The conductive layer 11 constitutes a control gate (CG) of the memory cell of the EPROM in the region where the semiconductor device is to be formed, that is, on the conductive layer 9, and forms the word line (WL) of the EPROM at the rest of the portions thereof.

Reference numeral 12 represents an insulating layer which is disposed in close contact with the sides of conductive layers 9, 11, or with the side of the conductive layer 9, and is disposed to cover at least sides of the insulating layer 8 serving as the gate insulating layer and to cover sides of insulating layer 10. The insulating layer 12 consists, for example, of a densified (compact) silicon oxide layer which is prepared by baking a silicon oxide layer which has been formed by chemical vapor deposition (hereinafter called "CVD"), the baking being performed for rendering the silicon oxide layer formed by CVD denser (compact). The insulating layer 12 is disposed in such a manner as to cover at least sides of the insulating layer 8, interposed between the conductive layer (FG) 9 and the semiconductor substrate 5. The thickness of this insulating layer 12 is equal to, or greater than, the thinner of the insulating layer 6 and the insulating layer 10. The insulating layer 12 restricts the leakage of charge that would otherwise occur between the conductive layers, or the leakage of charge that would otherwise occur at the upper surface of the insulating layer 8A, and thus improves the retention characteristics of the charge as the data to be stored in the conductive layer 9.

Since sides of the insulating layer 10 interposed between the conductive layer (FG) 9 and the conductive layer (CG) 11 are covered with the insulating layer 12, heat-treatment for an extended period of time for thermal

oxidation is not necessary. Accordingly, lift-up at the edge of the conductive layer (CG) 11 does not occur, and the drop of capacitance formed by the conductive layers 9 and 11 can be prevented. This means that the efficiency in the write and read modes of the memory cell can be improved, and the reliability as well as operating speed can also be improved in the read mode. Furthermore, the insulating layer 12 is arranged so as to mitigate the acute step that would otherwise be formed by the conductive layers 9 and 11. Accordingly, depositability of the conductive layer, which is to be deposited on the insulating layer 12 and consists of Al, for example, can be improved.

Reference numeral 13 represents an insulating layer which is disposed on the conductive layer 11 so as to come into contact with the insulating layer 12. An n^+-type semiconductor region 14 is disposed extending to the main surface of the semiconductor substrate 5 on both sides of the conductive layers 9 and 11 where the semiconductor device is to be formed. The n^+-type semiconductor region 14 is used as the source or drain region, or as a ground line (GL), and forms part of the memory cell of the EPROM.

The memory cell M of the EPROM, that is, the field effect transistor Q, consists primarily of the semiconductor substrate 5, the conductive layer 9 disposed on the substrate 5 via the insulating layer 8, the conductive layer 11 disposed on the conductive layer 9 via the insulating layer 10, and the pair of semiconductor regions 14.

An insulating layer 15 is disposed on the field insulating layer 6 and the insulating layers 8, 8A, 12, and 13 in such a manner as to cover the semiconductor devices and to electrically isolate them from a conductive layer to be disposed on them. The insulating layers 8A, 15 on the predetermined semiconductor region 14 are selectively removed, and a contact hole 16 is disposed to establish electric connection with a conductive layer to be disposed on the insulating layer 15. A plurality of conductive layers 17 are disposed so as to electrically connect with the predetermined semiconductor regions 14 via the contact holes 16 and to extend in the Y direction while crossing the conductive layer (WL) 11 on the insulating layer 15. The conductive layers 17 constitute the data lines (DL) of the EPRCMs.

Next, the dependence of the retention characteristics of charge, as the data, upon the film thickness of the insulating layer 12, which is disposed sideways of the conductive layers 9 and 11 of the memory cell, will be described.

Figure 5 is a diagram showing the dependence of the retention characteristics of the charge, as the data, upon the thickness of the insulating layer 12, and Figures 6(A) through 6(C) are sectional views of the principal portions of the memory cell (model) of an EPROM in which the film thickness of the insulating layer 12 is variable.

Referring to Figure 5, the abscissa represents the temperature dependence [1/T (C)] of the holding characteristics of the charge, as the data, and the ordinate represents the logarithm [log (hr)] of the holding time of the charge as the data. The lines (A), (B) and (C) correspond to the models shown in Figures 6(A), 6(B) and 6(C), respectively.

In Figures 6(A) through 6(C), Figure 6(A) represents the model in which no compact silicon oxide layer, to cover sides of conductive layers 9, 11 that are patterned by self-alignment, is used. Figure 6(B) shows the model in which compact silicon oxide layer 12A, formed by thermal oxidation to cover sides of the conductive layers 9, 11 that are patterned by self-alignment, is formed in a thickness about 1/2 the thickness of the insulating layer 8. Figure 6(C) shows the model in which compact silicon oxide layer 12B, formed by thermal oxidation to cover the conductive layers 9, 11 that are patterned by self-alignment, is formed in a film thickness which is equal to, or greater than, the smaller of the film thickness of the insulating layers 8 and 10. As can be appreciated from these Figs. 6(A) through 6(C), the thickness of the layers 12A and 12B are measured parallel to the surface of the semiconductor substrate.

As can be seen clearly from Figures 5 and 6(A) through 6(C), the retention time of the charge, as the data,

can be improved by covering sides of conductive layers 9, 11 with the silicon oxide layer 12B.

In this device, the silicon oxide layer 12B having a film thickness equal to, or greater than, the smaller of the film thickness of the insulating layers 8 and 10 covers edges of the conductive layers 9, 11, so that it becomes possible to restrict the charge stored in the conductive layer 9 from leaking from the edge portion of the conductive layer 9 to the semiconductor substrate 5 or to the conductive layer 11, and to improve the retention characteristics of the charge. However, when the silicon oxide layer 12B is formed by thermal oxidation, a heat-treatment step for an extended period is necessary, and this causes lift-up at the end portions of the conductive layers 9, 11 such as the conductive layers 9A, 11A as indicated by dotted lines in Figure 6(C). This is because the growing speed of the oxide film at the end portions of the conductive layers 9 and 11 is greater than that on the main surface of the semiconductor substrate 5. Accordingly, this device uses an insulating layer 12 that is prepared by baking a silicon oxide layer formed by CVD, for example, in place of the silicon oxide layer 12B formed by thermal oxidation. Such baking makes such silicon oxide layer formed by CVD denser. Preferably, its film thickness is equal to, or greater than, the smaller of the film thickness of the insulating layers 8 and 10.

Next, a method of production of this device will be described.

Figures 7(A) through 7(J) are sectional views showing principal portions of an EPROM and are useful for explaining the production steps; and Figures 8(A) through 8(C) are sectional views taken along line VIII A - VIII A of Figure 7(B), line VIII B - VIII B of Figure 7(C) and line VIII C - VIII C of Figure 7(J), respectively. Figures 9(A) through 9(J) are sectional views of principal portions of peripheral circuitry of an EPROM and are useful for explaining the production method.

In the drawings, an insulated gate field effect transistor (hereinafter called "MISFET") forming peripheral circuitry is shown so as to correspond to each production step of the memory cell of the EPROM.

First of all, a p^--type semiconductor substrate 5 consisting of silicon single crystal is prepared. A field insulating layer 6 is then formed on the main surface of the semiconductor substrate 5 at the portion between the regions where the semiconductor devices are to be formed. A p-type channel stopper region 7 is formed on the main surface of the semiconductor substrate 5 below the field insulating layer. The field insulating layer 6 is formed by selective thermal oxidation of the semiconductor substrate 5. The channel stopper region 7 is formed by introducing a p-type impurity by ion implantation, and then subjecting the impurity to drive-in diffusion by thermal oxidation. The

techniques for forming the channel stopper region, and for forming the field insulating region, are conventional. As shown in Figures 7(A) and 9(A), an insulating layer 8 is formed on the main surface of the semiconductor substrate 5 in the region where the semiconductor device is to be formed. It is formed by thermal oxidation of the semiconductor substrate 5, for example, and its film thickness is, e.g., about 500 (A°), so that a gate insulating layer can be provided.

After the step shown in Figure 7(A) and Figure 9(A), the floating gate of the memory cell of the EPROM and the gate of the MISFET of the peripheral circuit are formed. For this purpose, a first conductive layer of the production process, e.g., a polycrystalline silicon layer about 3,500A° thick, is formed on the field insulating layer 6 and on the insulating layer 8, and P in a high concentration is introduced into the polycrystalline silicon layer by thermal diffusion or ion implantation primarily so as to reduce the resistance. This polycrystalline silicon layer is then patterned in a predetermined pattern, thereby forming a polycrystalline silicon layer 9B to constitute the floating gate in the region in which the memory cell of the EPROM is to be formed, and forming also a polycrystalline silicon layer 9B to constitute the gate electrode 9C of the MISFET in the region in which a MISFET of the peripheral circuit is to be formed.

Then, an insulating layer 10A is formed in such a manner as to cover the polycrystalline silicon layer 9B and the gate electrode 9C, as illustrated in Figures 7(B), 8(A) and 9(B). This layer can be formed, for example, by thermally oxidizing the polycrystalline silicon layer 9B in a film thickness of, e.g., about 500 (Å).

After the step shown in Figures 7(B), 8(A) and 9(B), the control gate of the memory cell of the EPROM and word lines (WL) are formed as shown in Figures 7(C), 8(B) and 9(C). For this purpose, a second conductive layer of the production process, e.g., a polycrystalline silicon layer 11B which has a film thickness of, e.g., about 3,500 (A°) and into which P is doped in a high concentration, to lower the resistance of this polycrystalline silicon layer, is formed on the insulating layer 10A and on the field insulating layer 6.

After the step shown in Figures 7(C), 8(B) and 9(C), the polycrystalline silicon layer 11B, the insulating layer 10A and the polycrystalline silicon layer 9B are patterned in the region where the memory cell of the EPROM is to be formed, thereby forming the conductive layer 11 serving as the control gate (CG) and the word lines (WL), the conductive layer 9 serving as the floating gate and the insulating layer 10 interposed between these conductive layers. As shown in Figures 7(D) and 9(D), the insulating layer 8 at the portions other than the portion below the conductive layer 9, the insulating layer 8 at the portions

other than the portion below the gate electrode 9C, and the insulating layer 10A formed so as to cover the gate electrode 9C, are selectively removed, exposing the upper surface portion of the conductive layer 11, the upper surface portion of the gate electrode 9C and the predetermined upper surface portion of the semiconductor substrate 5.

After the step shown in Figures 7(D) and 9(D), an insulating layer 12A is formed over the entire surface as shown in Figures 7(E) and 9(E). The insulating layer 12A consists, for example, of a silicon oxide (e.g., silicon dioxide) layer formed, e.g., by CVD, and its film thickness may range, for example, from about 5,000 to about 10,000 A°.

After the step shown in Figures 7(E) and 9(E), the insulating layer 12A is etched anisotropically by reactive ion etching or the like, as known in the art, in a depth corresponding to its film thickness. Thus, for formation of an oxide sidewall, see, for example, the article by Tsang, et al., "Fabrication of High-Performance LDDFET's with Oxide Sidewall-Spacker Technology", in IEEE Transactions on Electron Devices, Vol. ED-29, No. 4 (April 1982), pp. 590-6.

As shown in Figures 7(F) and 9(F), an insulating layer 12B is formed on the sides of the conductive layers 9 and 11 so as to cover the sides of insulating layers 8 and 10 and to reach the upper surface of the conductive layer 11, and an insulating layer 12B reaching the upper surface portion of

the gate electrode 9C is formed on the side of the gate electrode 9C. The film thickness of the insulating layer 12B is equal to, or greater than, the smaller of the thicknesses of the insulating layers 8 and 10.

After the step shown in Figures 7(F) and 9(F), heat-treatment is conducted to bake, so as to densify the insulating film 12B as shown in Figures 7(G) and 9(G), providing a compact (dense) insulating layer 12. At the same time, an insulating layer 8A is formed on the upper surface portion of the semiconductor substrate 5 in which the semiconductor regions to be used as the source or drain region is to be formed, and an insulating layer 13 is formed on the conductive layer 11 and on the gate electrode 9C. The insulating layer 13 is disposed as a mask for introduction of an impurity for forming the semiconductor region, and to prevent the contamination by an unnecessary impurity that would affect adversely the electric characteristics of the EPROM. Oxidation in wet O_2 or dry O_2 at about 800 to about 1000°C for 10 - 30 min may be used for the heat-treatment. As a result of the heat-treatment, approximately a 500A°-thick insulating layer 13, for example, is formed on the conductive layer 11 and on the gate electrode 9C. After the step shown in Figures 7(D) and 9(D), a thin insulating layer (for example, of a thickness of up to about 300 A°) can be formed by thermal oxidation so as to cover the conductive layers 9, 11 and the gate electrode 9C. Then, the insulating layer 12 is formed. Such thin insulating layer

can act to improve the adhesion of the conductive layers 9 and 11, and the gate electrode 9C, with the insulating layer 12.

Incidentally, this is advantageous from the aspect of the production process because the insulating layers 8A and 13 can be formed simultaneously with the insulating layer 12.

After the step shown in Figures 7(G) and 9(G), an n^+-type semiconductor region 14 to serve as the source or drain region is formed in the main surface portion of the semiconductor substrate 5 at both sides of the conductive layers 9, 11 and the gate electrode 9C in the regions where the semiconductor devices are to be formed, through the insulating layer 8A, mainly using the insulating layer 12, conductive layers 9, 11, gate electrode 9C and the field insulating layer 6 as masks for implanting the impurity, as shown in Figures 7(H) and 9(H). This region 14 can be formed, for example, by ion implantation of As ion impurity in a dose of $1x10^{16}$ (atoms/cm^2), for example, at an energy of, e.g., about 70 to about 90 (KeV). The insulating layer 12 reduces the diffusion quantity into the regions where the memory cell of the EPROM and the channel of a MISFET of the peripheral circuit are to be formed. The mirror capacity formed by the conductive layer 9 and the semiconductor region 14 and by the gate electrode 9C and the semiconductor region 14 can be reduced. Accrodingly, the operating speed of the EPROM and its peripheral circuit can be improved. The semiconductor

region 14 is formed after the formation of the insulating layer 12, and since no heat-treatment step for an extended period is thereafter performed in the production process, excessive drive-in diffusion is not effected. For this reason, a sufficient effective channel length can be obtained and the short channel effect can be prevented.

After the step shown in Figures 7(H) and 9(H), an insulating layer 15 is formed over the entire surface as shown in Figures 7(I) and 9(I). The layer 15 can be formed, for example, of a phosphosilicate glass (PSG) layer whose upper surface portion can be made flat and smooth by glass flow. The acute step shape defined by the conductive layers 9, 11 and the gate electrode 9C is mitigated by the insulating layer 12 so that the upper surface portion of the insulating layer 15 is made flatter and smoother.

After the step shown in Figures 7(I) and 9(I), the insulating layers 8A and 15 on the predetermined semiconductor region 14 are selectively removed to define a contact hole 16. As shown in Figures 7(J), 8(C) and 9(J), third conductive layers 17, 17A of the production process are then formed on the insulating layer 15 so that they can be electrically connected with the predetermined semiconductor region 14 via the contact hole 16. The third conductive layers can be provided by use of an aluminum layer prepared by sputter deposition, for example. Though the aluminum layer has a relatively low resistance value, its depositability is low at the acute step portion.

However, since the upper surface portion of the insulating layer 15 has been made relatively flat and smooth as described above, depositability of te aluminum layer is high so that the reliability in multi-layered wiring technique can be improved.

The EPROM of this device can be completed after the series of production steps described above. Thereafter, post-treatment such as deposition of a protective film may be carried out.

Incidentally, the insulating layer 12B formed in Figure 7(F) may be formed in such a manner as shown in Figure 7(K).

After the step shown in Figure 7(E), the anisotropic etching of the insulating layer 12A is controlled so that the insulating layer 12C covering the insulating layers 8 and 10 may be formed as shown in Figure 7(K).

In the description given above, the insulating layer 12 is formed using a silicon oxide layer prepared by CVD, but the insulating layer 12 may be formed using a silicon oxide layer prepared by sputtering or plasma CVD, or such insulating layer 12 can be a densified layer prepared by baking and densifying a phosphosilicate glass layer

having a low concentration (less than 4 mol %) of phosphorus that does not generate glass flow at temperatures used during processing after depositing the phosphosilicate glass.

In the description given above, the gate electrode 9C constituting a part of the MISFET of the peripheral circuit of an EPROM is composed of the first conductive layer of the production process, but it may be composed of the second conductive layer of the production process.

Next, another production method different from that described above will be discussed.

Figures 10(A) through 10(D) are sectional views showing principal portions of an EPROM and are useful for explaining the production steps of this second production method.

After the step shown in Figure 7(E) ~~[of Embodiment 1]~~ (that is, formation of silicon oxide layer 12A), heat-treatment is carried out so that an insulating layer 12E is formed by densifying the insulating layer 12A as shown in Figure 10(A). Since the semiconductor region to serve as the source or drain region is not yet formed, the insulating layer 12E can be formed by steam or dry-O_2 oxidation at a relatively high temperature of from 800 to 1,000°C, for example.

After the step shown in Figure 10(A), anisotropic etching is conducted in the same way ~~[as in Embodiment 1]~~ thereby forming the insulating layer 12 as shown in Figure 10(B).

After the step shown in Figure 10(B), heat-treatment is carried out to form the insulating layers 8A and 13 as shown in Figure 10(C).

After the step shown in Figure 10(C), the n^+-type semiconductor regions 14, to serve as the source or drain region, are formed in the main surface portion of the semiconductor substrate 5 through the insulating layer 8A, as shown in Figure 10(D).

After the step shown in Figure 10(D), the steps shown in Figure 7(I) ~~[and so forth of Embodiment 1]~~ are conducted in the same way.

After the series of the production steps described above are carried out, an EPROM of this device can be completed.

Embodiment

Now a device being an embodiment of the present invention will be described.

Figure 11 is a sectional view of principal portions of an EPROM and is useful for explaining the construction of an Embodiment of the present invention, and Figure 12 is a sectional view taken along line XII - XII of Figure 11.

In these drawings, reference numeral 14A represents an n^--type semiconductor region which is disposed in the main surface portion of the semiconductor substrate 5 at the portion between the region in which the channel of the field effect transistor as the memory cell of EPROM is

to be formed and the semiconductor region 14, this n^--type semiconductor region being in electric contact with these regions. This n^--type semiconductor region is effective when the drive-in diffusion quantity to the region beneath the insulating layer 12 is not sufficient, or when the junction withstand voltage between the semiconductor region 14 serving as the drain region of the field effect transistor and the semiconductor substrate 5 is to be improved.

Next, the production method of this embodiment will be described.

Figure 13 is a sectional view of principal portions of an EPROM in the production process and is useful for explaining the production method of this Embodiment.

After the step shown in Figure 7(D) above, n^--type semiconductor regions 14A are formed on both sides of the conductive layers 9 and 11, using the conductive layer 11 and the field insulating layer 6 as masks for introducing an impurity, as shown in Figure 13. The n^--type semiconductor regions 14A may be formed by implanting As ion impurity or P ion impurity of $1x10^{14}$ to $1x10^{15}$ (atoms/cm^2) at 70 to 90 (KeV), for example. When implanting the impurity ion to form the semiconductor regions 14A, it is also possible to dispose an insulating layer which covers the upper surface portions of the conductive layers 9, 11 and semiconductor substrate 5 and functions as a mask for the ion implantation, and then to

remove the insulating layer after the implantation of the impurity by thermal diffusion or the like.

After the step shown in Figure 13, the steps shown in Figure 7(E) and so on may be carried out.

After the series of these production steps, an EPROM of this Embodiment can be completed.

Incidentally, this embodiment is not particularly limited to the method of Figs. 7 to 9 and the production method of Fig. 10 can also be applied.

In this embodiment, a MISFET of the peripheral circuit shown in Figures 9(A) to 9(J) above may also have the same structure (e.g., such n^--type semiconductor region). In other words, the n^--type semiconductor region is formed simultaneously with the step shown in Figure 13 under the state shown in Figure 9(D). Thereafter, the source and drain regions of MISFET of the peripheral circuit can be formed by the n^+-type semiconductor region 14 and the n^--type semiconductor region 14A when the production steps shown in Figure 9 are thereafter followed. This arrangement provides the effect that the breakdown voltage of the junction of the MISFET can be improved and the occurrence of hot carriers can be restricted.

Other features of this embodiment may be similar to the devices discussed above with reference to Figs. 1 to 10 and will not be discussed in more detail now.

Thus in a semiconductor integrated circuit device according to the present invention, with a conductive layer to function as a gate, and an insulating layer between the gate and the substrate, the following results may be achieved.

(1) A first insulating layer consisting, for example, of the baked and densified (compact) silicon oxide layer may be provided on the side of the first conductive layer so as to cover at least the gate insulating layer for the field effect transistor. This arrangement makes it possible to restrict the leakage of the charge, as the data, stored in the first conductive layer, to the semiconductor substrate, so that the charge retention characteristics of the field effect transistor can be improved.

(2) The first insulating layer having a film thickness greater than that of the gate insulating layer may be provided on the side of the first conductive layer so as to cover at least the gate insulating layer. This arrangement makes it possible to restrict the leakage of the charge, stored in the first conductive layer, to the semiconductor substrate, so that the charge retention characteristics of the field effect transistor can be

improved.

(3) A field effect transistor including conductive layers may be provided in which the conductive layers including a first conductive layer, and a second conductive layer to function as a control gate on the first conductive layer via an inter-layer insulating layer. A first insulating layer may be provided on both sides of the conductive layers so as to cover at least the gate insulating layer and the inter-layer insulating layer. According to this arrangement, the leakage of the charge stored in the first conductive layer to the semiconductor substrate and to the control gate may be restricted so that the retention characteristics of the charge, as the data, by the field effect transistor can be improved. Moreover, since lift-up, particularly at the end portions of the second conductive layer can be prevented, the drop of the parasitic capacitance formed by the first and second conductive layers may be prevented or at least reduced.

(4) Since the drop of the parasitic capacitance may be restricted as discussed at (3) above, the reliability and operating speed in the write and read modes of the data may be improved.

(5) An insulating layer capable of mitigating the acute step shape may be provided on the sides of the conductive layers, so that the upper surface of the insulating layer disposed thereon can be made

relatively flat and smooth, and depositability of further layers, including an upper conductive layer, can be improved.

(6) An insulating layer capable of mitigating the acute step shape may be provided on the sides of the conductive layers of the field effect transistor and on the sides of other portions such as on the sides of the gate electrode of a MISFET, so that the upper surface portion of an insulating layer to be disposed thereon can be made relatively flat and smooth, and the depositability of further layers, including an upper conductive layer disposed on the upper surface portion of the insulating layer, can be improved.

(7) After an insulating layer is formed on the sides of the conductive layer, a pair of semiconductor regions to be used as the source or drain region are formed. This arrangement eliminates the necessity of heat-treatment for an extended period which would otherwise cause excessive diffusion of the semiconductor regions. Accordingly, semiconductor regions having a shallow junction depth may be provided.

(8) Due to the effect described at (7) above and to the effect brought forth by the second insulating layer, excessive diffusion of the semiconductor region into the channel of the field effect transistor is restricted, and a sufficient effective channel length may

be obtained. Therefore, the short channel effect can be prevented or at least reduced.

(9) Due to the effect described at (7) above and to the effect brought forth by the second insulating layer, unnecessary drive-in diffusion of the semiconductor regions into the channel of the field effect transistor is restricted, so that the mirror capacity formed by the conductive layer and the semiconductor region may be reduced.

(10) Since the mirror capacity can be reduced as described at (9), the operating speed may be improved.

(11) Due to the effects described above at (1) to (6) and (8), the retention characteristics of the charge, as data, can be improved, the deposition of further layers, including an upper conductive layer, may be made easier, and the short channel effect can be prevented. Thus, the reliability of the semiconductor integrated circuit device may be improved.

(12) The operating speed of the semiconductor integrated circuit device may be improved by the effects described at (4), (7) and (9).

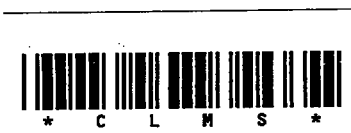
(13) The integration density of the semiconductor integrated circuit device can be improved because its reliability can be improved by the effects described at (1) to (4), (7), (8) and (11).

Although the present invention has thus been described with reference to an embodiment thereof,

the present invention is not limited to them, but can be achieved in various ways.

For example, although the foregoing embodiments have been described with reference to the case in which the memory cell of an EPROM is provided in the semiconductor substrate per se, the memory cell of an EPROM may be disposed in a well region after forming such a well region in a semiconductor substrate. Thus, the present invention contemplates such well region as a "semiconductor substrate" for forming the memory cell.

Although the foregoing embodiments have been described with reference to the case in which a MISFET is used as the peripheral circuit of EPROM, it may be a complementary MISFET or a bipolar transistor.



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CLAIMS:

1. A semiconductor device having:

a first conductive layer separated by a first insulating layer from a semiconductor substrate;

a second insulating layer adjacent and covering sides of the first insulating layer, the second insulating layer being a dense insulating layer sufficiently dense substantially to prevent charge leakage from the first conductive layer;

a second conductive layer separated by a third insulating layer from the first conductive layer;

two semiconductor regions in the substrate at the sides of the first conductive layer, the two semiconductor regions being of the same conductivity type and of opposite conductivity type to the part of the substrate adjacent the first conductive layer, whereby there is field effect transistor with the part of the substrate adjacent the first conductive layer being a channel of that transistor, the first conductive layer being a floating gate of the transistor, the second conductive layer being a control gate of the transistor, and the first insulating layer being the gate oxide layer of the transistor; and

further semiconductor regions having the same conductivity type as, but a lower impurity concentration than, the two semiconductor regions, and being respectively between the part of the substrate being the channel of the transistor and each of the two semiconductor regions.

* C L M S *

2. A semiconductor device according to claim 1, wherein the second conductive layer is of polycrystalline silicon.

3. A semiconductor device according to claim 1, wherein the second conductive layer is of a metal having a high melting point.

4. A semiconductor device according to claim 1, wherein the second conductive layer is a compound of silicon and a metal having a high melting point.

5. A semiconductor device according to claim 1, wherein said second conductive layer comprises a polycrystalline silicon layer and a silicide layer of a metal having a high melting point thereon.

6. A semiconductor device according to any one of the preceding claims, wherein the two semiconductor regions are As ion impurity regions in the substrate.

7. A semiconductor device according to any one of the preceding claims, wherein the further semiconductor regions are P ion impurity regions in the substrate.

8. A semiconductor device according to any one of the preceding claims, wherein the second insulating layer is a silicon oxide layer formed by deposition and baked to achieve a suitable density.

9. A semiconductor device according to any one of claims 1 to 7, wherein the second insulating layer is a silicon oxide layer formed by chemical vapour deposition.

10. A semiconductor device according to any one of claims 1 to 7, wherein the second insulating layer is a low

concentration phosphosilicate glass film which has not been subjected to glass flow.

11. A semiconductor device according to any one of claims 1 to 7, wherein the second insulating layer is a silicon oxide layer formed by sputtering.

12. A semiconductor device according to any one of claims 1 to 7, wherein the second insulating layer is a silicon oxide layer formed by plasma chemical vapour deposition.

13. A semiconductor device according to any one of the preceding claims, wherein the first conductive layer is of polycrystalline silicon.

14. A semiconductor device according to any one of the preceding claims, wherein the second insulating layer extends on the substrate over the semiconductor regions.

15. A semiconductor device substantially as herein described with reference to and as illustrated in Figs. 11 to 13, of the accompanying drawings.

16. A semiconductor device according to any one of the preceding claims, being an EPROM.

17. A method of producing a semiconductor device comprising:

forming a first conductive layer on a first insulating layer which separates the first conductive layer from the substrate;

forming a second insulating layer adjacent and covering sides of the first insulating layer, the second

insulating layer being a dense insulating layer of sufficient density substantially to prevent charge leakage from the first conductive layer;

forming a third insulating layer on the first conductive layer;

forming a second conductive layer on the third insulating layer;

forming two semiconductor regions of a first conductivity type in the substrate; that part of the substrate between the two regions being of a second conductivity type opposite to the first, the two semiconductor regions being source and drain regions of a field effect transistor with that part of the substrate therebetween forming the channel of the field effect transistor, the first conductive layer forming a floating gate of the field effect transistor, the second conductive layer forming a control gate of the field effect transistor, and the first insulating layer being the gate insulating layer of the field effect transistor; and

forming further semiconductor regions of the same conductivity type as, but a lower impurity concentration than the two semiconductor regions, the further semiconductor regions being respectively between the part of the substrate forming the channel of the transistor and each of the two semiconductor regions.

18. A method according to claim 17, wherein the step of forming the second insulating layer comprises forming a

silicon oxide layer covering the or each conductive layer, removing selectively the silicon oxide layer at parts other than at both sides of each conductive layer, and then baking the silicon oxide layer for densification.

19. A method according to claim 17, wherein the step of forming the second insulating layer comprises forming a silicon oxide layer to cover each conductive layer, baking the silicon oxide layer for densification, and thereafter removing selectively the silicon oxide layer at parts other than at both sides of the or each conductive layer.

20. The method according to claim 17, wherein the step of forming the second insulating layer includes depositing a silicon oxide layer and baking the silicon oxide layer to densify the silicon oxide layer, and the step of forming the pair of semiconductor regions includes introducing impurity ions into the semiconductor substrate, and wherein said depositing and baking are performed prior to the introduction of impurity ions.

21. The method according to claim 17, wherein the step of forming the second insulating layer includes deposition of material for forming the second insulating layer and baking for densification thereof, and is performed prior to the step of forming the pair of semiconductor regions, including introduction of impurity ions into the semiconductor substrate, whereby the extent of diffusion of the impurity ions to a region of the semiconductor substrate beneath the conductive layers is limited.

22. A method according to any one of claims 17 to 21, wherein the step of forming the two semiconductor regions is performed after the step of forming the second insulating layer.

23. A method of producing a semiconductor device substantially as any one herein described with reference to Figs. 11 to 13 of the accompanying drawings.