"HUE CONTROL CIRCUIT"

The invention relates to a hue control circuit comprising a setting element for adjusting the phase of a colour synchronising signal relative to that of a colour television chrominance signal to be demodulated without substantially affecting the amplitude of either signal.

United States Patent 3 518 363 discloses such a hue control circuit wherein the phase of the colour synchronising signal is influenced by detuning a circuit with the aid of a capacitance arranged in parallel with an adjustable portion of a potentiometer connected across a portion of the circuit. The connections to the potentiometer then carry an a.c. voltage as a result of which the circuit is critical as regards the position of its several parts.

The invention has for its object to provide a hue control circuit such that the setting element may be provided in an appropriate position and that the remaining portion of the circuit can be constructed substantially as an integrated circuit.

The invention provides a hue control circuit of the type described in the opening paragraph which is characterised in that the hue control circuit has an input which is coupled to an adder circuit via a first control circuit and via a circuit which shifts the phase substantially through 90° and a second control circuit, the first and second control circuits being adjustable by means of a d.c. voltage which can be varied by the setting element, the first control circuit having a substantially cosinusoidal effect and the second control circuit a substantially sinusoidal effect on the amplitude of the signal conveyed through the respective control circuit as a function of the deviation of the d.c. voltage from that produced by the setting element in its normal position.

As the setting element now produces a d.c. voltage its position in the circuit is not critical. In addition, the control circuits and the circuit which shifts the phase through 90° can be constructed almost wholly in integrated circuit form.

The invention will now be further described by way of example

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with reference to the accompanying drawings. In the drawings:

Figure 1 illustrates by means of a block diagram an embodiment of a hue control circuit according to the invention and

Figure 2 illustrates by means of a circuit diagram a possible embodiment of a portion of a hue control circuit as shown in Figure 1.

In Figure 1, a chrominance signal from a colour television signal is applied to the input 1 of a variable gain amplifier 3. An output 5 of the amplifier 3 is connected to an input 7 of a demodulation circuit 9, to an input 11 of a first control circuit 13 and to an input 15 of a circuit 17 which produces a phase shift of substantially 90°.

An output 19 of the phase-shifting circuit 17 applies a 90° phase shifted chrominance signal to an input 23 of a second control circuit 25 via an amplitude control circuit 21.

A pair of outputs 27 and 29, respectively of the first and second control circuits 13 and 25 are respectively connected to a pair of inputs 31 and 32 of an adder circuit 35.

To the input 11 of the first control circuit 13 a first detection circuit comprising a diode 37 and a capacitor 39 is connected and to the input 23 of the second control circuit 25 a second detection circuit comprising a diode 41 and a capacitor 43.

The first (37, 39) and second (41, 43) detection circuits respectively apply to inputs 45 and 47 of a difference-determining circuit 49, a voltage respectively representing the amplitude of the chrominance signal at the inputs 11 and 23 of the respective first and second control circuits 13 and 25. The difference-determining circuit 49 applies to a control signal input 51 of the amplitude control circuit 21 a control signal which renders the amplitude of the signal at the input 23 of the second control circuit 25 equal to the amplitude of the signal at the input 11 of the first control circuit 13 without the amplitude of the signal at the input 11 of the first control circuit 13 being influenced.

The first and second control circuits 13 and 25, respectively

have a respective control signal input 33 and 55 to which an adjustable d.c. voltage originating from a setting element 57 in the form of a potentiometer is applied. In a normal position of the wiper of this potentiometer 57 the first control circuit 13 supplies from its output 27 the maximum output singal amplitude and the second control circuit 25 supplies from its output 29 a signal amplitude equal to zero. The output signal amplitude of the first and second control circuits 13 and 25, respectively vary substantially cosinusoidally and sinusoidally versus the deviation of the d.c. voltage supplied in the normal position by the potentiometer 57. As a result thereof the amplitude of the chrominance signal appearing at an output 59 of the adder circuit 35 is substantially not influenced by the setting of the potentiometer 57, while the phase thereof is adjustable by means of the potentiometer 57 with respect to the phase of the chrominance signal at the input 7 of the demodulation circuit 9.

The colour synchronising signal of the chrominance signal at the output 59 of the adder circuit 35 is conveyed by way of a gate circuit 61 to the respective inputs 63 and 65 of a phase detection and amplitude-detection circuit 67 and 69 to respective further inputs 71 and 73 of which a reference signal received from an output 75 and 77, respectively of an oscillator circuit 79 is applied. A control signal received from an output 81 of the phase detection circuit 67 and applied to an input 83 of the oscillator circuit 79 adjusts the phase of the signal at its output 75 to 0° with respect to the phase of the colour synchronising signal at the input 63 of the phase detection circuit 67 and adjusts the phase of the signal at its output 77 to 90° relative thereto.

The amplitude detection circuit 69 supplies from its output 85 a control signal the value of which is substantially not influenced by the setting of the potentiometer 57. This control signal is applied to a control signal input 87 of the variable gain amplifier 3 which in response thereto adjusts the amplitude of the chrominance signal at its output 5 such that the amplitude of the colour synchronising signal remains constant.

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The outputs 75 and 77 of the oscillator circuit 79 are further connected to respective inputs 89 and 91 of the demodulation circuit 9 for applying reference signals thereto with the aid of which the colour difference signals from the chrominance signal are demodulated. So the demodulation axes of the chrominance signal can be rotated by the potentiometer 57 without the control signal at the control signal input 87 of the variable gain amplifier 3 producing a change in amplitude when the position of the potentiometer 57 is changed. As a result thereof only the hue and not the colour saturation is influenced on display.

Figure 2 shows a circuit diagram of an advantageous embodiment of that portion of the circuit shown in Figure 1 which is comprised between the output 5 of the controllable amplifier 3 and the output 59 of the adder circuit 35 and the input 7 of the demodulation circuit 9. Corresponding parts have been given the same reference numerals as in Figure 1.

The output 5 of the amplifier 3 is the output of an emitter follower 101, 103 to an input 102 of which the chrominance signal CHR 0° is applied of which the phase is not influenced.

The 90° phase-shifting circuit 17 is formed by a resistor 105 connected to the output 5 of the emitter follower 101, 103, by a differential amplifier comprising two transistors 107, 109 the emitters of which are each connected via a resistor 111, 113 to a current source 115, and by a capacitor 117 connected between the collector and the base of the transistor 107. The base of the transistor 109 is connected via a resistor 119 to the output of an emitter follower 121, 123 whose input 125 is connected to a d.c. voltage V1 which is equal to the d.c. voltage level at the input 102. For that purpose, the input 125 can be connected to ground via a capacitance and to the input 102 via a resistor.

The collector of the transistor 107 is connected via a resistor 127 to the interconnected emitters of a pair of transistors 121, 123 of the amplitude control circuit 21 which further comprises a pair of transistors 125, 127 having interconnected emitters which are connected to a current

source 129. The bases of the transistors 121 and 127 are connected to a d.c. voltage V2 and the control voltage is applied to the bases of the transistors 123 and 125. The collector of the transistor 121 is connected to a resistor 131, to the collector of the transistor 125 and to the base of a transistor 133 of an emitter follower circuit which further comprises two resistors 135, 137, a transistor 139 and a resistor 141. The base of the transistor 139 is connected to the junction between the resistors 135 and 137. A negative feedback resistor can be arranged between the emitter of the transistor 133 and the input 125, for the purpose of direct current stabilisation.

Connected to the emitter of the transistor 139 is the first detection circuit comprising a diode 142 and a capacitor 143, the connection between the diode 142 and the capacitor being connected to the base of a transistor 145 of the difference-determining circuit 49. The emitter of the transistor 145 is connected to a current source 147 and to the emitter of a further transistor 149 of the difference-determining circuit 49. The base of the transistor 149 is connected to the output of the second detection circuit which comprises a capacitor 151 and a diode 153 which is connected to the output 5 of the emitter follower 101, 103.

The collector of the transistor 145 is connected to the collector of a transistor 149 via a current mirror circuit comprising three transistors 155, 157, 159 and is connected to a capacitor 161 across which a control voltage is produced which depends on the value of the difference between the amplitude of the phase-shifted chrominance signal component CHR 90° at the emitter of the transistor 139 and the amplitude of the 0° chrominance signal component CHR 0° at the emitter of the transistor 101. This control voltage is applied via an emitter follower 163, 165 to the bases of the transistors 123, 125 of the amplitude control circuit 21, which adjusts this difference substantially to zero.

The adjustable tap of the setting potentiometer 57 is connected via a resistor 171 to the base of a transistor 173 the emitter of which is connected to a current source 177 via a

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resistor 175 and, via a further resistor 179, to the emitter of a transistor 181 whose base is connected to a tap of a series arrangement of three resistors 183, 185, 187. The junction between the resistors 185, 187 is connected to the base of a pnp transistor 189 whose collector is grounded and whose emitter is connected to the base of the transistor 173. The transistor 189 forms together with the resistor 171 a limiter which ensures that the voltage at the base of the transistor 173 cannot become too high.

The collector of the transistors 173 and 181, are connected to a positive voltage via respective resistors 191 and 193. In the normal position of the sliding contact of the setting potentiometer 57 the voltage difference between these collectors is zero and in a position deviating from this normal position this voltage difference is positive or negative depending on the direction in which the sliding contact position of the potentiometer 57 deviates from the normal position.

The voltage difference between the collectors of the transistors 173, 181 is applied via a level shifting circuit comprising two diodes 195, 197 and three resistors 199, 201, 203 to the bases of a first emitter-coupled pair of transistors 205, 207 whose emitters are connected to a current source 209, the collector of the first transistor 205 being connected to the emitters of a second emitter-coupled pair of transistors 211, 213.

The voltage difference between the collectors of the transistors 173 and 181 is also applied to the bases of the transistors 211 and 213 of the second pair of transistors.

The collector of the first transistor 211 of the second pair of transistors and the collector of the second transistor 207 of the first pair of transistors are connected to the emitters of a first and a second transistor 215 and 217, respectively of a third pair of transistors. The collector of the second transistor 213 of the second pair of transistors is connected to the emitter of a first and a second transistor 223 and 225 of a fourth emitter-coupled pair of transistors via respective resistors 219

and 221.

The collector of the first transistor 215 of the third pair and the collector of the first transistor 223 of the fourth pair are connected to a connection of the output 59 and a resistor 227. The collector of the second transistor 217 of the third pair and the collector of the second transistor 225 of the fourth pair are connected to the other connection of the output 59 and to a resistor 229.

The base of the second transistor 225 of the fourth pair is connected to the output 5 of the emitter follower 101, 103 and the bases of the first and second transistors 215, 217 of the third pair and the first transistor 223 of the fourth pair are connected to the d.c. voltage at the output of the emitter follower 121, 123.

In response to the control of both the first pair 205, 207 and the second pair 211, 213 by the collector voltages of the transistors 173, 181 the current through the second transistor 213 is at a maximum at the normal sliding contact position of the setting potentiometer 57 when the voltage difference between the bases of the transistors 211 and 213 and 205, 207, respectively is zero. This current decreases both for a positive and a negative deviation of the sliding contact position of the setting potentiometer 57 relative to the normal position thereof. The change in the current through the transistor 213 is substantially cosinusoidally, depending on the voltage difference between the collectors of the transistors 173 and 181.

The amplitude of the chrominance signal component CHR 0° appearing in the balanced state at the output 59 via the fourth pair of transistors 223, 225 consequently changes over a given setting range substantially cosinusoidally versus the voltage difference. The third pair of transistors 215, 217 provides a direct current compensation so that no d.c. voltage change occurs at the output 59 when the setting of the setting potentiometer 57 is changed.

The voltage difference at the collectors of the transistors 173, 181 is further applied to the bases of a first and a second

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transistor 231 and 233, respectively of a fifth emitter-coupled pair of transistors, the emitters of which are connected to a current source 235. The collector of the first transistor 231 of this fifth pair is connected to the emitter of a first transistor 239 via a resistor 237 and to the emitter of a second transistor 243 of a sixth emitter-coupled pair of transistors via a resistor 241. The collector of the second transistor 233 of this fifth pair is connected via resistors 245 and 247, to the emitters of respective first and second transistors 249 and 251 of a seventh emitter-coupled pair of transistors.

The base of the first transistor 239 of the sixth pair and the base of the second transistor 251 of the seventh pair receive the d.c. voltage from the output of the emitter follower 121, 123 while the base of the second transistor 243 of the sixth pair and the base of the first transistor 249 of the seventh pair receive the 90°-shifted chrominance signal CHR 90° from the output of the emitter follower 139, 141.

The collectors of the first transistors 239 and 249, respectively of the sixth and seventh pairs are connected to the resistor 229 and the collectors of the second transistors 243 and 251, respectively of the sixth and seventh pairs are connected to the resistor 227. These first transistors 239 and 249 and also the second transistors 243 and 251 are controlled in anti-phase by the chrominance signal CHR 90°, so that, because in the normal position of the setting potentiometer 57 the currents through the transistors 231 and 233 of the fifth pair are equal, no 90°-component of the chrominance signal is produced across the resistors 227 and 229. When the sliding contact of this setting potentiometer 57 deviates from the normal position, a 90°-component is indeed produced across these resistors, more specifically with an amplitude which over a given setting range depends substantially sinusoidally on the deviation of the voltage difference between the bases of the transistors 231, 235 with respect to this voltage difference in the normal sliding contact position.

As a cosinusoidal 0°-component which depends on that deviation

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was developed across the resistors 227, 229 via the fourth pair of transistors a chrominance signal CHR which has an adjustable phase and a constant amplitude is produced at the output 59.

It will be obvious that if so desired the gate circuit 61 can be provided in a different place in the circuit and/or can be of a multiple construction, distributed over several places if desired.

It is further of course possible to effect the hue control in the chrominance signal to be demodulated instead of in the colour synchronising signal, for example by coupling the input 7 of the demodulation circuit 9 to the output 59 of the adder circuit 35 and the input of the gate circuit 61 to the output 5 of the amplifier 3.

If so desired, the automatic amplitude control circuit 21, 49, 37, 39, 41, 43 can be omitted, although then generally an amplitude setting will be required.

* C L M S *

CLAIMS:-

1. A hue control circuit comprising a setting element for adjusting the phase of a colour synchronising signal relative to that of a colour television chrominance signal which is to be demodulated without substantially affecting the amplitude of either signal, characterised in that the hue control circuit has an input which is coupled to an adder circuit via a first control circuit and via a circuit which shifts the phase substantially through 90° and a second control circuit, the first and second control circuits being adjustable by means of a d.c. voltage which can be varied by the setting element, the first control circuit having a substantiallycosinusoidal effect and the second control circuit a substantially sinusoidal effect on the amplitude of the signal conveyed through the respective control circuit as a function of the deviation of the d.c. voltage from that produced by the setting element in its normal position.

2. A hue control circuit as claimed in Claim 1, characterised in that included between the 90°-phase-shifting circuit and the second control circuit there is an amplitude control circuit a control signal input of which is coupled via a difference-determining circuit to a first detection circuit which is coupled to an output of the amplitude control circuit and a second detection circuit which is coupled to the input of the 90°-phase shifting circuit.

3. A hue control circuit as claimed in Claim 2, characterised in that the first control circuit comprises first, second, third and fourth pairs of emitter-coupled transistors whilst the second control circuit comprises fifth, sixth and seventh pairs of emitter-coupled transistors, the emitters of the second pair of transistors being connected to the collector of the first transistor of the first pair of transistors, the emitters of the third pair of transistors being connected to the collectors of the first transistor of the second pair and of the second transistor of the first pair, the emitters of the fourth pair being connected to the collector of the second transistor of the second

pair, the emitters of the sixth pair being connected to the collector of the first transistor of the fifth pair, the emitters of the seventh pair being connected to the collector of the second transistor of the fifth pair, the bases of the first transistor of the fifth pair and of the second transistor of the second pair being connected to a voltage which is adjustable by means of the setting element and to the base of the second transistor of the first pair via a first level shifting circuit, the bases of the second transistor of the fifth pair and of the first transistor of the second pair being connected to a voltage which can be adjusted in the opposite sense by means of the setting element and via a second level shifting circuit to the base of the first transistor of the first pair of transistors, the base of the first transistors of the sixth, third and fourth pairs and the base of the second transistor of the seventh pair being connected to a d.c. voltage, the base of the second transistor of the fourth pair being connected to the input of the 90° phase-shifting circuit, the bases of the second transistor of the sixth and of the first transistor of the seventh pair being connected to an output of the amplitude-control circuit the collectors of the first transistors of the sixth and seventh pairs being connected to the collectors of the second transistors of the third and fourth pairs and to a first resistor and the collectors of the second transistors of the sixth and seventh pairs being connected to the collectors of the first transistors of the third and fourth pairs and to a second resistor.

4. A hue control circuit substantially as herein described with reference to the accompanying drawings.

5. A hue control circuit as claimed in any of the preceding claims and formed, with the exception of the setting element, as an integrated circuit.