

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
22 February 2001 (22.02.2001)

PCT

(10) International Publication Number
WO 01/13377 A1

(51) International Patent Classification⁷: G11C 16/00

(21) International Application Number: PCT/US00/21005

(22) International Filing Date: 1 August 2000 (01.08.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/148,779 13 August 1999 (13.08.1999) US
09/417,273 13 October 1999 (13.10.1999) US

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(81) Designated States (national): CN, JP, KR, SG.

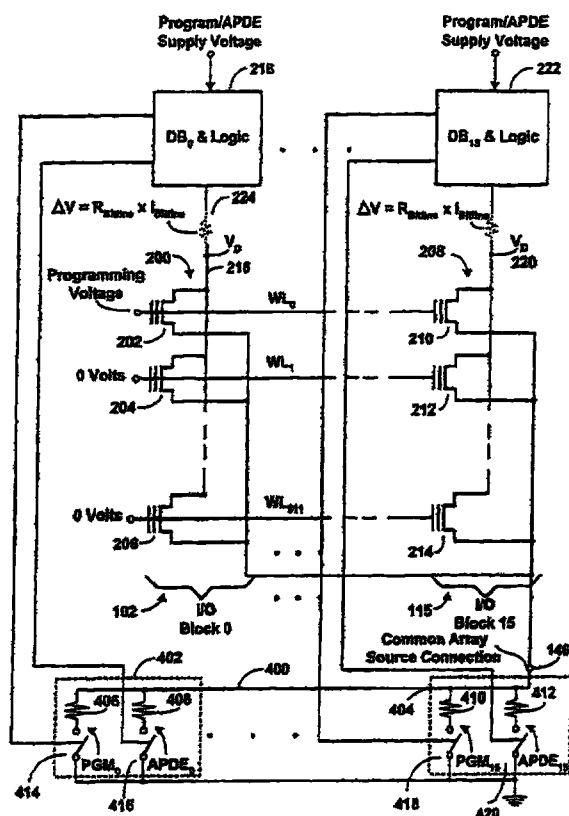
(84) Designated States (regional): European patent (AT, BE,
CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC,
NL, PT, SE).

Published:

- With international search report.
- Before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments.

[Continued on next page]

(54) Title: CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAMMING AND OVER-ERASE CORRECTION MODES IN FLASH EEPROM



(57) Abstract: A method of and a flash memory device for quenching bitline leakage current during programming and over-erase correction operations. The flash memory cells are organized in an array of I/O blocks with each block having columns and rows. An array of resistors is connected between the common array source connection and ground. The array of resistors is made up of sets of resistors, each set having a programming mode resistor and an APDE mode resistor. A data buffer switches either a programming mode resistor or ADPE mode resistor into the circuit when a bitline is selected for either programming or APDE. The values of the resistors are selected to raise the voltage at the source above a selected threshold voltage of the memory cells so that over-erased cells will not provide leakage current to the bitline during either programming or APDE.

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